

X-Parameters: The μ Stability Factor and Its Application to Avoid Oscillation Problems During the Characterization of Power GaN FETs

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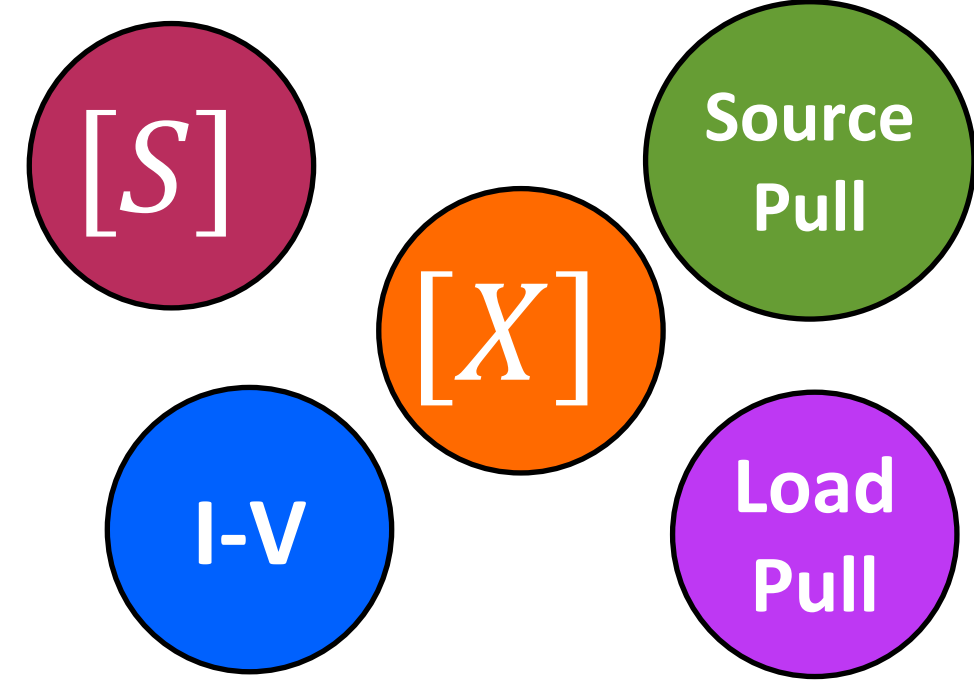
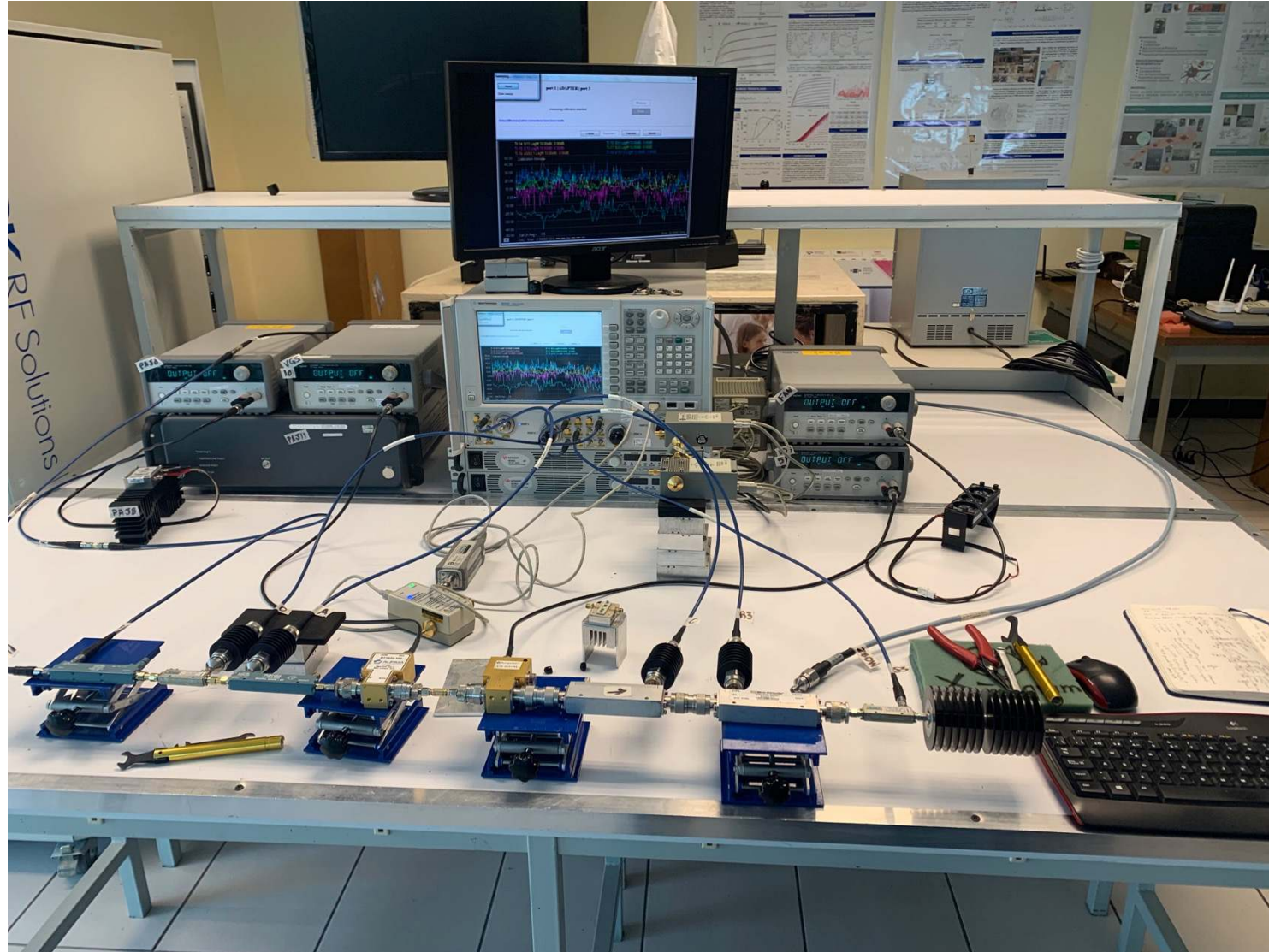


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- 1. Introduction**
- 2. X-Parameters Background**
- 3. The μ Stability Factor in Terms of the X-Parameters**
- 4. Experimental Results**
- 5. Conclusion**



Transistor characterization is fundamental for developing:

- Linear Model
- Nonlinear Model
- Microwave Circuits

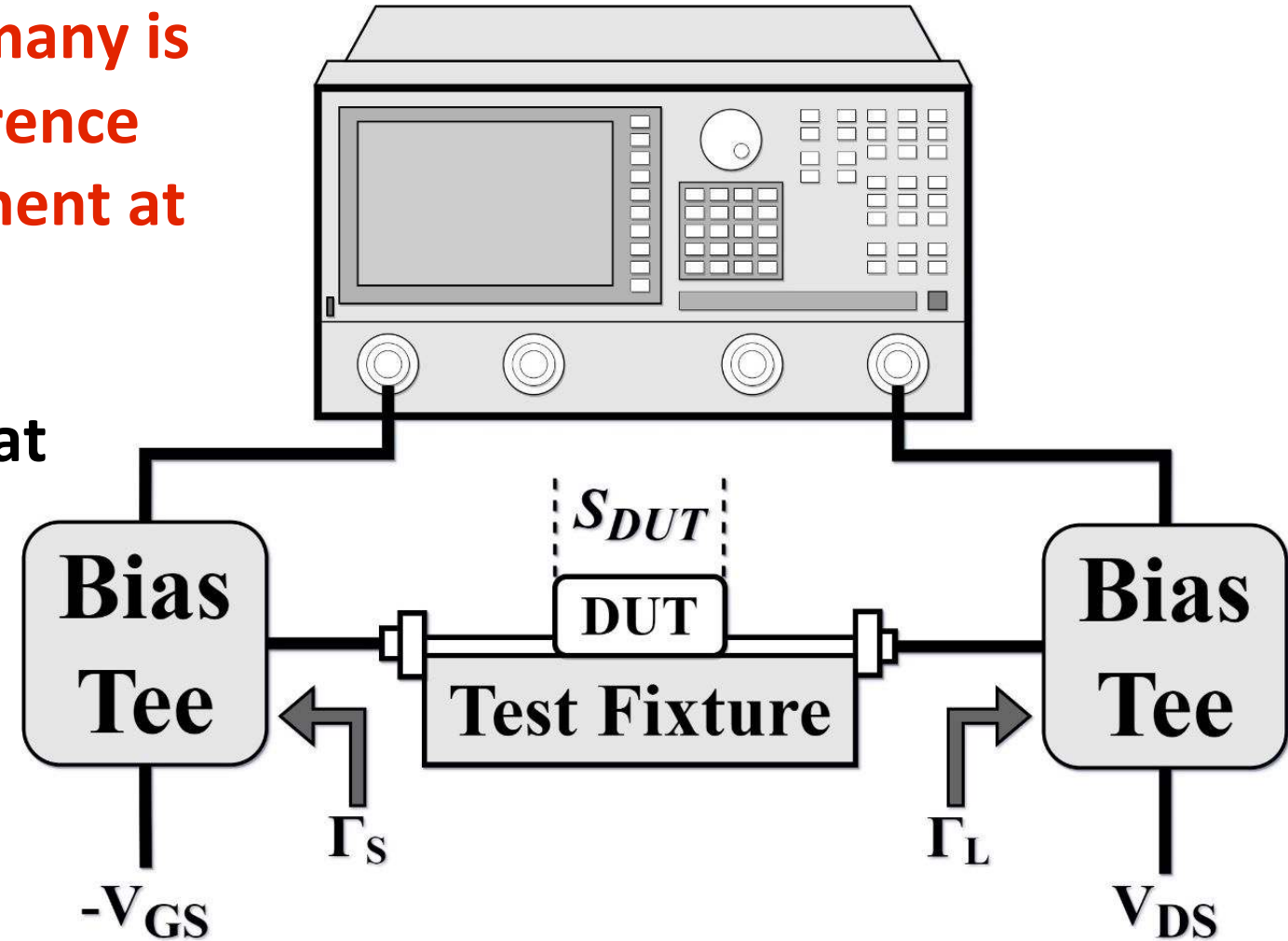


The main concern for many is establishing the reference plane of the measurement at the DUT plane

However, there are other things that one should worry about



An instability problem could appear, making it impossible to characterize the FET



Introduction

Instability during the characterization process is something that is not mentioned very often

Transistor Stability Analysis

Linear

Nonlinear

S-Parameters

- Rollet Factor (K)
- Stability Circles
- Edward-Sinsky Factor (μ)

★ Simple methodology ★ Frequency domain
★ Easy and straightforward results interpretation

- Nyquist
- Hopf Bifurcation

➡ Mathematically more complex
➡ Not easy to interpret the results
★ Time&Frequency domain

A simple methodology to analyze the stability of the FET as a function of the frequency and the input power could help to answer the following questions:

- **What causes the instability?**
- **How important is it to analyze the stability of a FET when it is operating in saturation?**
- **How can we stabilize the FET?**

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The X-parameters describe the reflected wave of a Device Under Test (DUT) as a function of the bias (DC) and the input signal as:

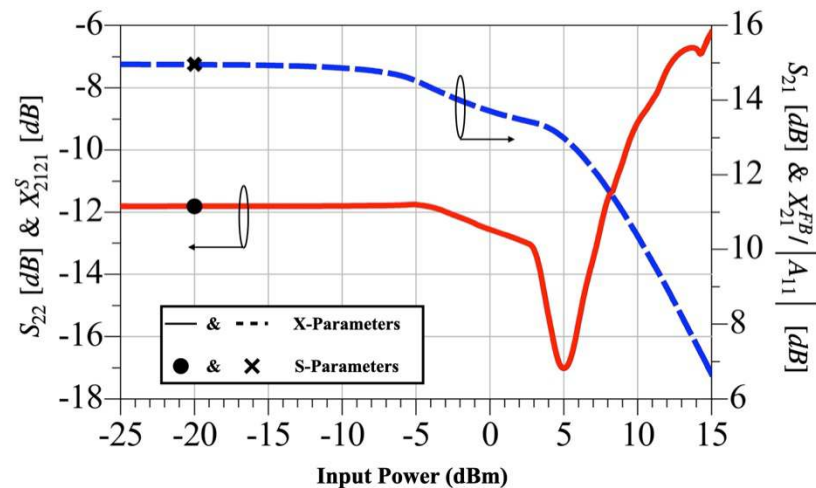
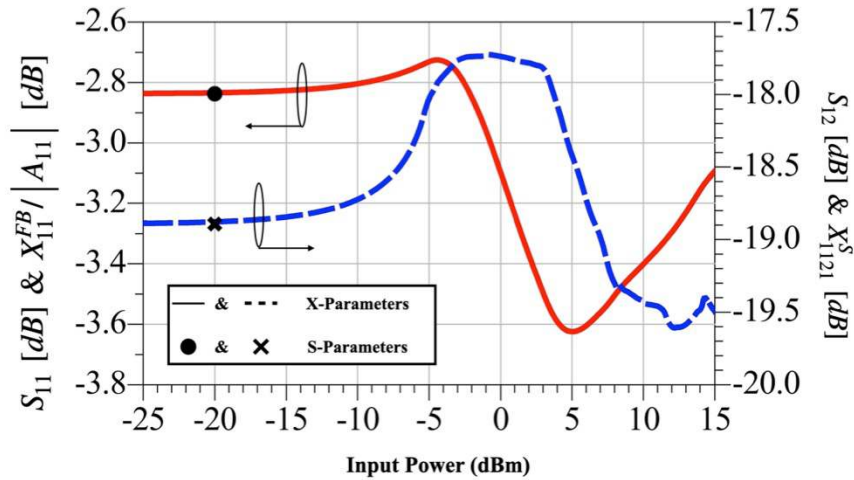
$$B_{pk} \left(DC, |A_{11}| \right) = \underbrace{X_{pk}^F \left(DC, |A_{11}| \right) P^k}_{\text{The harmonic of the output voltage}} + \sum_{\substack{q=1, l=1 \\ (q,l) \neq (1,1)}}^{q=N, l=K} \left[\underbrace{X_{pkql}^S a_{ql} P^{k-l} + X_{pkql}^T a_{ql}^* P^{k+l}}_{\text{Describe the change in the traveling wave between the ports } p \text{ and } q \text{ at the harmonics } k \text{ and } l} \right]_{(1)}$$

Where:

- | | |
|-----------------------|-----------------------------------|
| p → the output port | k → harmonic of the output port |
| q → the inputport | l → harmonic of the input port |

X-Parameters Background

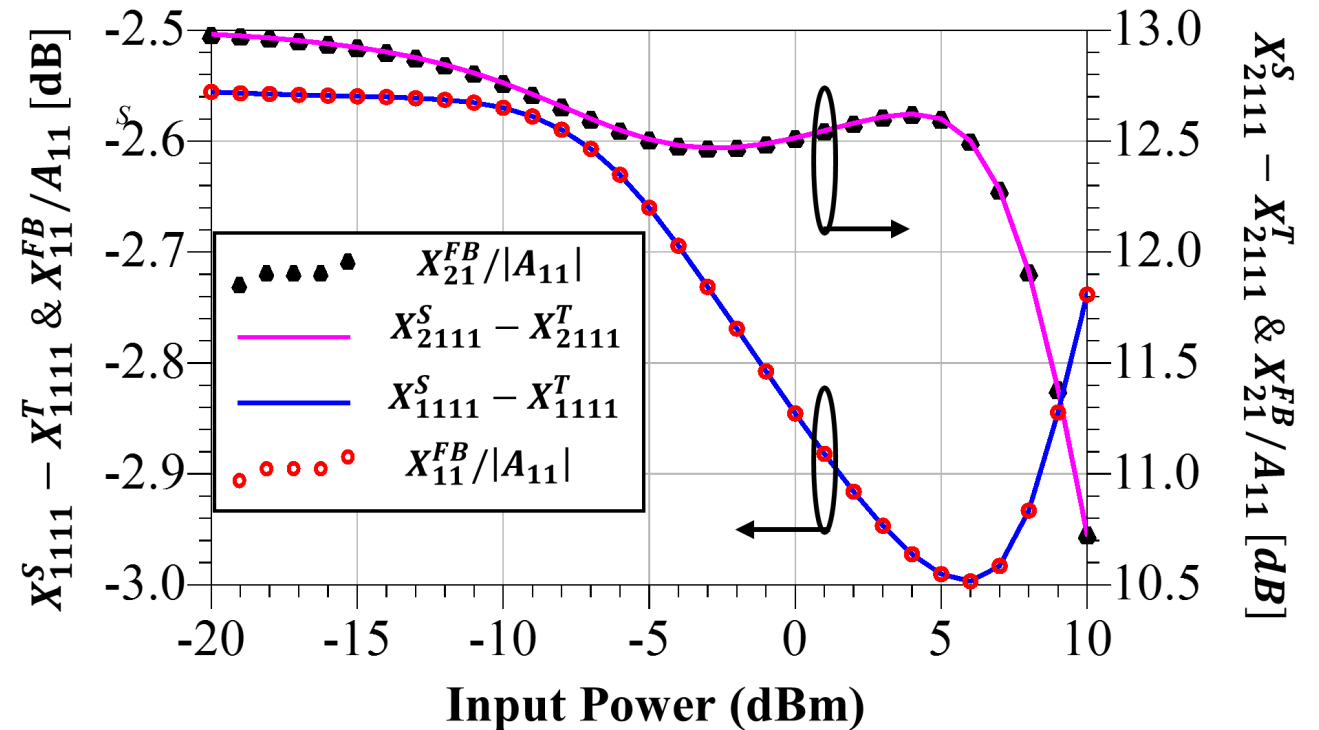
At low input power the X^S term converge with the S-Parameters



Whereas the Large-Signal (LS) behavior can be described by:

$$S_{11}^{LS} \rightarrow X_{1111}^{ST} = \frac{X_{11}^F}{|A_{11}|} \quad (2a) \quad S_{12}^{LS} \rightarrow X_{1121}^{ST} = X_{1121}^S - X_{1121}^T P^2 \quad (2b)$$

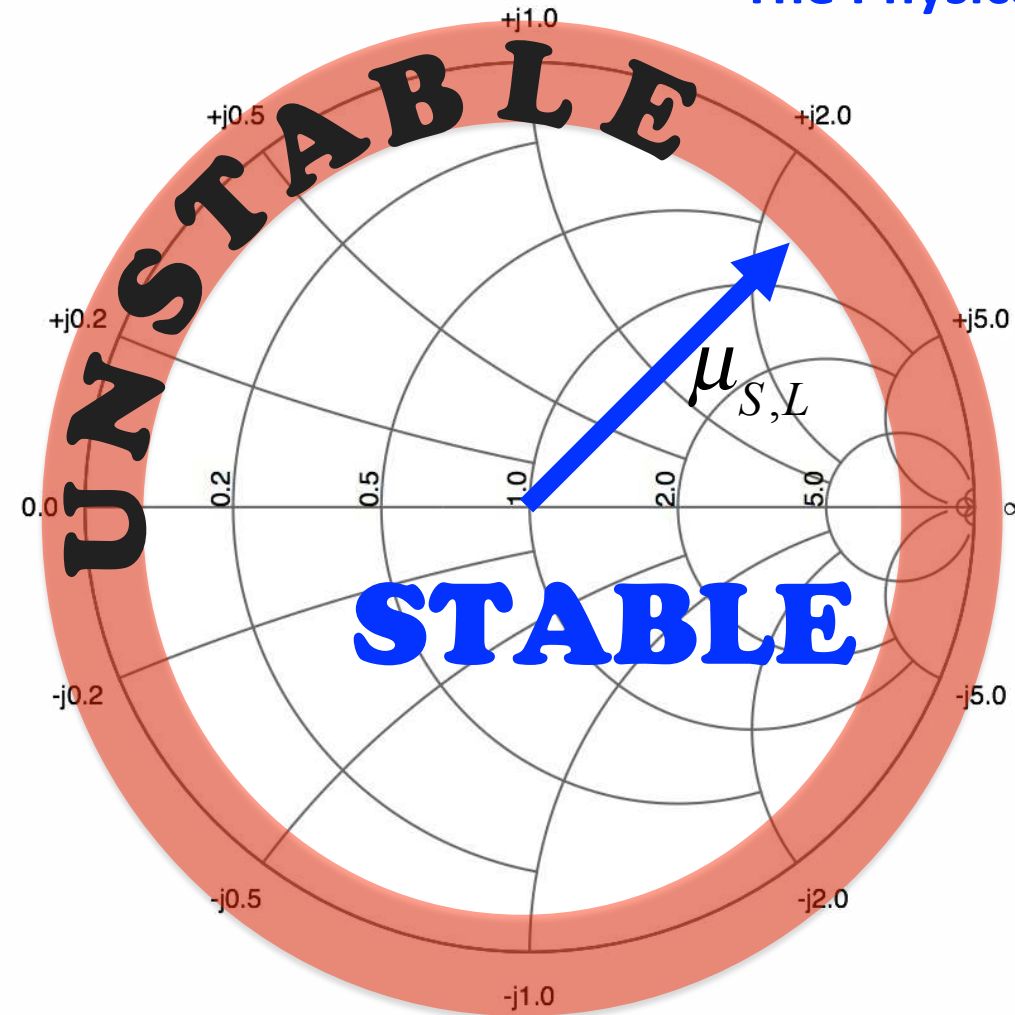
$$S_{21}^{LS} \rightarrow X_{2111}^{ST} = \frac{X_{21}^F}{|A_{11}|} \quad (2c) \quad S_{22}^{LS} \rightarrow X_{2121}^{ST} = X_{1121}^S - X_{2121}^T P^2 \quad (2d)$$



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The Physical Interpretation

The μ stability factor indicates the minimum distance from the center of the Smith chart to the possible Γ that makes unstable the transistor



The μ stability factor is defined as:

$$\mu_S = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{21} S_{12}|} \quad (3)$$

$$\mu_L = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{21} S_{12}|} \quad (4)$$

Where:

$$\Delta = S_{11} S_{22} - S_{12} S_{21} \quad (5)$$

If $\mu_{s,L} > 1$, the FET is **UNCONDITIONALLY STABLE**, otherwise, the FET is **CONDITIONALLY STABLE**

Since S-parameters are for linear regimen,
the question is....



¿What happened in the nonlinear regimen of the FET?

Thus, the μ stability factor in terms of the X-parameters is proposed to write

as:

$$\mu_S^{ST} = \frac{1 - |X_{2121}^{ST}|^2}{\left| X_{1111}^{ST} - \Delta \left(X_{2121}^{ST} \right)^* \right| + \left| X_{2111}^{ST} X_{1121}^{ST} \right|} \quad (6)$$

$$\mu_L^{ST} = \frac{1 - |X_{1111}^{ST}|^2}{\left| X_{2121}^{ST} - \Delta \left(X_{1111}^{ST} \right)^* \right| + \left| X_{2111}^{ST} X_{1121}^{ST} \right|} \quad (7)$$

**X-Parameters can
describe the
nonlinear behavior
of the FET**



The advantages of using X-parameters in the stability analysis are:

- **Allows to analyze the stability of the FET in frequency and input power.**
- **The interpretation of the stability analysis is straightforward.**
- **The analysis time is reduced compared with other methods.**

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Experimental Results

SWEEP PLAN

SweepPlan

SwpPlan1

Start=2 Stop=4 Step= Lin=101

UseSweepPlan=

SweepPlan=

Reverse=no



X-Parameters

X_Param

XP2

Freq[1]=f GHz

Order[1]=12

SwpVar[1]="f"

SwpPlan[1]="SwpPlan1"

XParamMaxOrder=3

Var
Eqn

VAR

VAR1

f=1.0

X2P
XNP2

XP_Source

PORT1

Num=1

Z0=(50+j*0) Ohm

LS_freqHarms[1]=1

LS_format[1]=Mag/Phase

LS_swpType[1]=Use sweep

LS_value[1,Mag]=

LS_start[1,Mag]=dbmtow(-10)

LS_start[1,Phase]=0

LS_stop[1,Mag]=dbmtow(26)

LS_stop[1,Phase]=

LS_numPts[1,Mag]=37

LS_numPts[1,Phase]=

XP_Load

PORT2

Num=2

Z0=(50+j*0) Ohm

Load_mode=Impedance

LS_freqHarms[1]=1

LS_format[1]=Mag/Phase

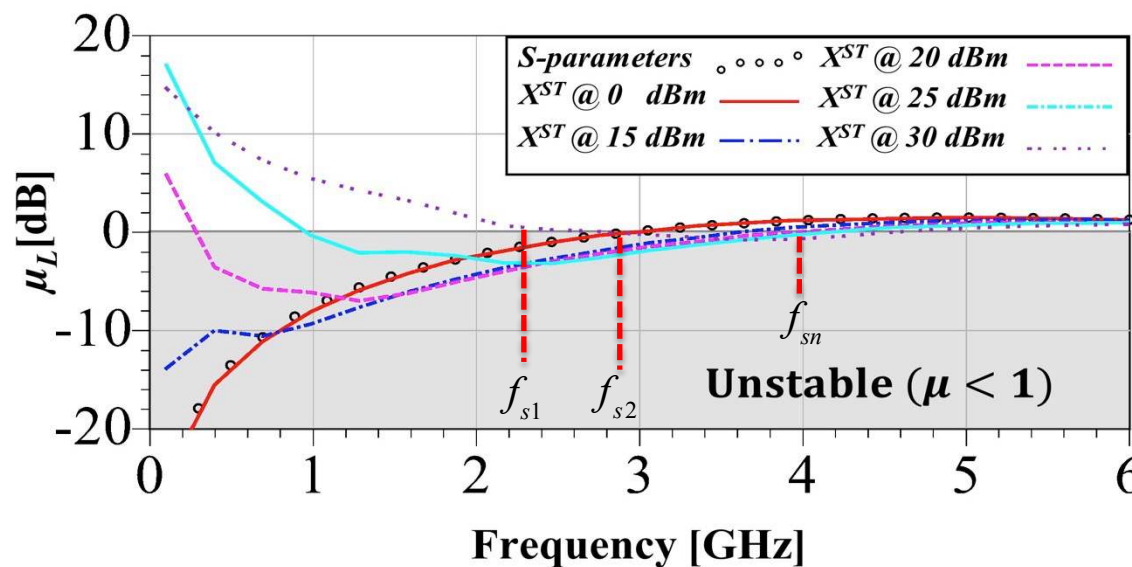
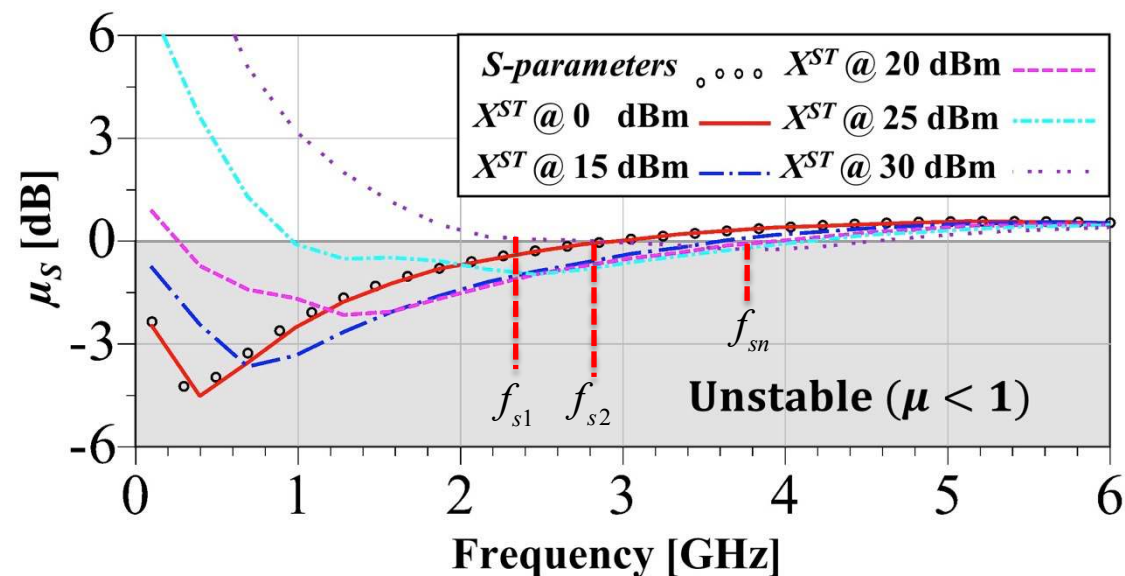
LS_swpType[1]=Use sweep

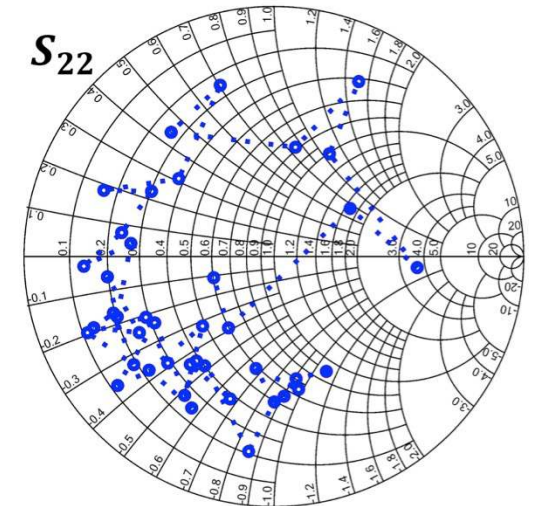
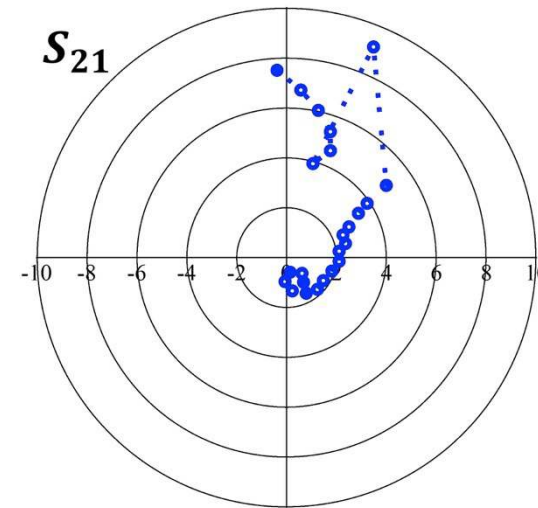
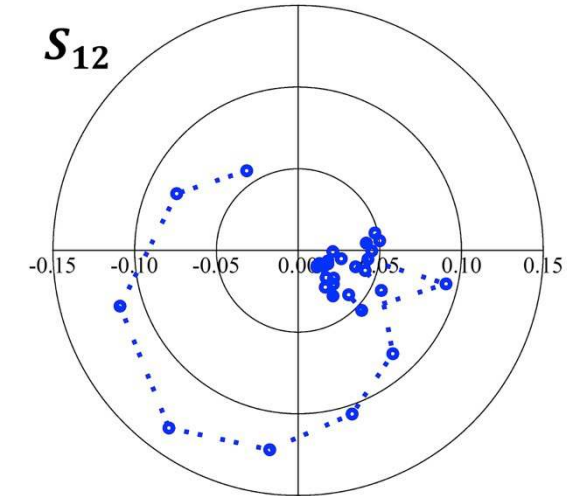
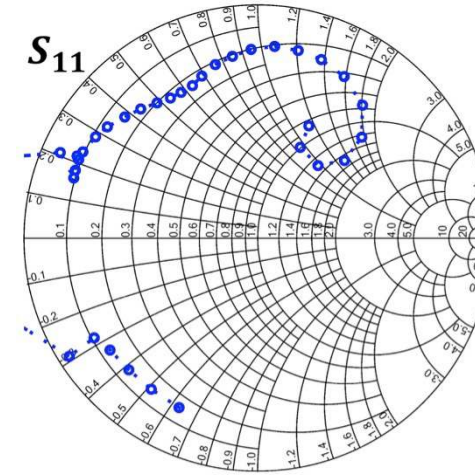
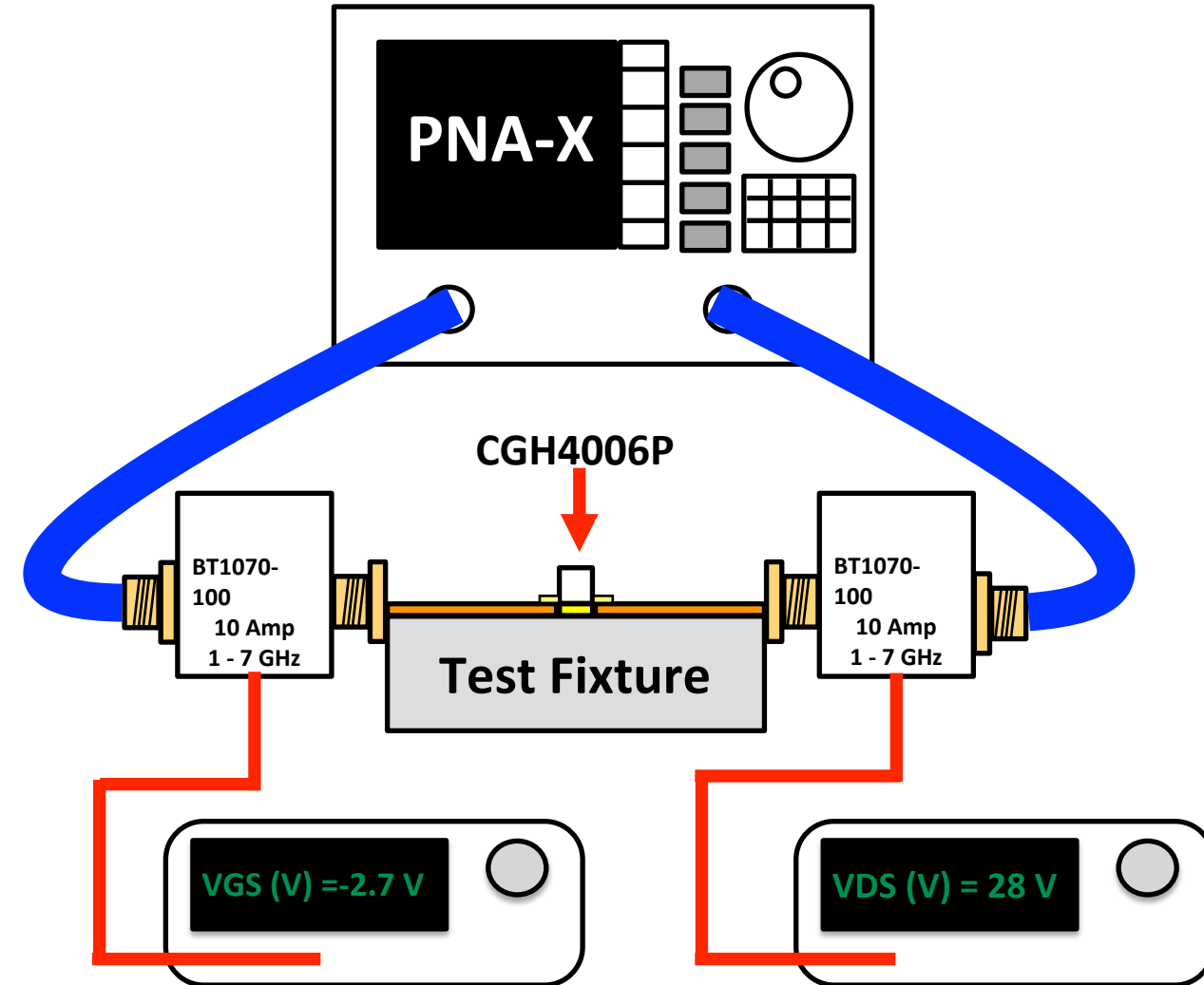
LS_value[1,Mag]=

LS_start[1,Mag]=

LS_stop[1,Mag]=

LS_numPts[1,Mag]=

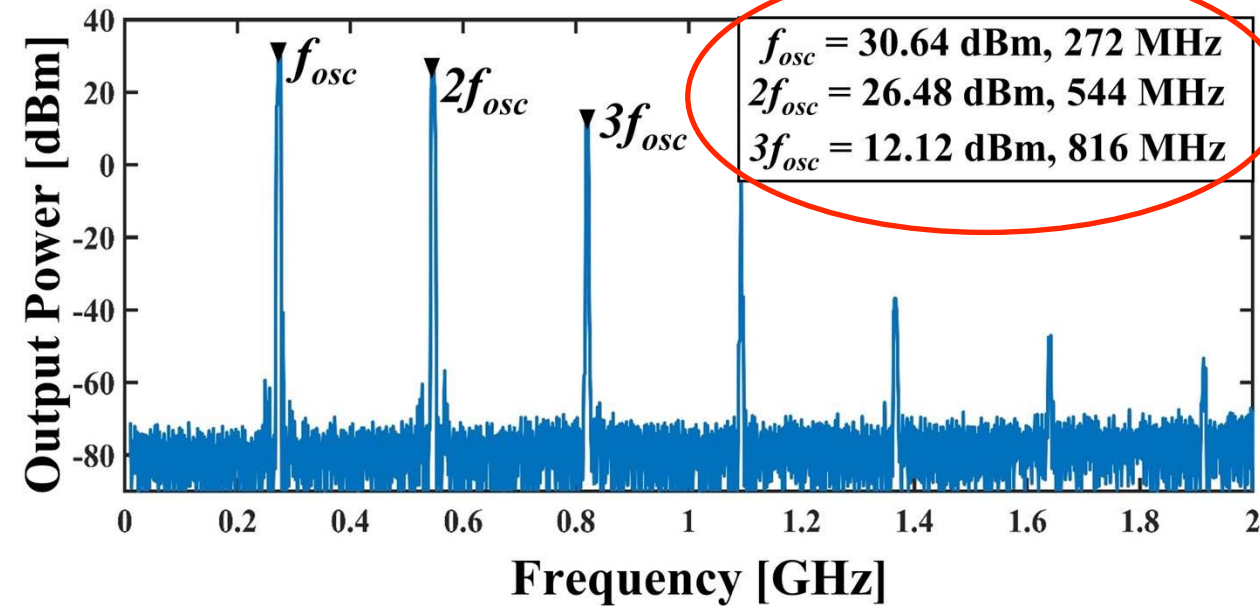
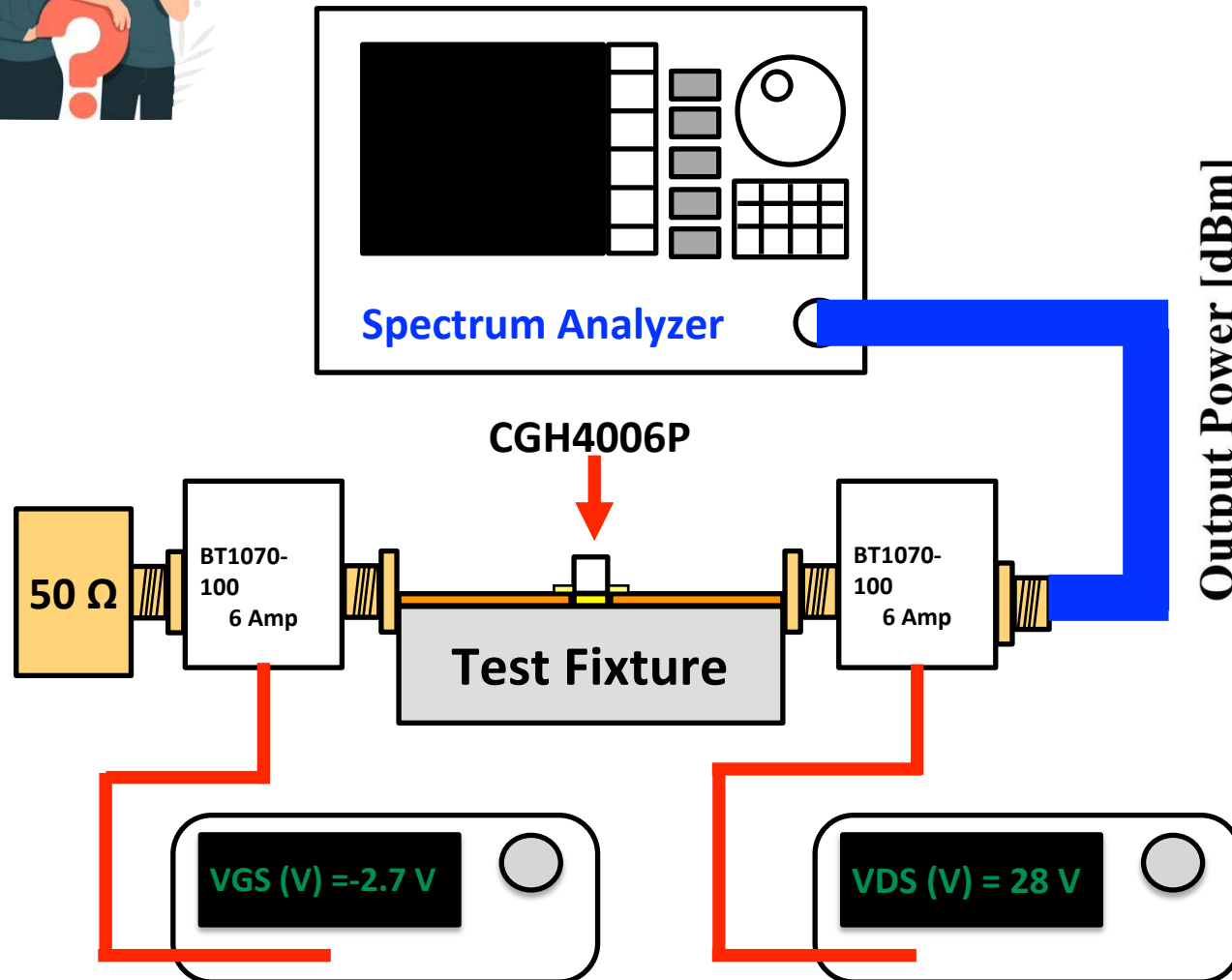




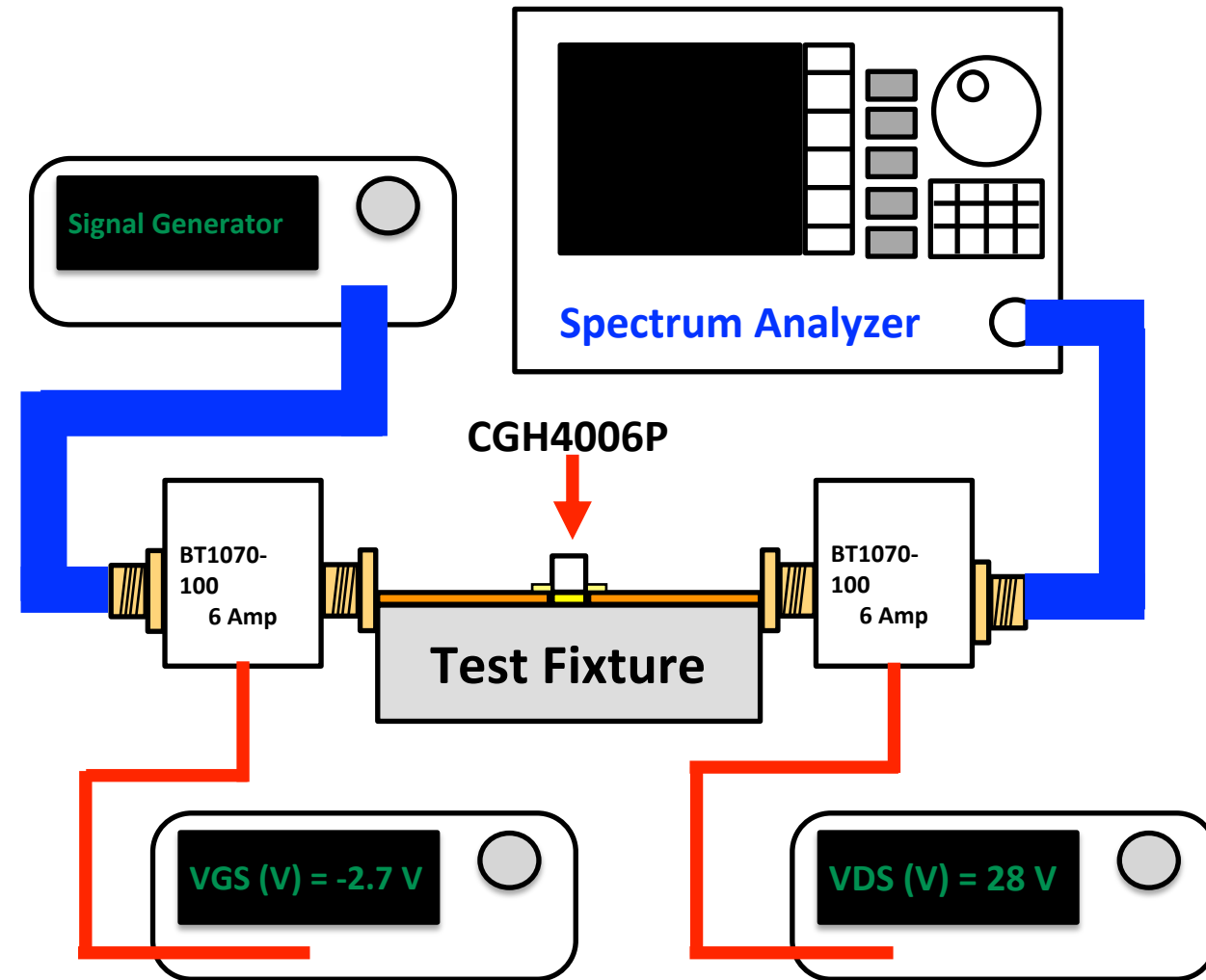
It does not look like a typical S-Parameters measurement

The question is, **WHAT HAPPENED?**

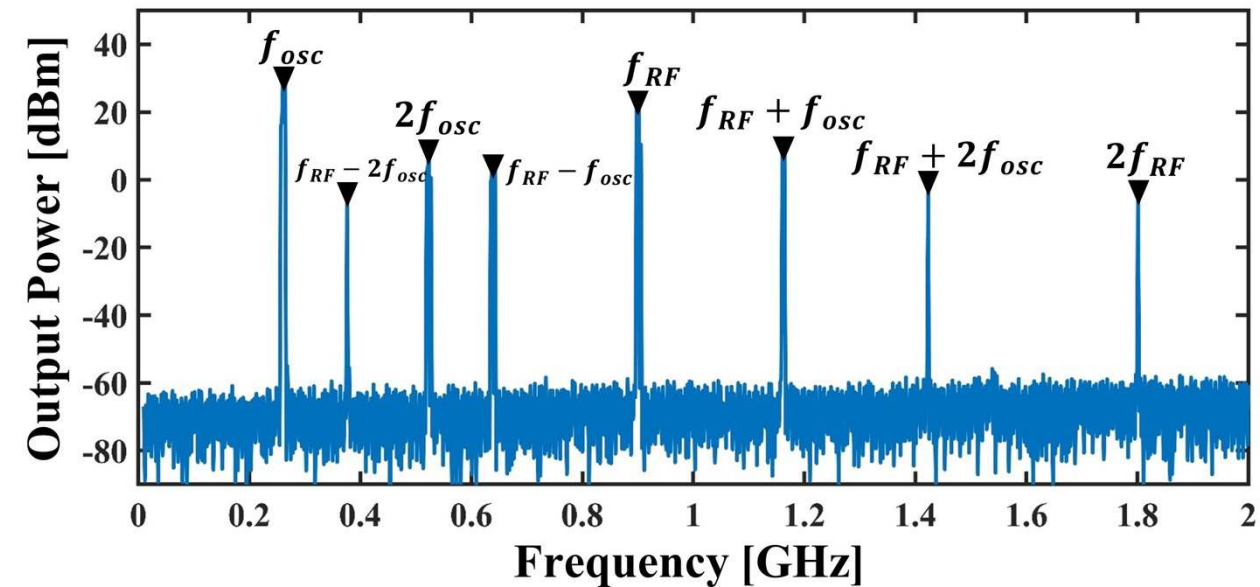
Parametric Oscillations



This is an indication that the FET is **UNSTABLE**

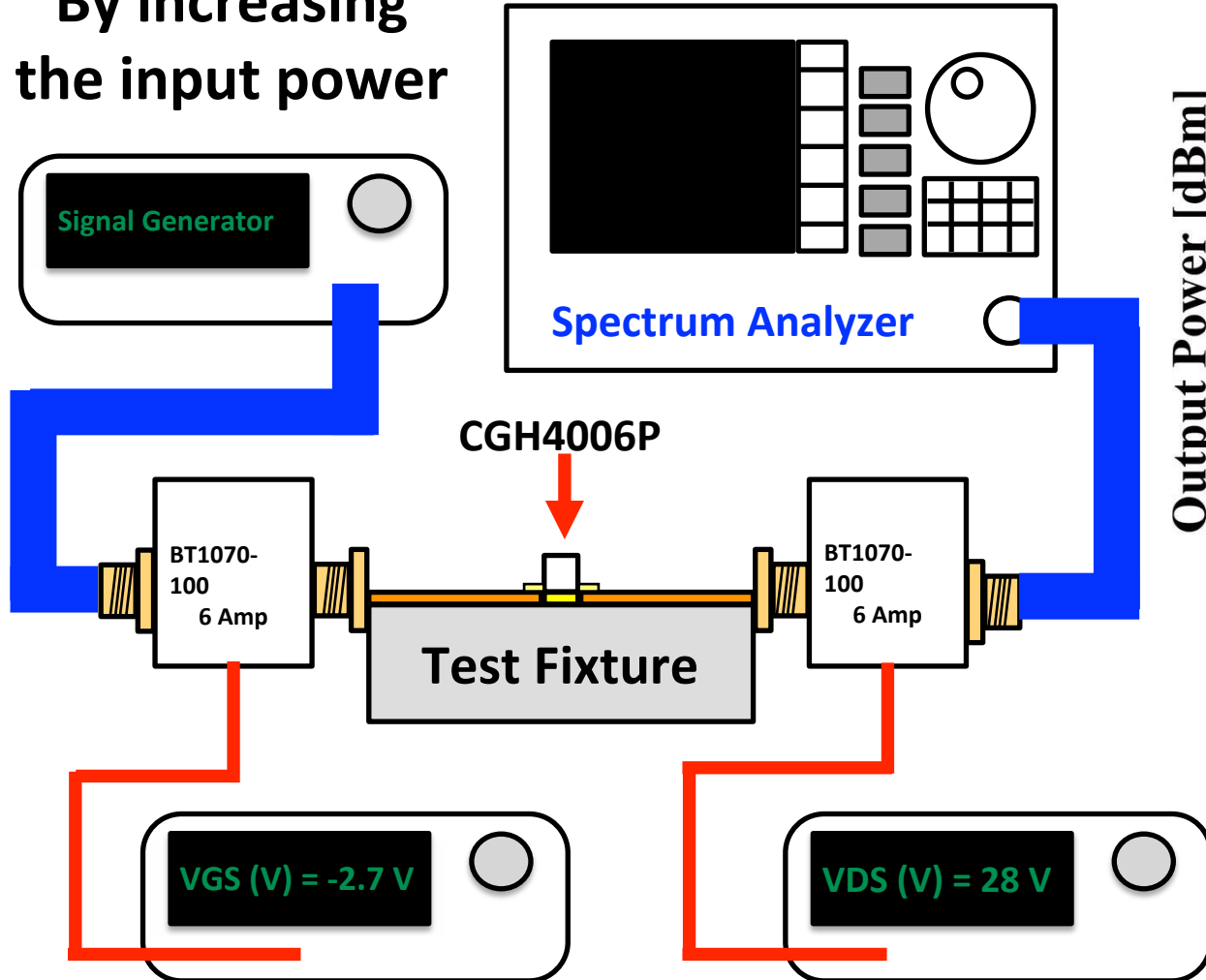


Parametric Oscillations + Intermodulation Distortion

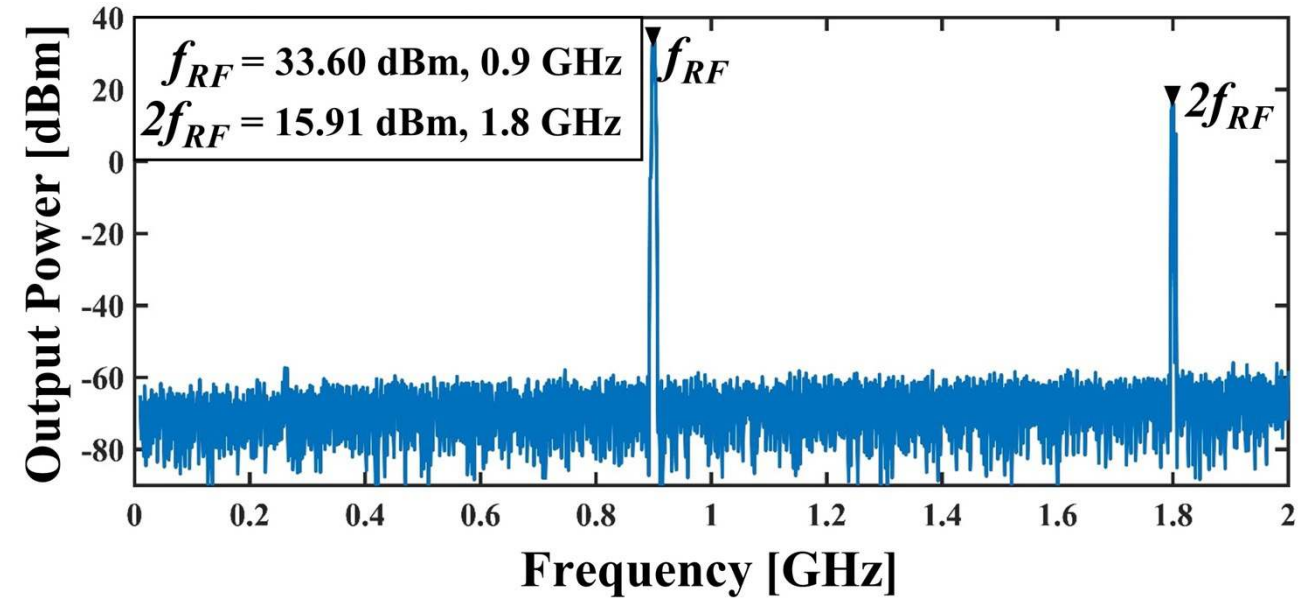


A very **BAD IDEA** to use the FET as an amplifier

By increasing
the input power



...and as predicted in **SIMULATION**



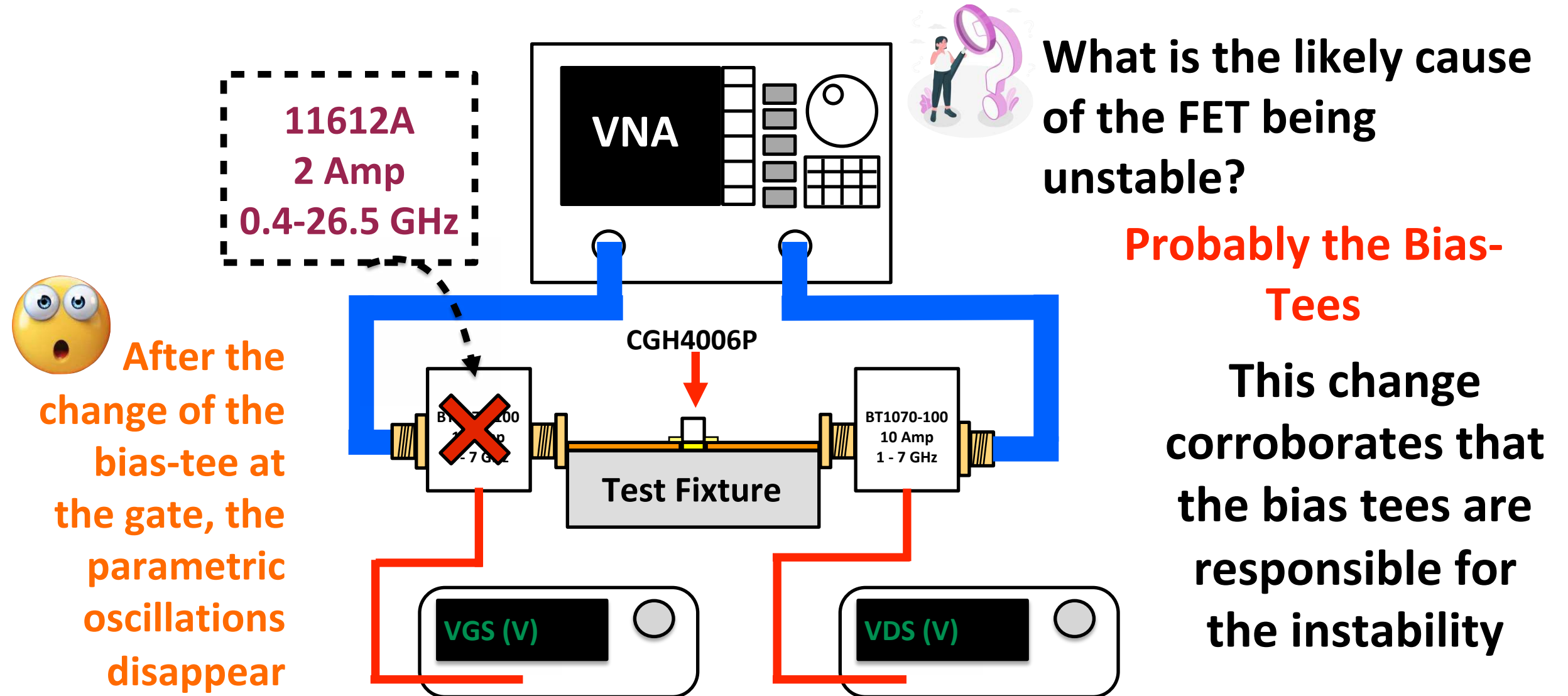
The parametric oscillations
have been disappearing. It
seems the FET is **STABLE**

This experiment suggests:

- **When the gain is compressed, the FET is stable.**
- **The main problem of stability lies in the case of low input power.**

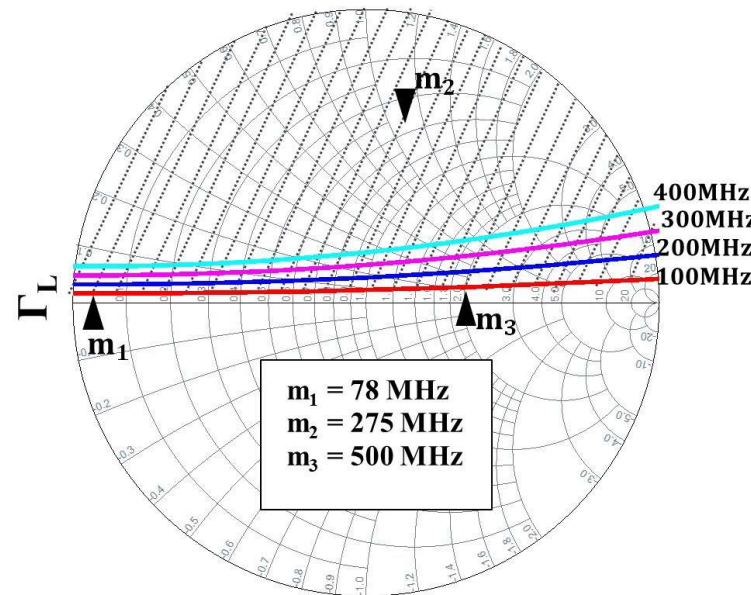
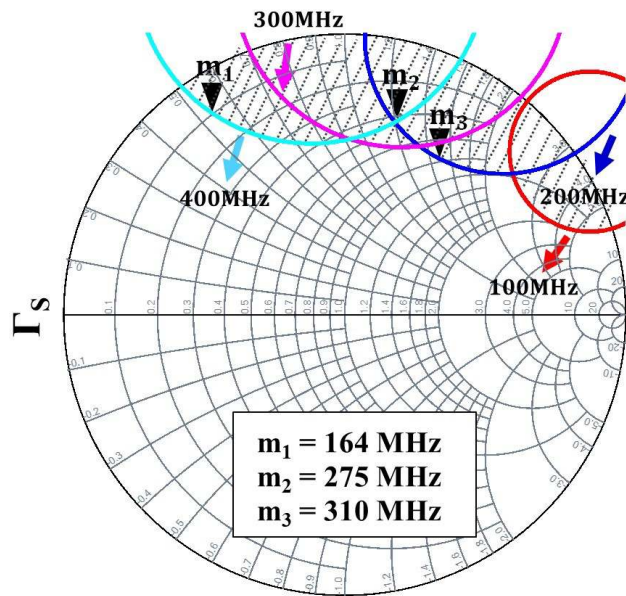


Thus, the classical stability analysis using stability circles could help to understand the instability problem of the FET at the characterization moment

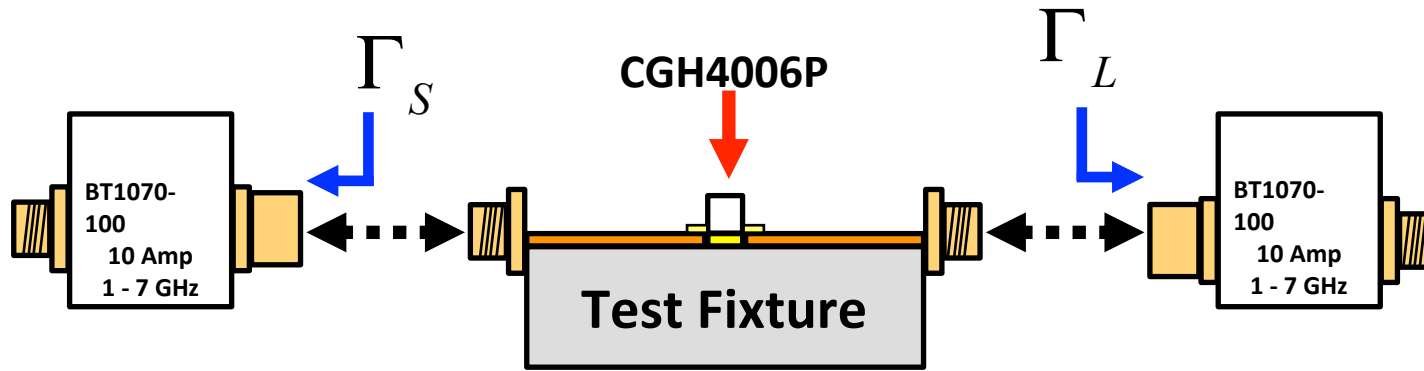


A first approach to verify the effect of the Bias-Tee is computing the input and output stability circle of the FET with the model of the vendor

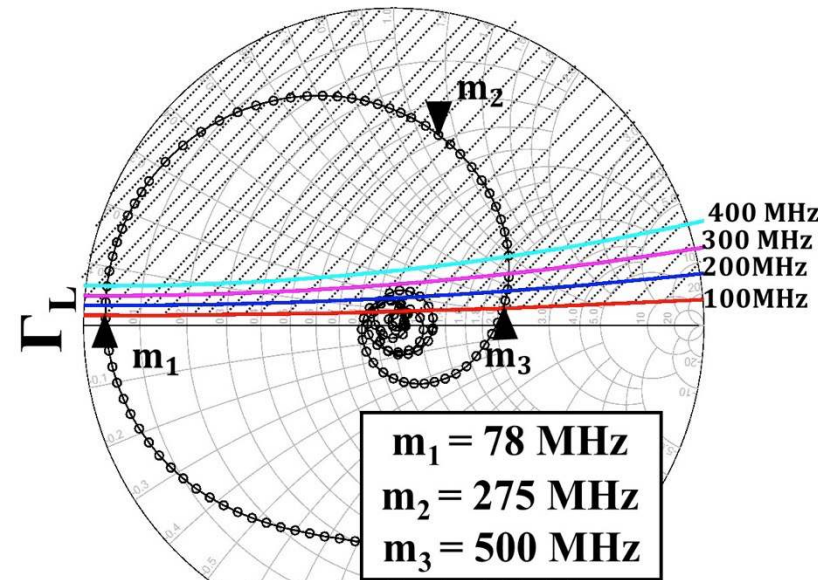
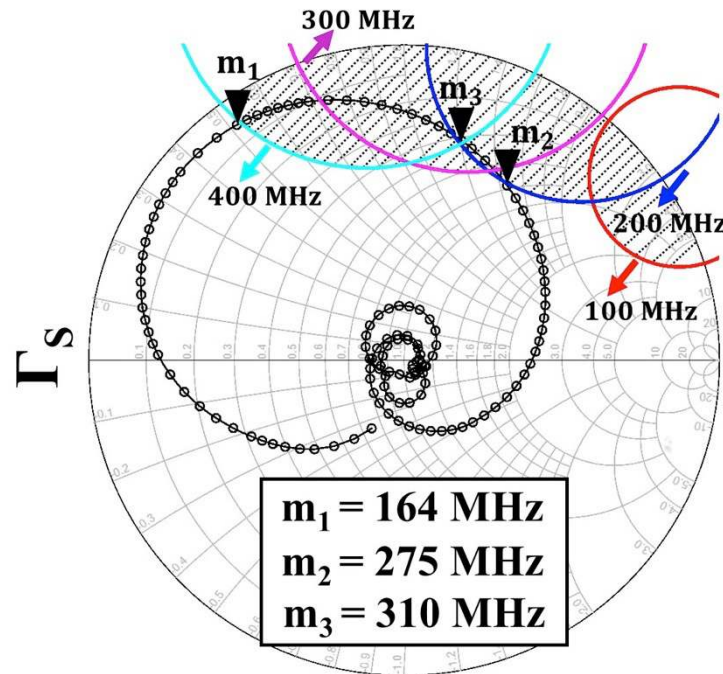
A simulation at low-frequency of the stability circles shows the possible region of Γ can cause the instability of the GaN FET



Experimental Results

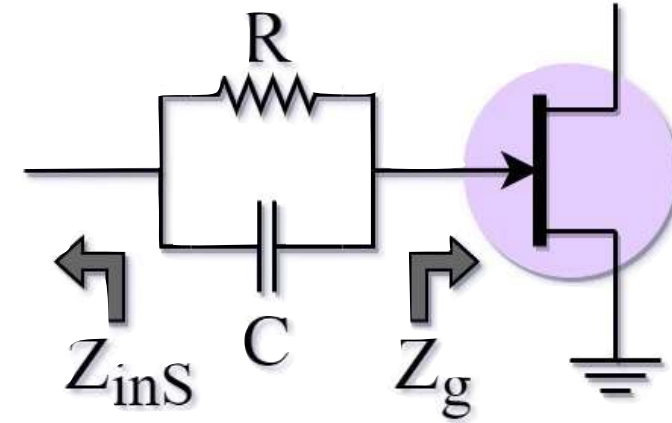


Comparing the frequency range at which Γ_S y Γ_L are inside the instability area simultaneously reveals that at 164 – 275 MHz, the FET is potentially unstable



This information is suitable for designing a stability circuit

In the literature, a parallel R-C network in series with the gate of the GaN FET is widely used, but without an explanation of how to determine the value of R or C



This R-C network works as a high-pass filter, where the cut-off frequency (f_c) is determined as:

$$f_c = \frac{\kappa}{2\pi C\alpha} \pm \frac{\sqrt{R\kappa - \alpha \left[(R + \rho)^2 + \kappa^2 - 8\text{Re}(Z_{inS}Z_g) \right]}}{2\pi RC\alpha} \quad (4)$$

Where:

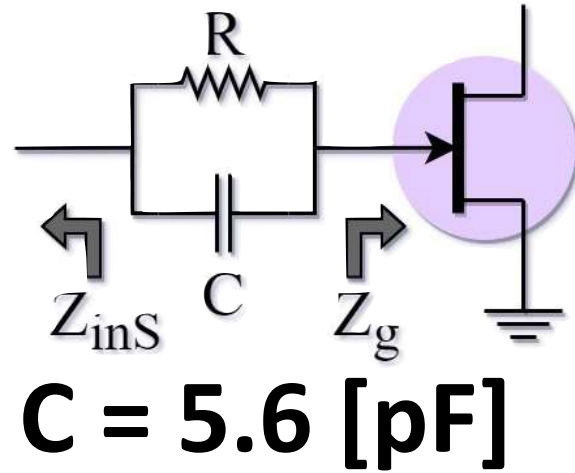
$$\kappa = \text{Im}(Z_{inS} + Z_g) \quad (5)$$

$$\rho = \text{Re}(Z_{inS} + Z_g) \quad (6)$$

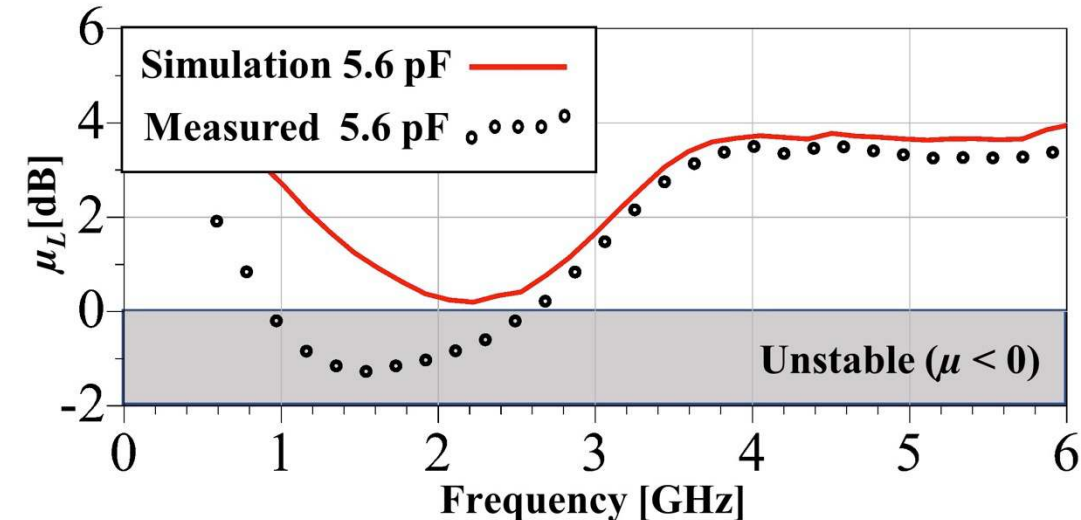
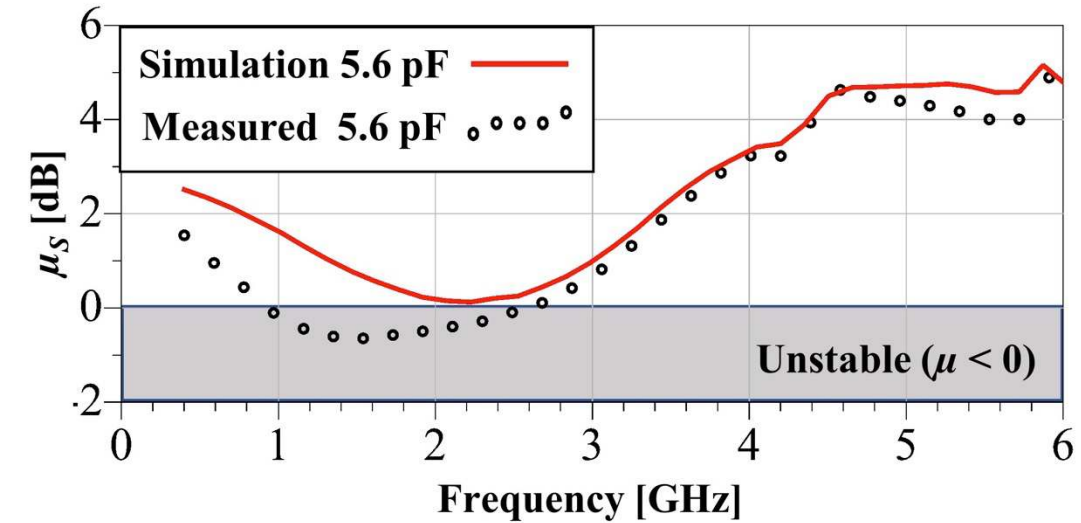
$$\alpha = \kappa^2 + \rho^2 - 8\text{Re}(Z_{inS}Z_g) \quad (7)$$

Experimental Results

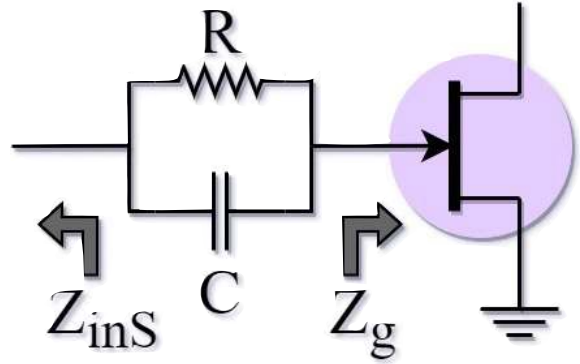
Thus, assuming a $f_c = 0.4$ GHz, $R = 100 \Omega$, $Z_{inS} = 50 \Omega$, and Z_g is the input impedance of the FET obtained with S-parameters



Simulations do not agree with the measurements, and it seems that it is unstable

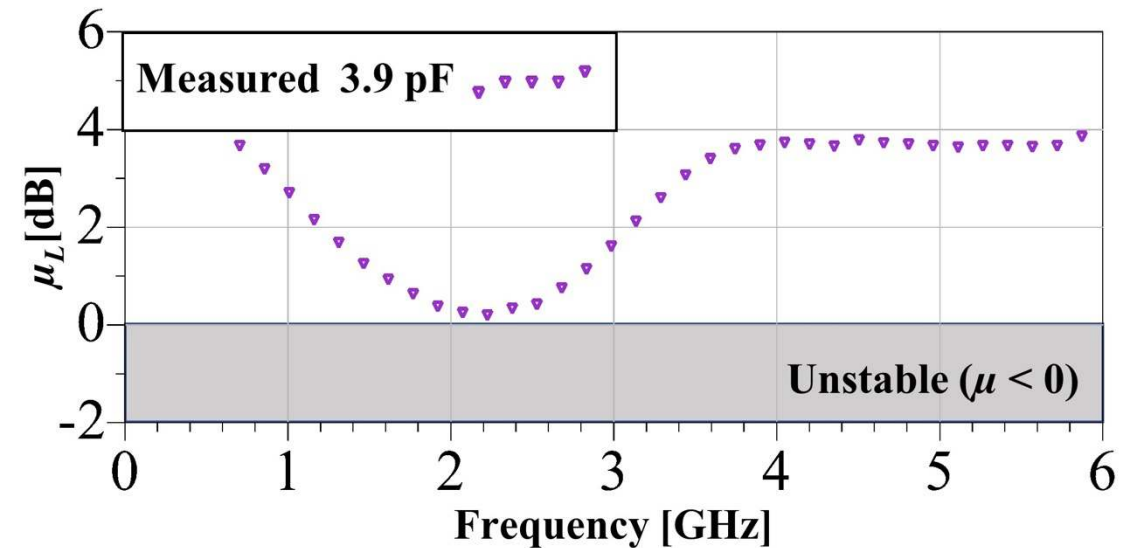
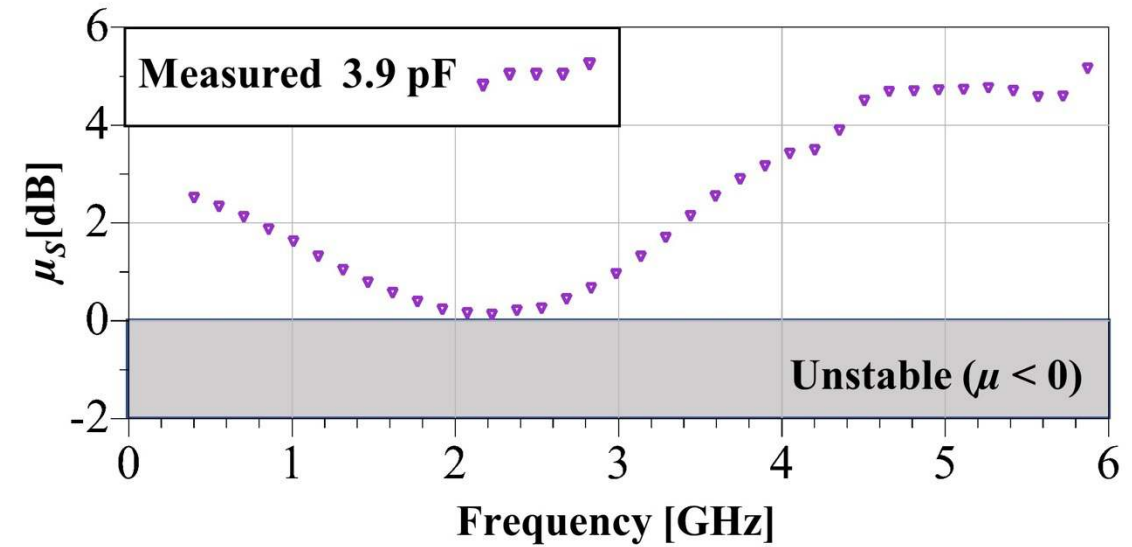


Tuning the value of C , shows that



$$C = 3.9 \text{ [pF]}$$

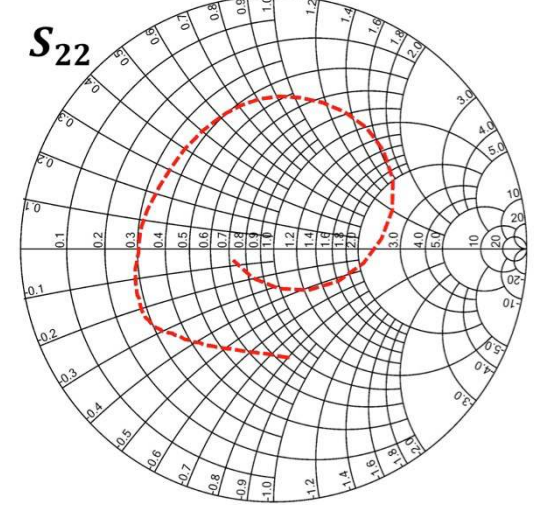
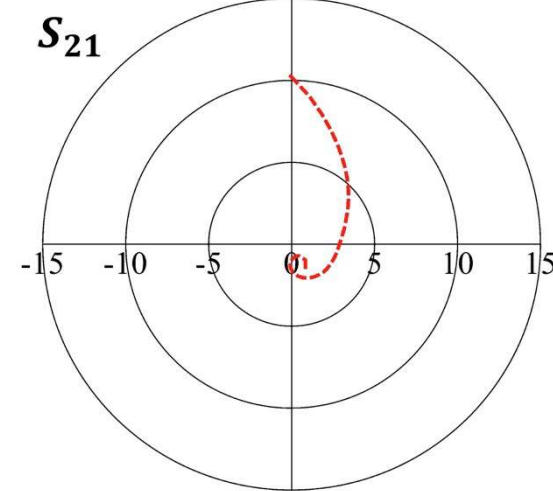
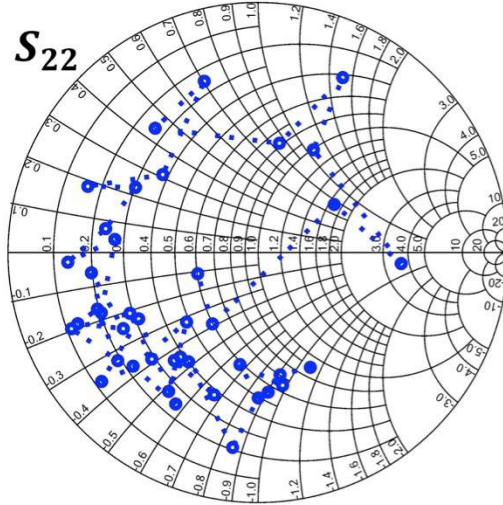
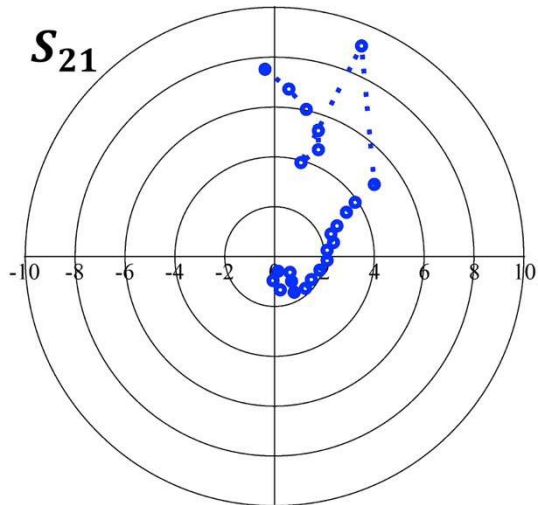
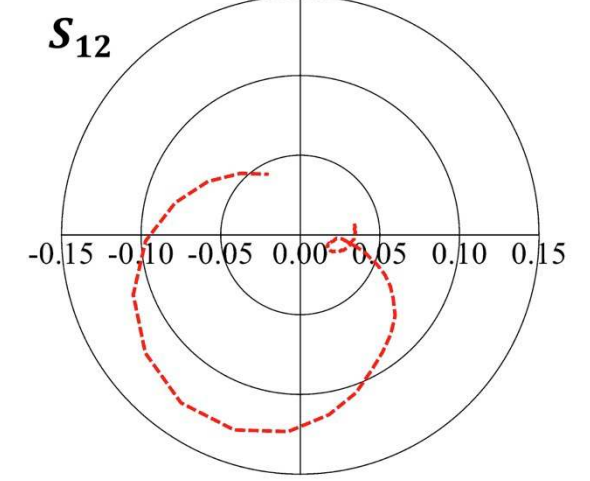
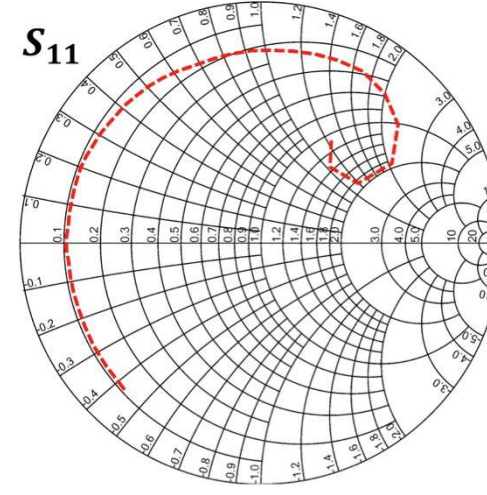
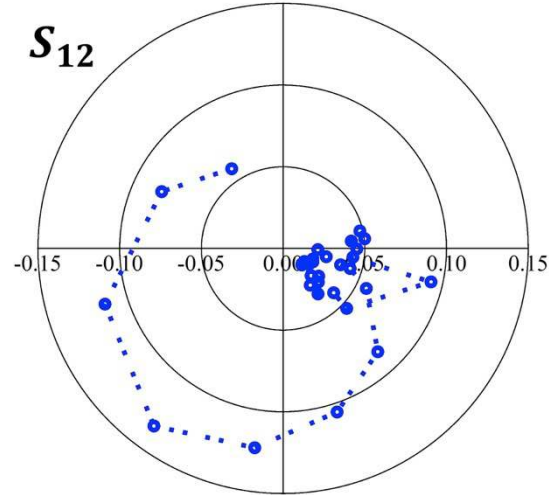
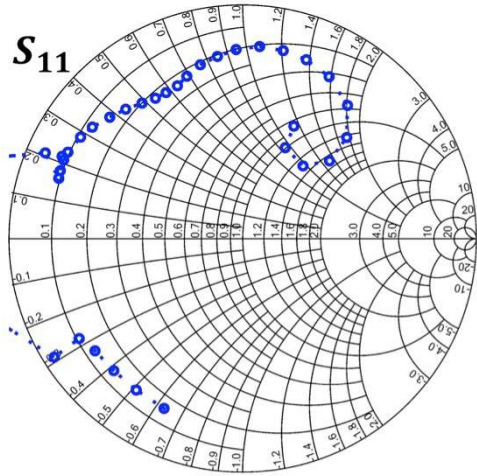
Now the measurements
show that the FET is
STABLE



Experimental Results

w/o Stabilized

Stable



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- During the characterization of the FET, the bias tees could be the source that caused the instability.
- Incorporating the X-Parameters in the μ factor allows for analyzing the effect of the input power on the stability of the FET.
- The simulation and experimental results corroborated that compressing the gain can stabilize an unstable FET.
- Since the FET under high gain compression level condition is stable, the small-signal stability analysis methods become more relevant.
- Although the results demonstrated that the FET is stable under high-gain compression, it is more recommendable to use a high-pass filter at the gate of FET with cut-off frequency higher than the possible parametric oscillations to stabilize the transistor.