We4A-5

A 3.5~7.5 GHz GaAs HEMT Cryogenic Low-Noise Amplifier Achieving 5 Kelvin Noise Temperature for Qubits Measurement

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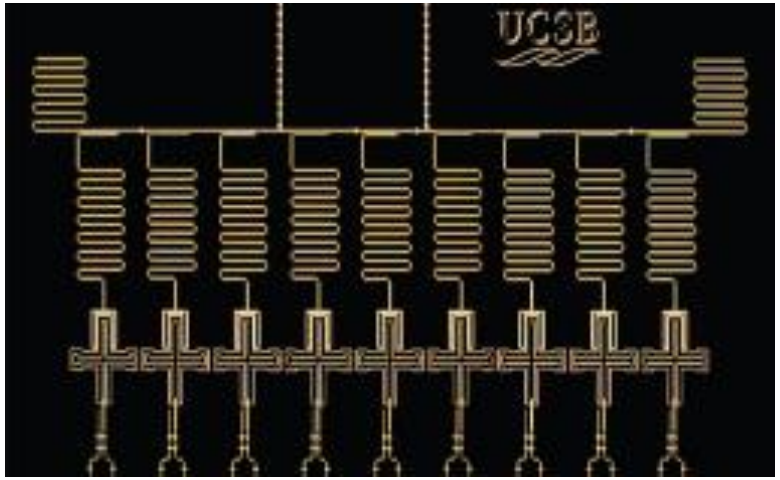
Outline

- Background
- The Cryogenic LNA: Prior Art
- GaAs HEMT Cryogenic Low-Noise Amplifier Design
- Measurements
- Conclusion

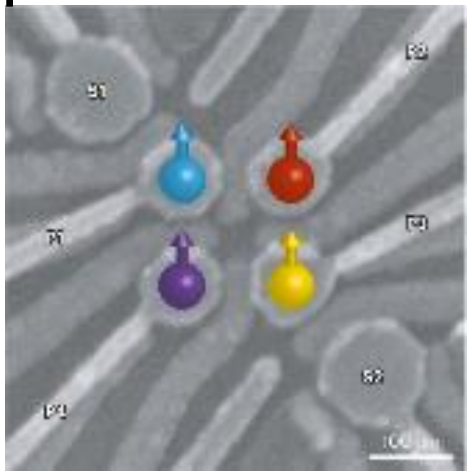
Background

❑ Physical Qubits in Quantum Processor

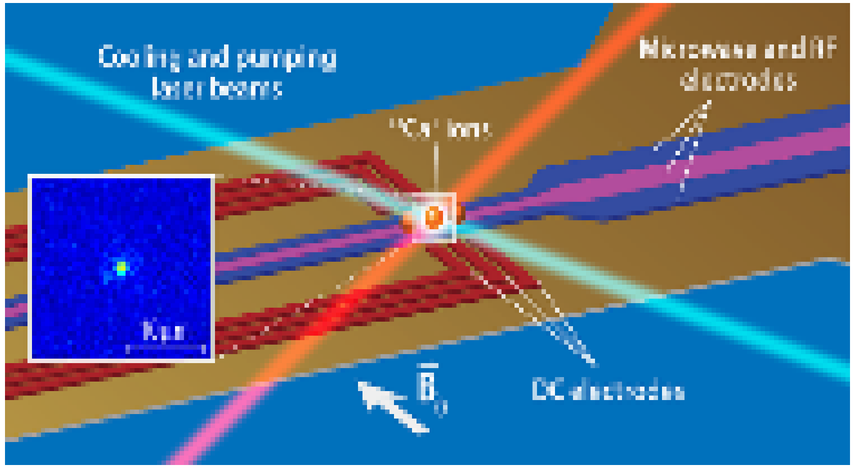
- Superconducting Qubits
- Semiconductor Spin qubits
- Trapped Ions Qubits



Kelly et al. Nature 519, 66–69 (2015).



Hendrickx et al. Nature 591, 2021.



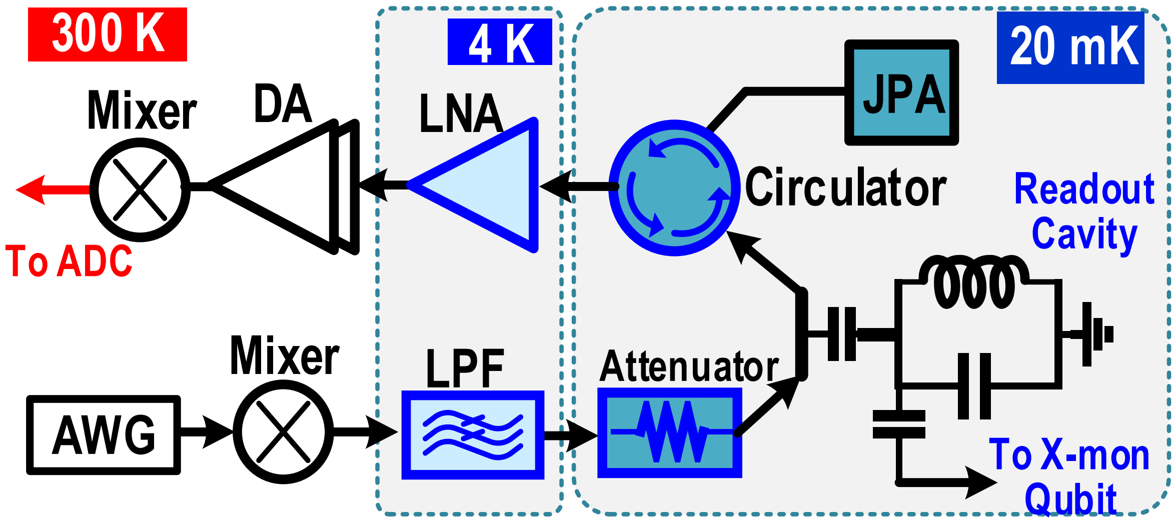
Kim, Physics 7, 119 (2014)

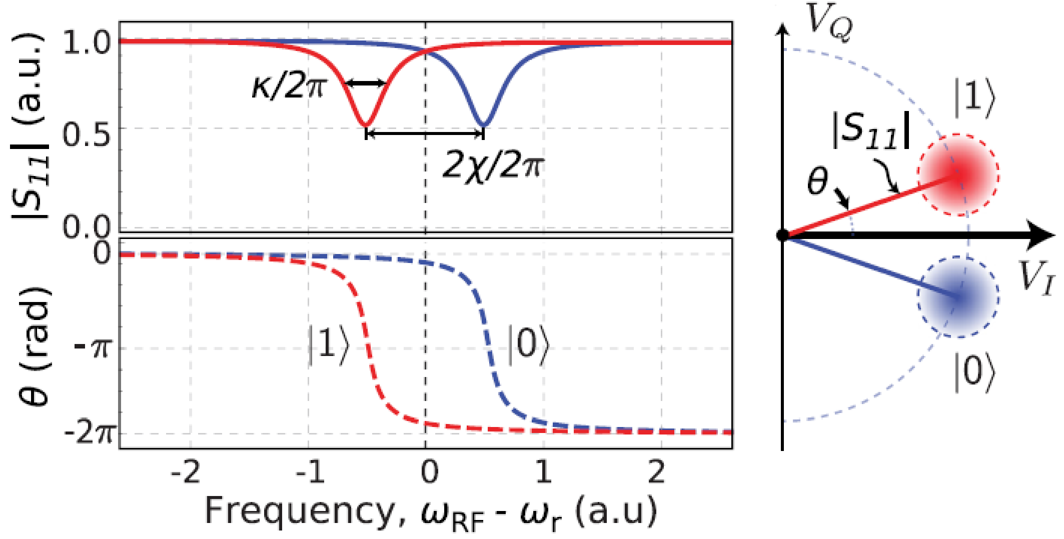
+ Many more

- Take advantage of Entanglement, Superposition, and Interference of Microscope particles
- Quantum processors need to work at tens of mK to several Kelvin temperature
- Qubits are controlled and readout at RF/microwave frequency.
- Cryogenic electronics is attracting more and more attention.

Background

❑ Superconducting Qubit Dispersive Readout





Krantz, Philip, et al. APR, 6.2,2019

- Up-converting chain generates probing signal
- Readout chain performs the demodulation of the reflected/transmitted signal
- I/Q demodulation similar as which in a wireless communication system.
- Room temperature & Cryogenic (Bi)CMOS solution both need cryogenic LNA.
- With JPA may alleviate the 4 K LNA NF requirement, but design a broadband & high gain JPA is still challenging.

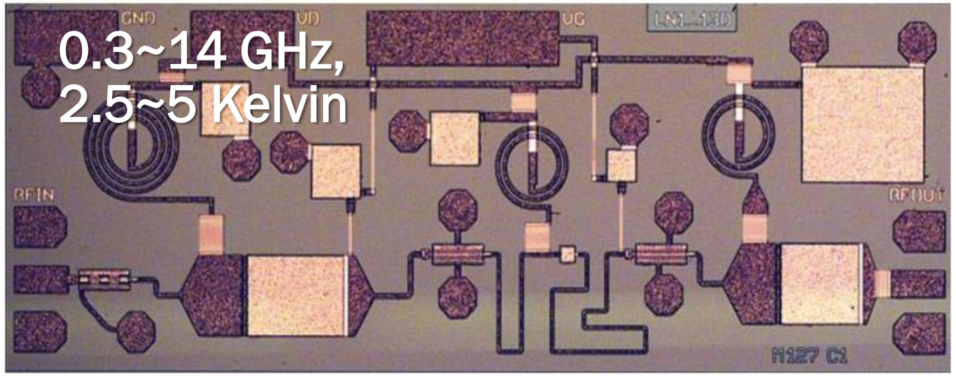
Prior Art

❑ Technologies for Cryogenic Circuit Designs

Technology	Lowest operating temperature	Limit by	Characteristics
Si BJT	100 K	Low Gain	
Ge BJT	20 K	Carrier freeze out	
Si JFET	40 K	Carrier freeze out	
SiGe HBT	70 mK[1]		Low flicker noise/medium noise
InP	<4 K		Extremely low noise/low reliability
GaN	<4 K		High linearity/high power consumption
CMOS	40 mK	Kink effect for>180nm tech.	High integration/high noise
GaAs	<4 K		Low noise/Medium power consumption

Prior Art

- **Cryogenic InP LNA**



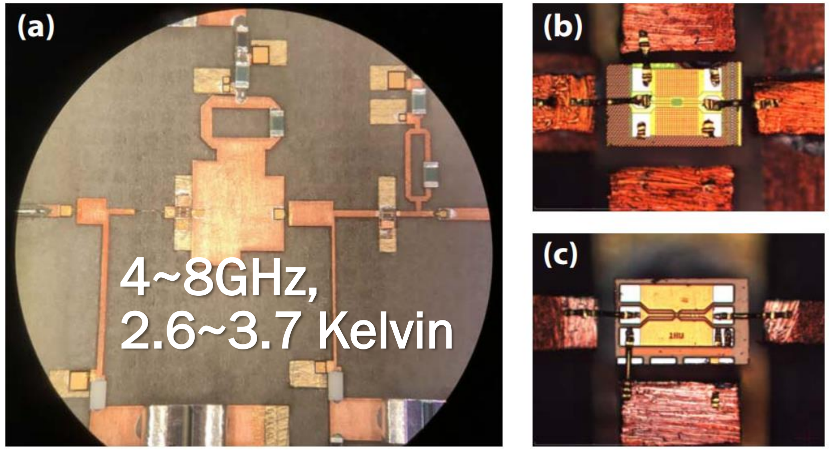
E. Cha, TMTT, 60(11),2018

- Sub<2 K ENT can be achieved.
- Low yield leads to very expensive.
- Cryogenic InP LNA is is the main products in the market.

- **Cryogenic SiGe HBT LNA**

- CLNA designed on standard HBT process can achieve ~5 K ENT.
- Doping profiles of B and E and the Ge profile of the SiGe layer can be modified to achieve <3 K ENT.
- 1 mW~10 mW.

W. Wong, 2020 IEEE/MTT-S IMS.



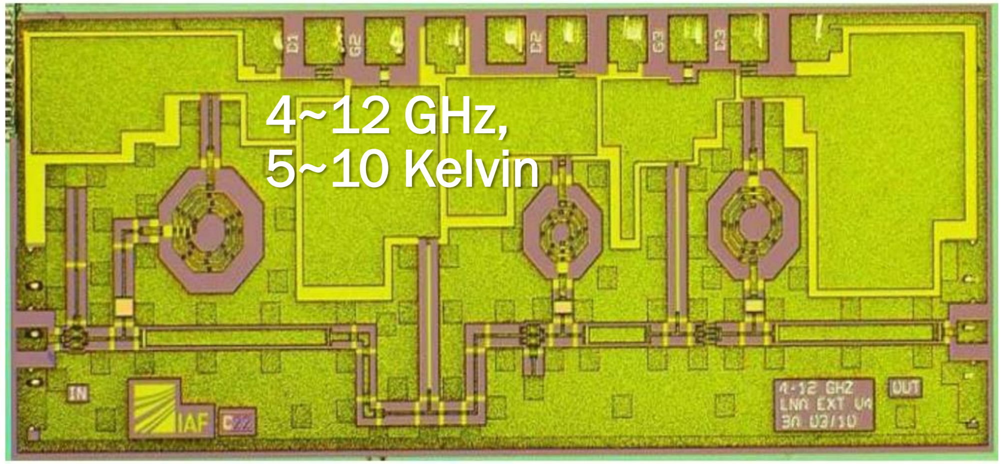
Prior Art

- **Cryogenic CMOS LNA**
  - Can be integrated with other mixed/ digital signal blocks.
  - ~4 K ENT can be achieved at sub-2 GHz applications.
  - >10 K ENT for C-band applications.
  - High power consumption ~ tens of mW: self-heating
  - High yield.

A. Sheldon, IEEE MWCL, 32(11), 2022.

- **Cryogenic GaAs LNA**
  - Often realized by GaAs MMIC.
  - GaAs mHEMT can achieve both low NT and low power.
  - GaAs pHEMT needs tens of Mw power to obtain several Kelvin ENT.

B. Abelán, TMTT, 60(12), 2012

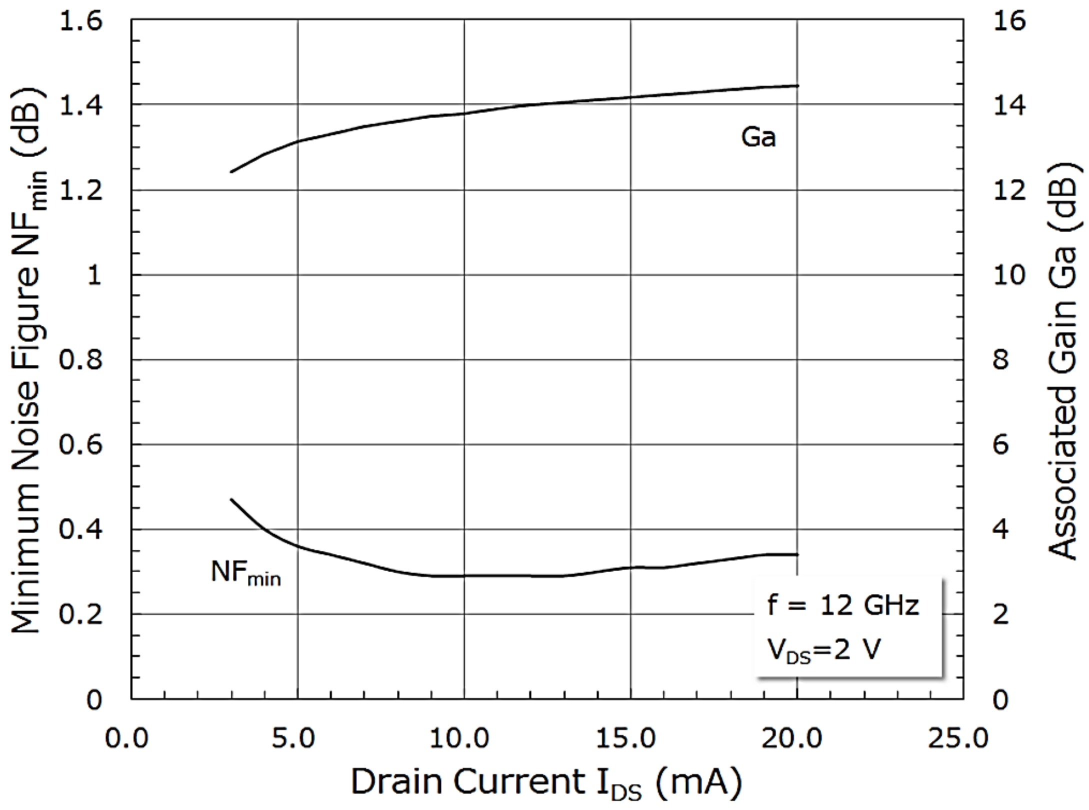


In this work, we will implemented CLNA by discrete GaAs pHEMT devices.

Specifications

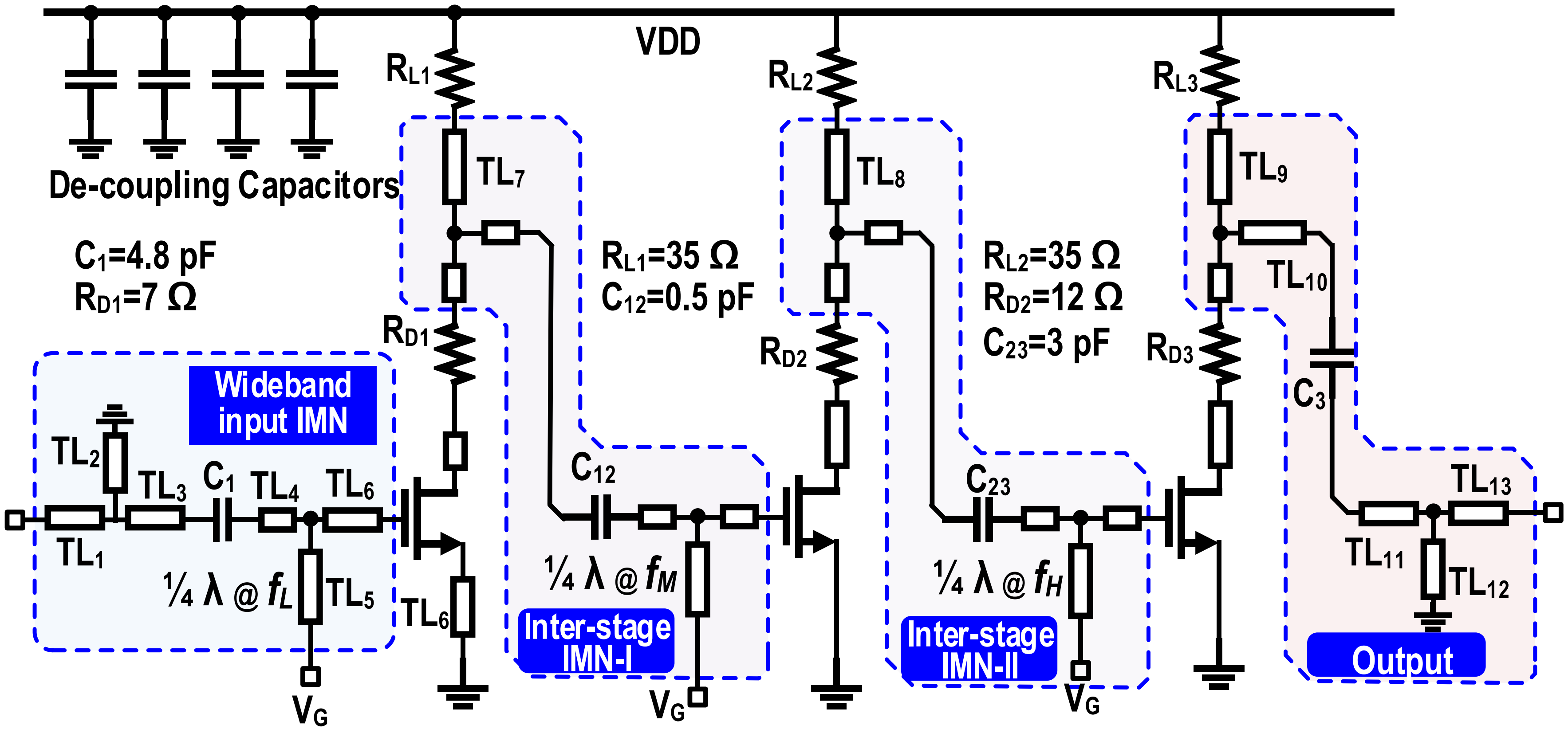
- Specification of LNA for Dispersive superconducting qubits
  - Frequency: about 4~8 GHz.
  - Input return loss: >10 dB. (~8 dB can be acceptable due to the circulator.
  - Output return loss: >10 dB.
  - Gain: >30 dB.
  - Linearity: not importance for single qubit readout. When FDMA readout is applied, OIP3 need to be seriously considered.
  - Noise Figure (Equivalent noise temperature): ~5 Kelvin.

GaAs Device



- The discrete GaAs HEMTs (CEL3512K2).
  - With 0.3~0.45 dB NF_{min} at frequency 4~8 GHz at room temperature (RT, 300K).
  - Available gain: ~12 dB under (2 V, 10 mA).

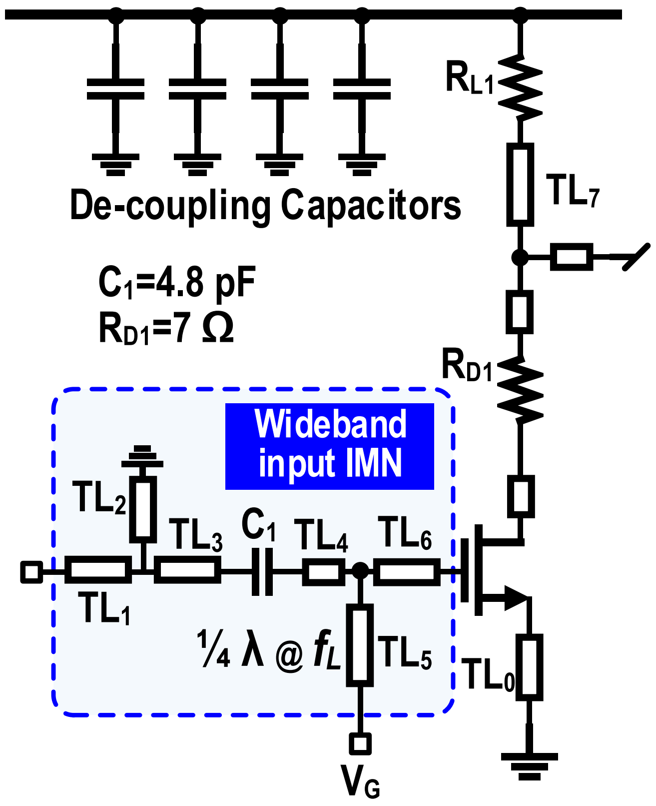
LNA Structure

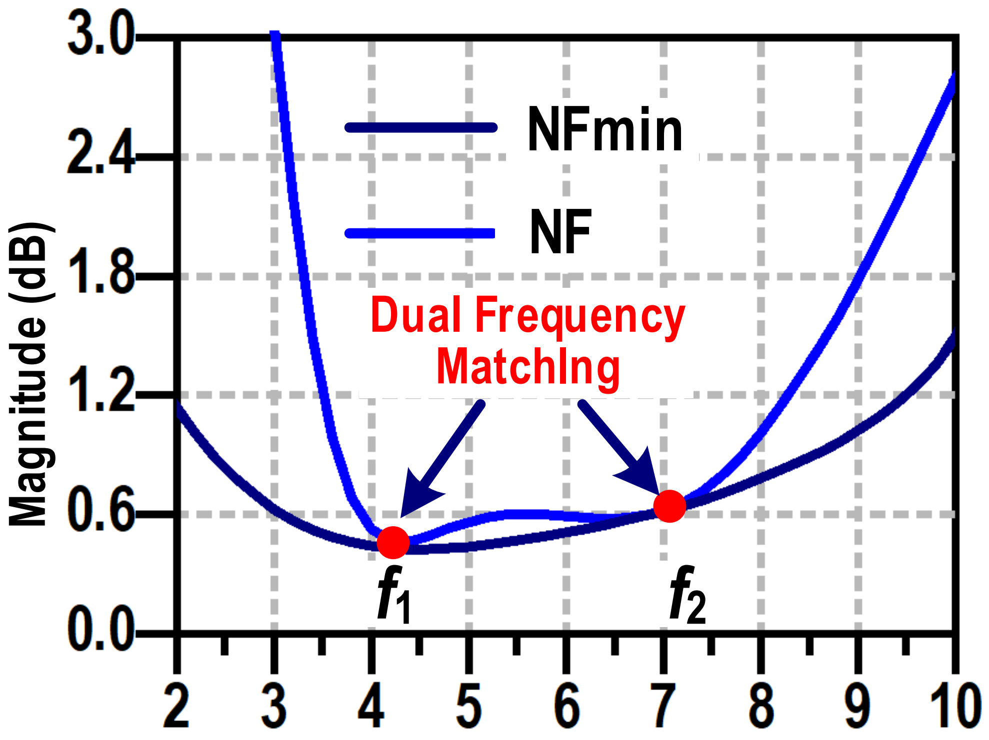


- The LNA consists of three stages: the 1st stage is a low-noise stage, the 2nd stage provides sufficient gain, and the 3rd stage increases gain further (>30 dB) while achieving wideband output impedance matching.
- The stage R_{D1}~R_{D3} are applied to stabilize the high gain amplifier.
- R_{L1}~R_{L3} were used to flatten the in-band gain variation.

First Low Noise Stage

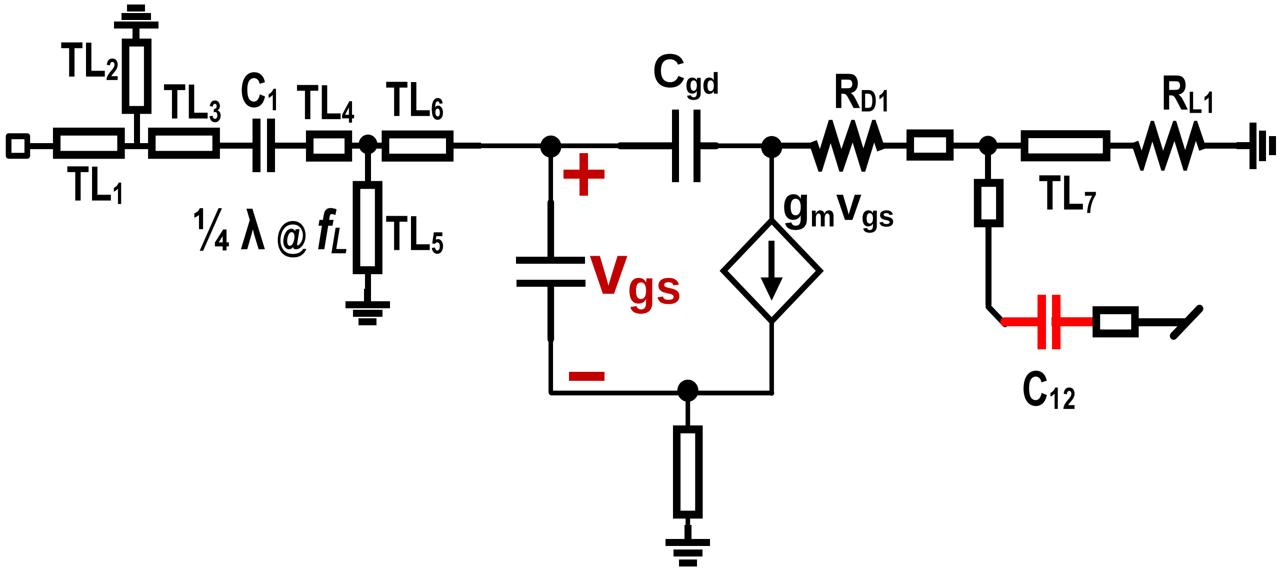
- Input Low Noise Matching Network

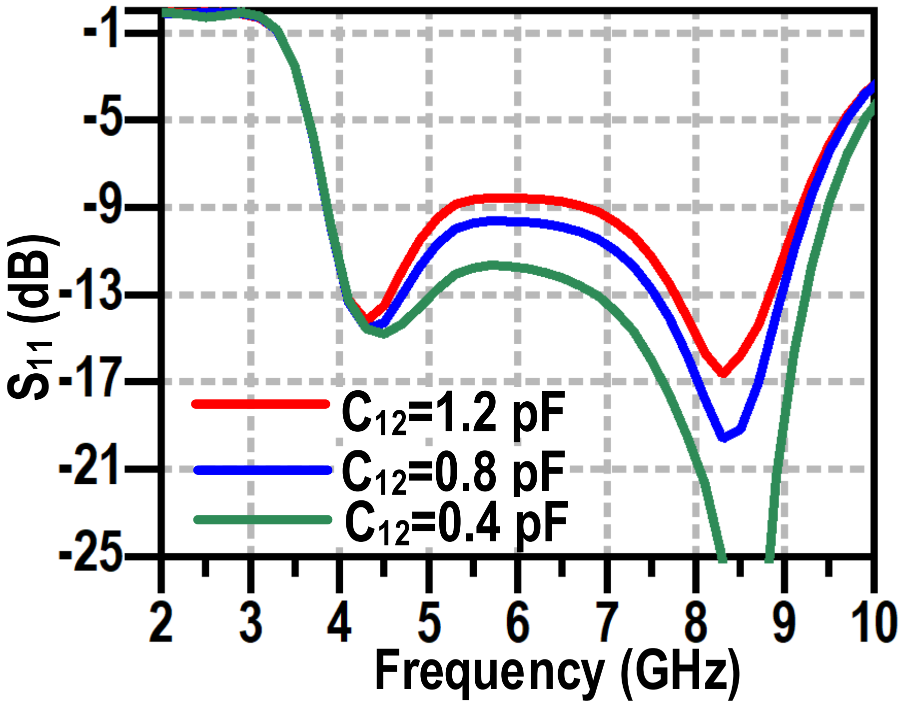




- Six transmission line sections TL_0 at the S of the M1, (TL_1~TL_6) at the gate and were used to achieve dual-frequency optimum noise impedance
- The biasing condition of the three stage are set the same to save cryogenic wire resource

Optimization of Input RL



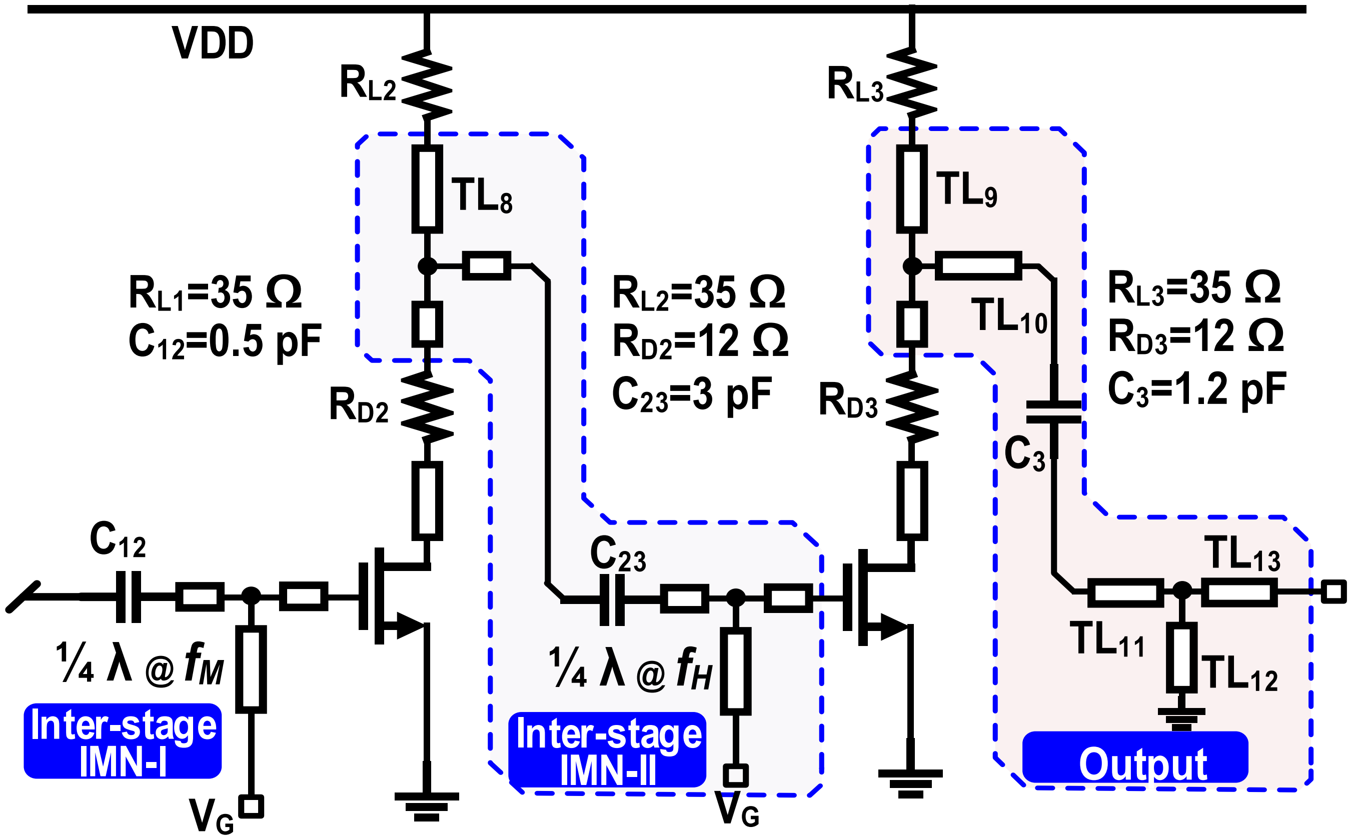


- The elements in the drain of M_1 can be used to optimize the RL due to C_{gd}

$$Z_{IN}=f\ [IMN, Z_L]$$

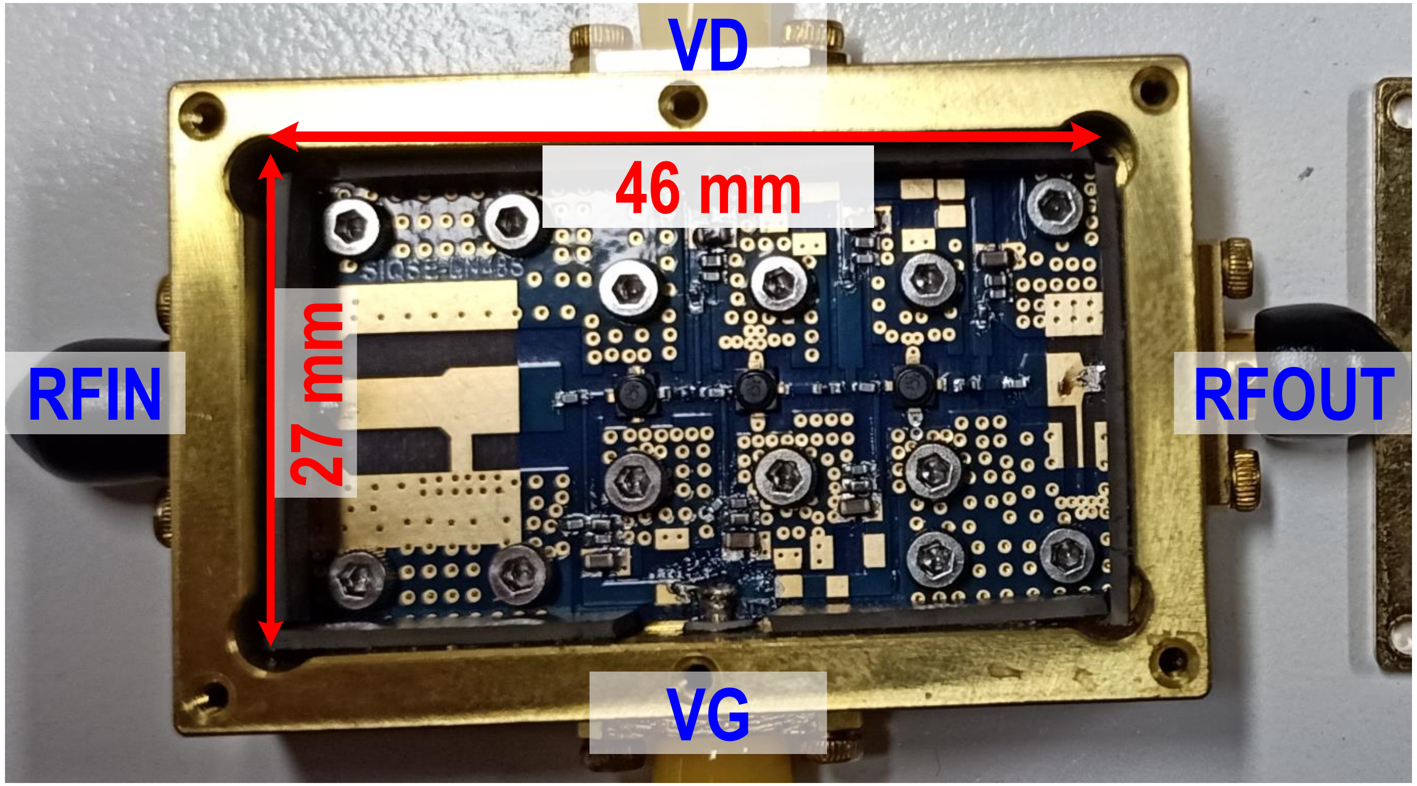
- IMN was applied to achieve optimum noise matching.
- Z_L can adjust the S_{11} while without (or only slightly) influencing on NF.

2nd and 3rd Stages



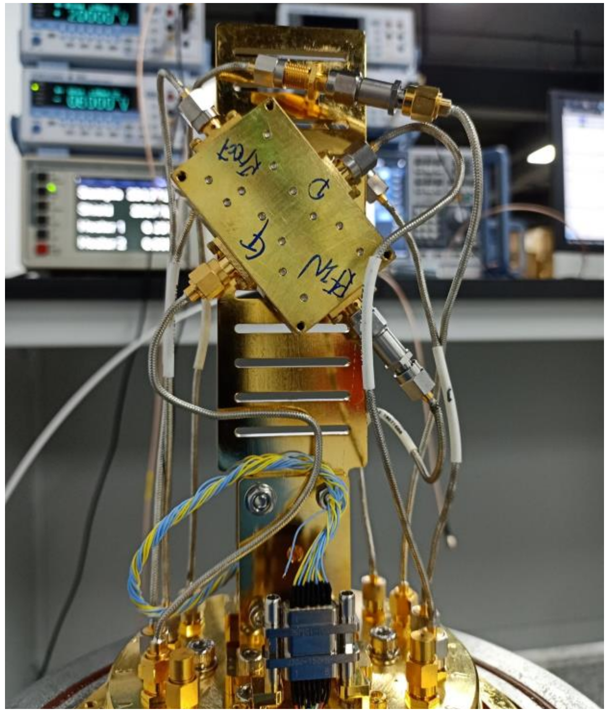
- The inter-stage IMNs were implemented by drain and gate biasing elements and the DC-block capacitors.
- The biasing condition of the 2nd & 3rd stages are set same as 1st stage to save cryogenic wire resource.

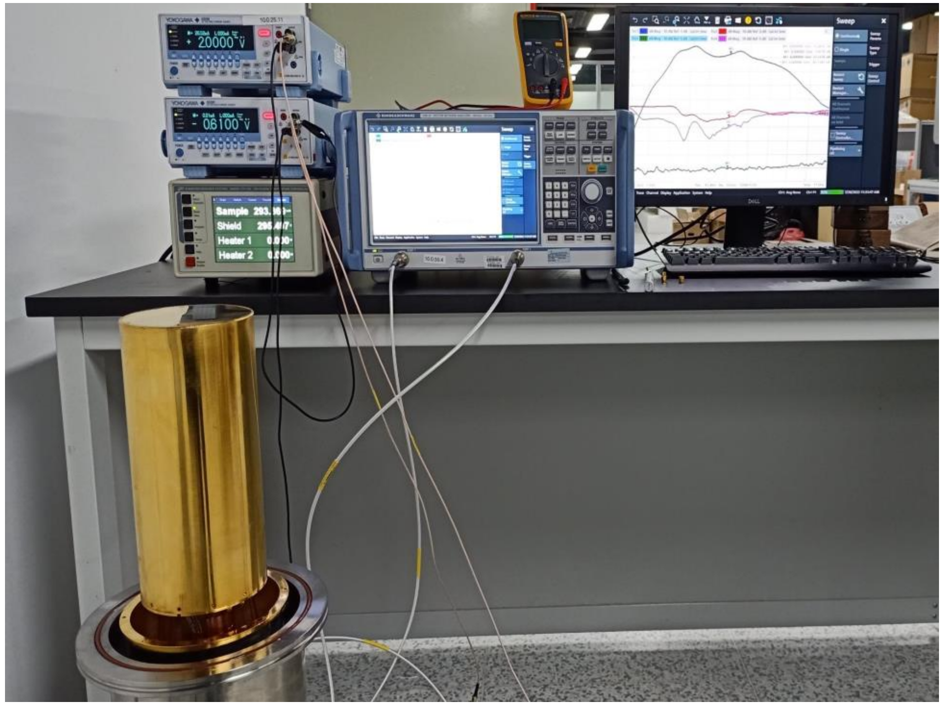
Implementation



- Rogers 5880 with the minimum thickness (0.254 mm).
- Dielectric constant (ε_r) at CT decreases <6% from its RT value (2.2).
- PCB is around 27 mm×46 mm and is installed in a bronze box.
- The non-conductive silicone absorbers are used to avoid cavity effect and the self-excited oscillation.

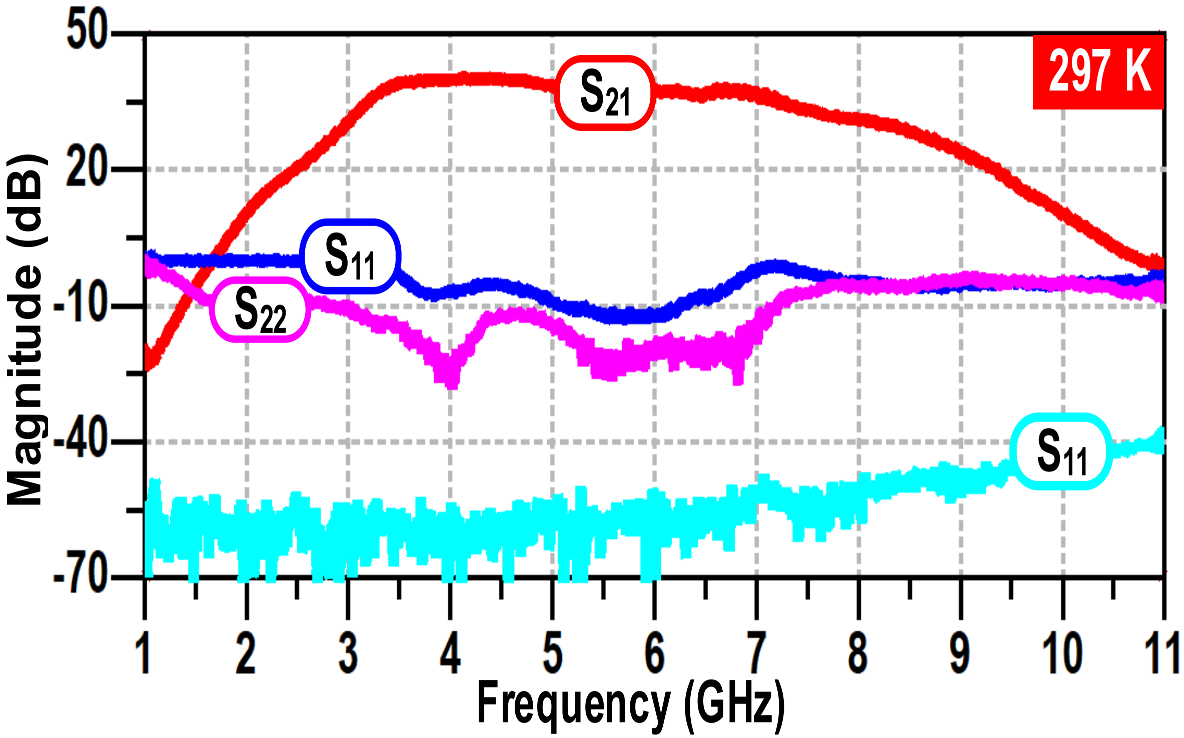
Measurements Setups

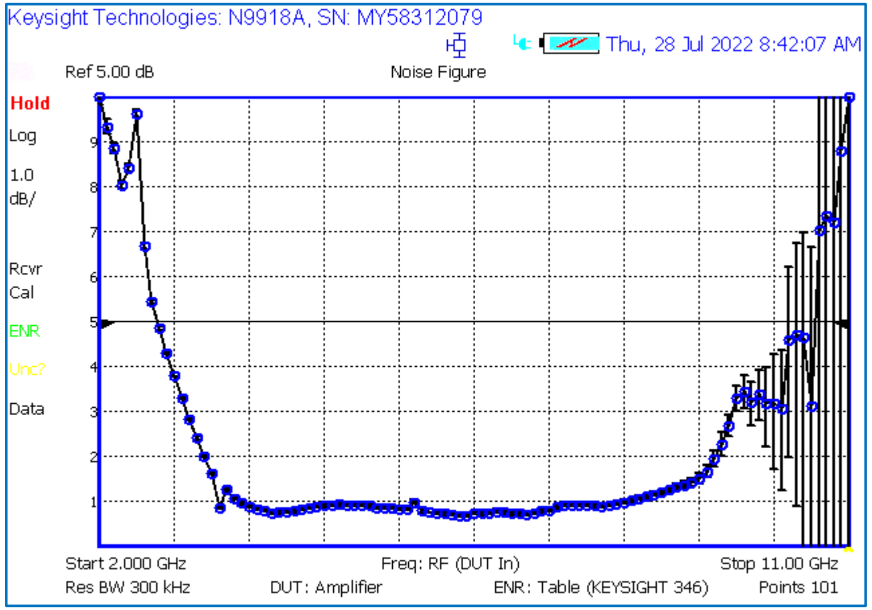




- The LNAs are fixed in a 4-Kelvin cryostat for cryogenic characterization.
- S-parameters: Rohde & Schwarz VNA (ZNB 20).
- NF: Keysight FieldFox N9918A with the NF measurement option.

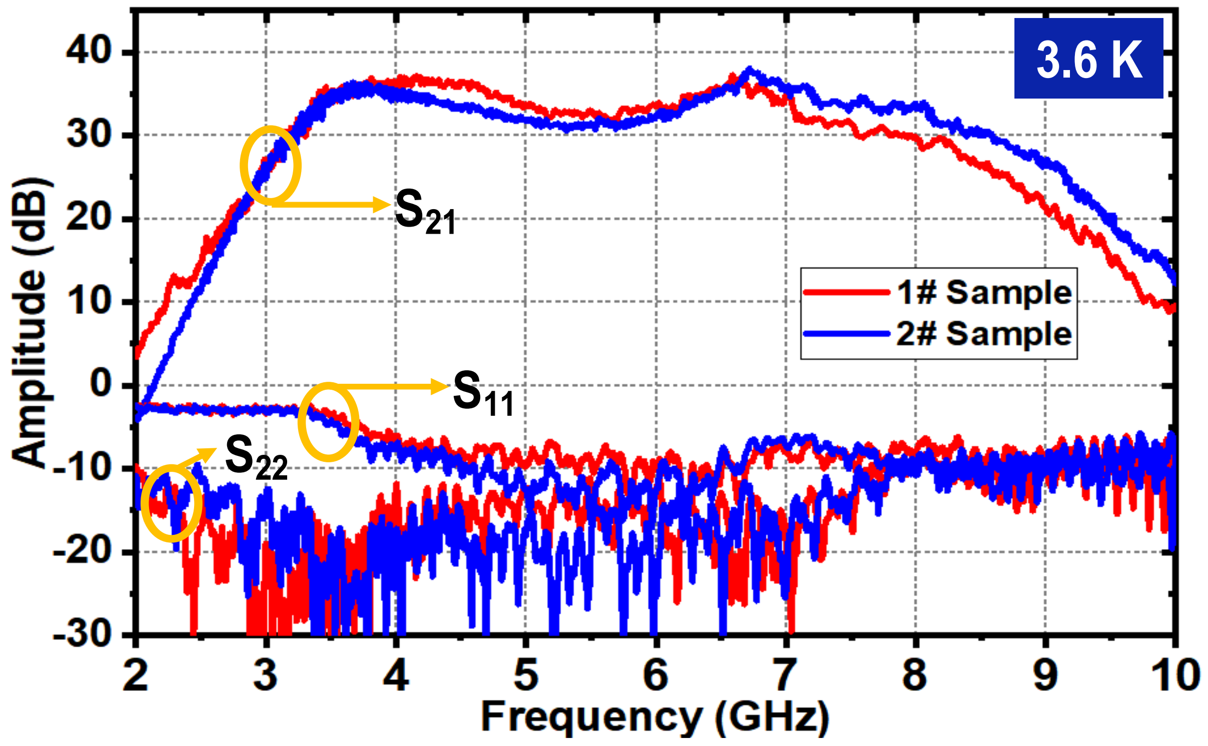
RT S-parameters & NF





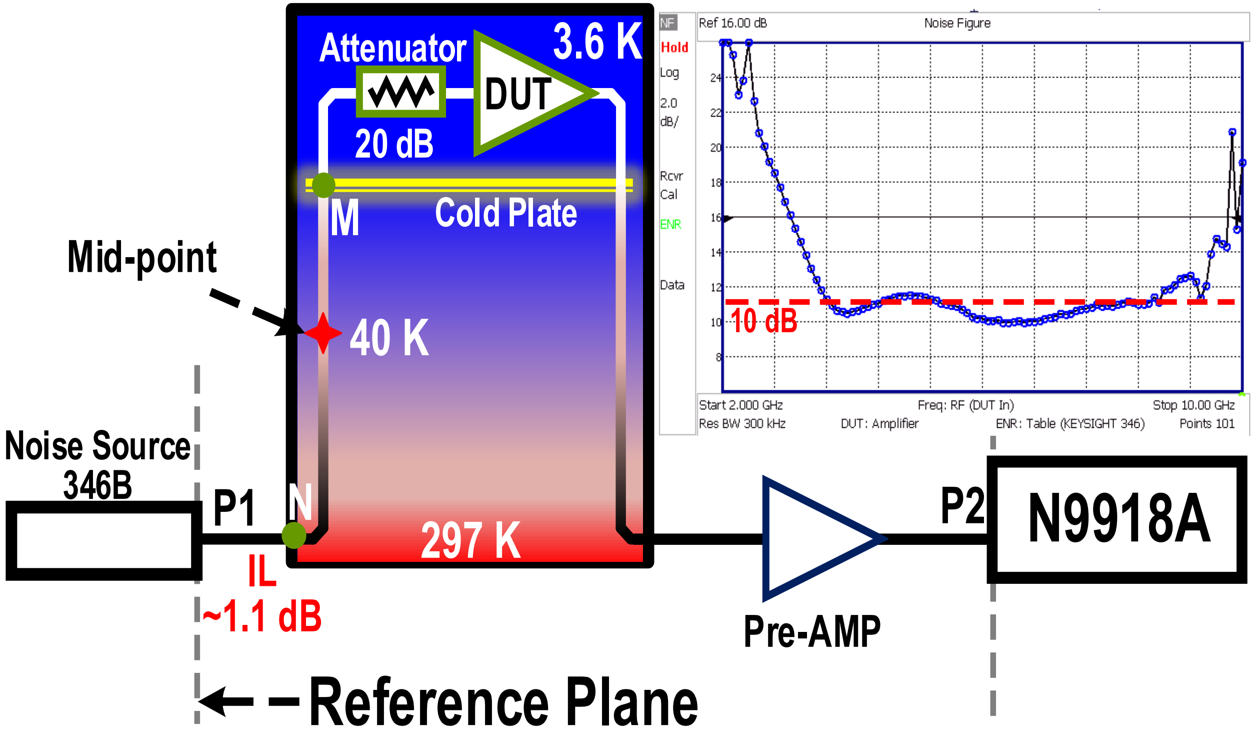
- Room temperature biasing conditons: VDD=2 V, I_D=27.6 mA (V_G~-0.61 V).
- The gain at RT is 36±2.5 dB in ~3~7.5 GHz
- The S_{11} is <-7 dB and S_{22} is<-10 dB.
- NF<1 dB with minimum ~0.75 dB.

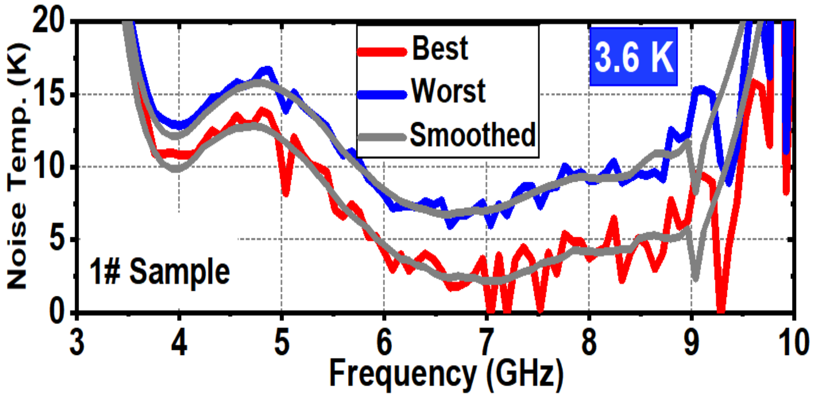
CT S-parameters

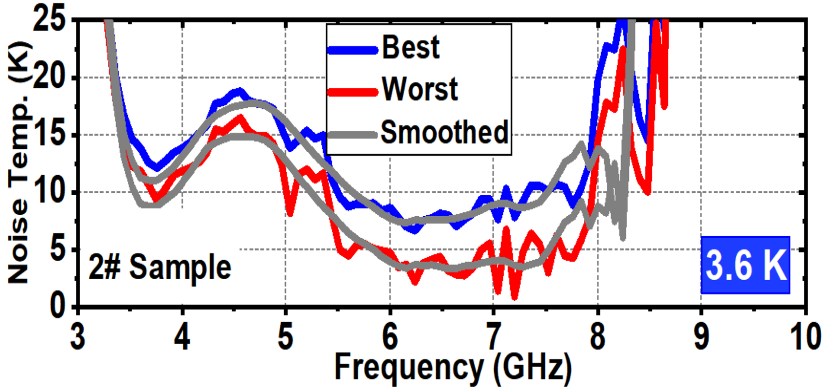


- For two samples (1# and 2#) were characterized.
- .The LNA consumes a 9.5 mA current under 2 V VDD of at CT
- Gain >30 dB in 3.5 ~7.5 GHz.
- In good agreement from sample to sample.

CT NF (Equivalent Noise Temperature)



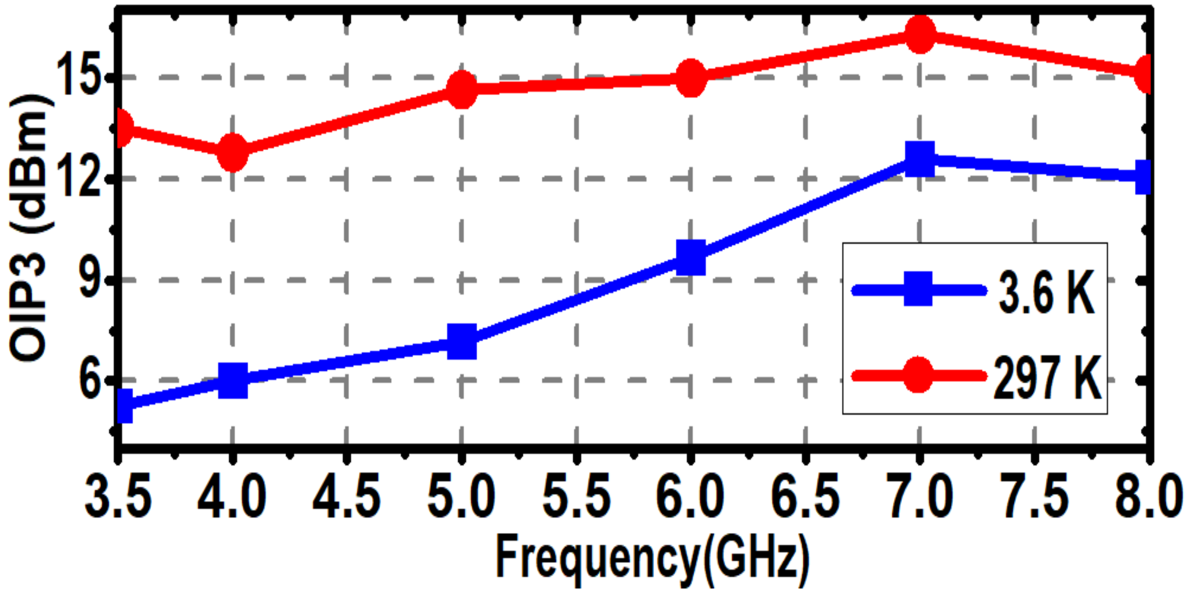




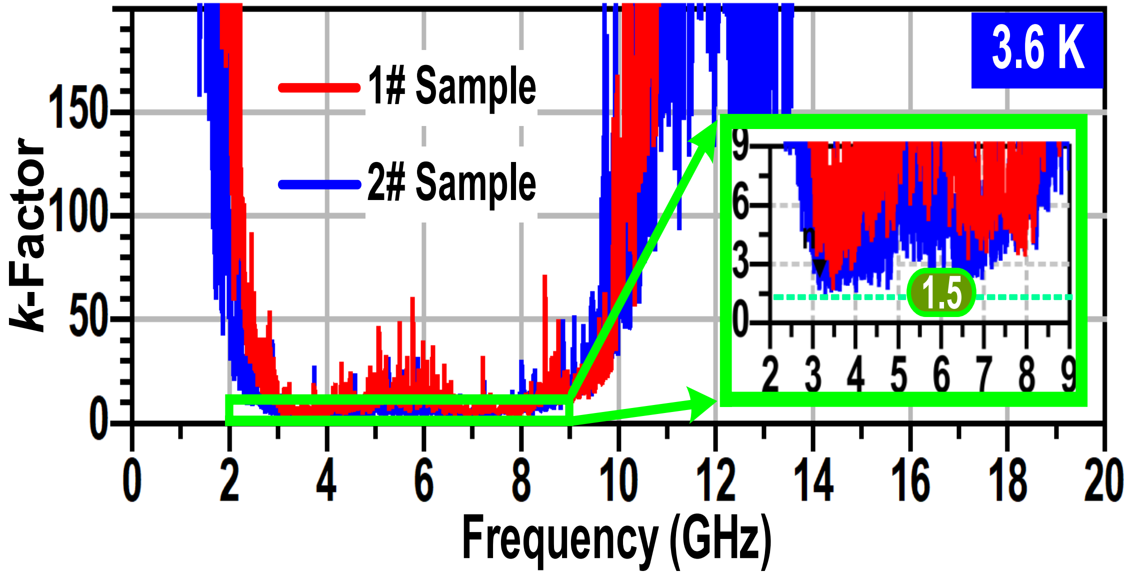
- The NF at CT is measured using the cold attenuator method.
- The cold/hot noise sources were provided by the Keysight 346B.
- A 20 dB coaxial attenuator was used for thermal isolation.
- The influence of the test fixtures (cables, attenuator, and adapters) is de-embedded.
- The LNA shows ~5 K equivalent NT at 6~7 GHz

OIP3 and Stability Factor

- OIP3 at CT and RT

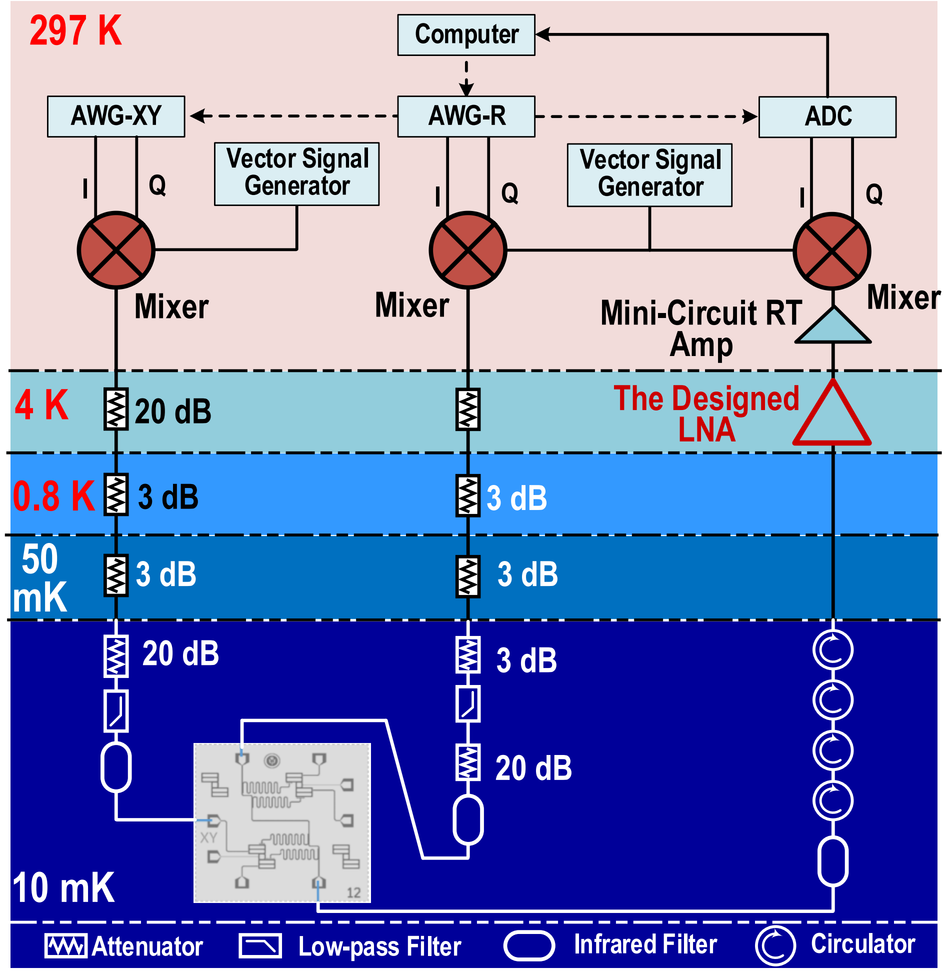


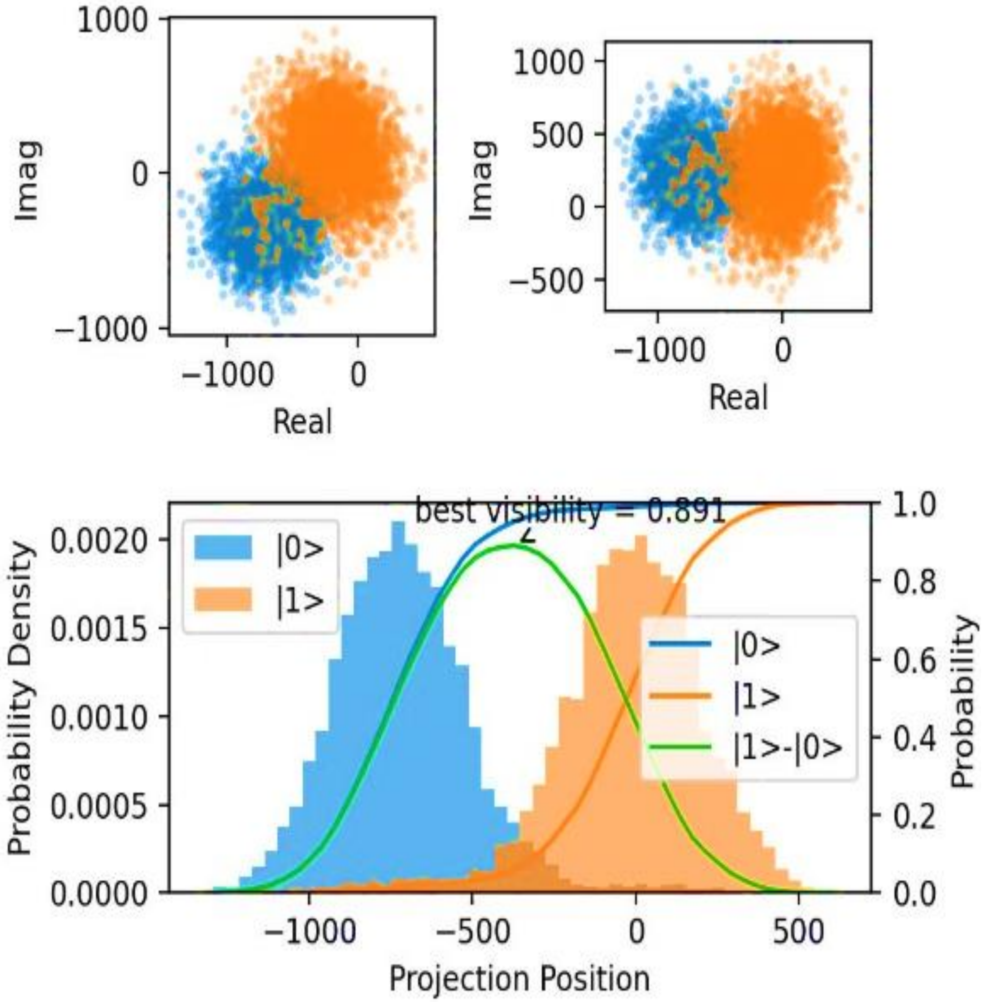
- *k*-factor at CT and RT



- The OIP3 was tested using two tones with 20 MHz offset frequency.
- The linearity degraded ~6 dB at CT comparted with RT due to the which is the increment of the I-V threshold slope.
- The LNAs' k-factors are > 1.5 in the operating band indicating the stability of the LNAs.

Qubit Measurement Using the LNA





- The LNA module was installed on a 4 K plate of BlueForce DR.
- We got a best visibility of 0.891 for distinguishing states |0> and |1>,

Conclusion

- An cryogenic LNA is necessary no matter RT quantum processor controller solution or the emerging cryogenic CMOS controller.
- An LNA operating at 3.6 K was designed and implemented.
- The LNA has an average gain of 32 dB and a minimum equivalent NT 5 K in the frequency range of 3.5 to 7.5 GHz.
- This work demonstrates that discrete GaAs devices can be used to achieve cryogenic LNA for transmons qubit readout.