Abstract—Whether it is for 5G applications, with the demand of data rate increase, for THz imaging, or other applications, there is an increasing need for millimeter-wave technologies. In particular, novel materials more reliable and more stable at high frequencies, are of strong interest. In this context, the use of carbon nanotube (CNT) based bumps to replace existing materials for interconnects, is not unheard of. However, in this article, demonstration of a successful experimental CNT flip chip device in the W band (75GHz-110GHz) is done. This new test structure is based on a dedicated CNT transfer process, which is compatible with CMOS technologies, due to process temperatures that are kept below 220°C.

Keywords—RF nanotechnology, Interconnects, Carbon nanotubes, Electronics packaging.

I. INTRODUCTION

As it is well known in electronics, the increase of the operating frequency leads to the size reduction of the microwave circuits. As described in [1], this size reduction can induce high current densities in classical metallic interconnects. And, for high current densities, typically higher than 10⁶ A/m², electromigration can appear in such interconnects. This phenomenon, due to the intrinsic properties of the metals used [2], can also increase the interconnect delay [3]. Because a single Carbon nanotube (CNT) can support currents up to 10⁹ A/cm² [4], has a long mean free path and high thermal conductivity, CNT bumps seem like good candidates for next generation interconnects.

CNT bumps have already been studied by different groups as potential interconnects [5-8]. Soga et al. [5] have demonstrated the good mechanical properties and low bundle resistance for a 100μm diameter bump. CNT bumps for practical applications in high-power amplifier have been shown in [6]. And, Hermann et al. [7] have tested over 2000 temperature cycles CNT flip-chip interconnects, and have found them reliable.

In this article, we propose the fabrication and the characterisation of a test structure based on a CNT bumps flip-chip bounding in the W band (75GHz-110GHz). To our knowledge, that has never been done before at frequencies higher than 40 GHz [9]. Furthermore, the fabrication process that we developed is new and compatible with CMOS technology. It is easily transposable to other CNT applications such as EM shielding [10] or waveguide [11].

The first section of this article, presents electromagnetic (EM) simulations of the test structure using an equivalent CNT model implemented in HFSS. Then we describe the fabrication process. In the last section, we present the measurements in the W band and we give comments according to the theoretical results.

II. EM MODELING

A. Interconnects design

The test structure that we consider in this work, is composed of a coplanar CPW line flip-chip bounded on two input and output (I/O) CPW access lines, through CNT bumps. All the CPW lines are considered on a silicon substrate. The test structure is described in Fig. 1.

![Fig. 1. Flip-chip design: (a) isometric view; (b) top view](image-url)
large lateral dimensions of the bumps we need to design (I/O) tappers in order to connect the bumps to the 50 Ohms CPW lines. Up to now, we are obliged to consider bumps with large lateral size because of the youth of the transfer process and its current attainable resolution.

<table>
<thead>
<tr>
<th>Dimensions/Structures</th>
<th>Structure 1: 100µm wide bump</th>
<th>Structure 2: 200µm wide bump</th>
</tr>
</thead>
<tbody>
<tr>
<td>W (µm)</td>
<td>75</td>
<td>75</td>
</tr>
<tr>
<td>G (µm)</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>W2 (µm)</td>
<td>110</td>
<td>210</td>
</tr>
<tr>
<td>G2 (µm)</td>
<td>35</td>
<td>50</td>
</tr>
<tr>
<td>Height of the bump (µm)</td>
<td>100</td>
<td>200</td>
</tr>
</tbody>
</table>

**Table 1. Main dimensions of structures 1 and 2**

**B. Full wave EM simulation - CNT bulk model**

In this work, we use a bulk material model equivalent to the vertically aligned CNT forest. This model is described in [12]. This equivalent bulk material model is deduced considering the complex surface conductivity of a metallic single-walled carbon nanotube. Its conductivity is complex and anisotropic (equal to zero in the directions perpendicular to the CNTs), it is written below:

\[
\sum = \begin{bmatrix}
0 & 0 & 0 \\
0 & 0 & 0 \\
0 & 0 & \sigma_{axial}
\end{bmatrix}
\text{with, } \sigma_{axial} = \frac{8e^2v_F}{h(\nu+\omega)}D_{NT}, \tag{1}
\]

where:

- \(\omega\) is the angular frequency
- \(e \approx 1.602 \times 10^{-19}\) C is the elementary charge
- \(h \approx 6.626 \times 10^{-34}\) J.s is the Plank constant
- \(\nu = \tau^{-1}\) is the relaxation frequency
- \(v_F\) is the Fermi velocity in CNT
- \(D_{NT}\) is the density of CNTs in the forest.

The conductivity at 90 GHz, for a density of 10^{15} CNTs/m², is equal to 2.3*10^5 S/m. The equivalent material is implemented in the EM modelling software Ansys HFSS. The results of the three dimensional EM simulations are presented next.

**C. Simulation results**

The 3D EM simulations are done between 80 and 110 GHz. For both structures, two types of simulations are made, one in which the bumps are in gold with a taken bulk conductivity of 4.1*10^7 S/m and one in which the bumps are in CNTs, described by the model from II-B.

Simulations of structure 1 (Fig. 2) show losses in I/O transmission between -1 and -2dB with a I/O reflection parameter kept below -15dB. We can see that the structure 1 with CNT bumps has more losses than the same structure 1 with gold bumps, and less adaptation. However, the difference is not significant, as it is of only 0.1dB in transmission and only 1dB in reflection. Simulations of structure 2 (Fig. 3) show I/O transmission losses between -3dB and -5dB up to 105GHz. The structure 2 has higher I/O losses than structure 1, because wider bumps (200µmx200µm) are considered. And in that case, it is difficult to obtain a good I/O matching whether it is with CNT or gold bumps.

Moreover, we can notice that the difference of performances between CNT and gold bumps is less compelling for structure 2 than for structure 1. This is due to the fact that structure 1 has a finer matching, which means the difference of impedance between the two types of bump will have more impact on the global transmission.
III. FABRICATION

A. Fabrication of the CPW lines

The CPW lines (I/O accesses and the bounded CPW line), are fabricated on a 500µm thick high resistivity silicon substrate. The fabrication follows a classical clean room microelectronic lift-off process. Negative photoresist is used and E-beam evaporation, with a layer of Ti (10nm) and a layer of Au (1um).

B. CNT growth

CNTs are grown separately using classical thermal chemical vapour deposition process [13], with a Blackmagic AIXTRON PECVD process. At the end of the process, we obtain a dense CNT forest (between 10^{13} and 10^{15} CNTs/m^2 [14]) with a height of 250 micrometres.

C. Transfer process

We first proceed to transfer the separately grown CNTs on the I/O CPW lines on the substrate carrier (bottom part of our device). To do so, we deposit by evaporation 100nm of gold on top of our grown CNT forest, and then proceed to deposit solder by classical lithography process on the I/O lines where we want to transfer the bumps. This way, we can obtain the bumps of the device after soldering of the CNTs with the deposited solder, by heating at the proper temperature. The next step consists of covering the bumps with a 1µm thick Au cap. This is made using a shadow mask and an evaporation process. Solder is then deposited on the flipped CPW line. Then, the bonded CPW line is aligned with the bumps and put on top, via Flip-Chip (FINEPLACER lambda from Finetech GmbH & Co) and heated around 200°C to get a soldering of the bounded line with the CNT bumps. The process is detailed in Fig.4.

Fig. 4. Schematic of the step by step fabrication process of the Flip-Chip

An SEM picture of the transferred CNT bumps is given in Fig. 5. As we can see, due to transfer, there is a slight decrease in height, from 250µm to 185µm. Because we know there is a decrease in height due to the applied pressure, we previously grow the CNT to a bigger height accordingly.

IV. MEASUREMENTS

A. Measurement tools

The measurements are made using:
- a PNAX N5247A Vectorial Network Analyzer from Keysight
- a PM8 probe station for the 70-110GHz band from Cascade Microtech
- infinity probes 110-S-GSG-100BT from Cascade Microtech

B. Millimetre Wave Measurements

As explained previously, because of the technological constraints of the CNT transfer process the structure 2 (with the larger size bumps) is fabricated.

For the first time, a CNT based flip-chip bounded test structure has been measured in the W band. It presents S-parameters around -5dB in transmission and below -10dB in reflection. The results are shown in Fig.6. After checking the dimensions of the fabricated test structure, we observe that the distance between the substrate carrier and the top substrate is lower than 200um. Indeed, during the flip-chip process of the top substrate, due to the applied pressure the CNTs are laid down (below 100um). Back-simulations are done in order to estimate the equivalent electrical length of the CNTs. We notice in Fig.6 a good agreement between the experimental and theoretical results for bumps of a 100um height.

Fig. 5. SEM picture of the transferred CNT bumps on the bottom part of the device

Fig. 6. Comparison between the S-parameters measurements of the prototype and the EM simulations
The measured S-parameters of the CPW line (top substrate before being bonded) are shown in Fig. 7. From these measurements we can estimate the losses induced by the CNT bumps.

![Comparison between the S-parameters measurements of the prototype and the EM simulations](image)

Fig. 7. Comparison between the S-parameters measurements of the prototype and the EM simulations.

The measured losses in dB/mm of the bounded line before being bounded that are between -0.55dB/mm and -1.22 dB/mm depending on the frequency. From these measurements, we estimate the losses due to the I/O CPW lines and to the bounded line (the whole structure minus the CNT interconnects). Indeed, all the lines are made using exactly the same materials and process. Thus, by considering a length of 2.5 mm in total (see Fig. 1b), the transmission losses of the (I/O and bounded) lines are estimated to be equal to, at least, -1.4dB to -3dB, in the 75-103GHz band. This implies that the losses due to one bump are between -0.8dB and -1dB (total losses of -3dB and -5dB at 75GHz and 103GHz, respectively). Even though they are high, they are close to the simulated ones (see Fig.3) that would be induced by gold bumps of the same dimensions.

From these measurements, we can also argue that the losses at higher frequencies are not only due to the CNT bumps, but also to the behaviour of the lines (and in particular their discontinuities (introduced for the matching)) at higher frequencies.

At last, a dedicated CNT transfer process used for the interconnects’ fabrication is developed with success. This process is fully compatible with a CMOS process. Currently this technology is still being improved by investigating the following points: reduce the pressure during the flip-chip process (or add spacers) to avoid the reduction of the height of the bumps due to the bending of the CNTs, increase the resolution of the process in order to make interconnects down to the 10um size and increase the CNT density to have even higher performances.

VI. CONCLUSION

To our knowledge, this is the first time that a flip-chip bounded structure composed of CNT based interconnect is successfully measured in the W band. These measurements permit to validate several points:

As measured, the transmission losses of the CNT bumps are about -1.6dB to -2dB in the W band. This result confirm that CNT bump can provide good electrical performances and that is very encouraging for future applications.

Theoretical and experimental results are in good agreement. That contributes to validate the bulk CNT model. In addition, we will proceed to EM back simulations based on the verification of all the dimensions of the fabricated test structure. These EM back-simulations will permit to better understand the behaviour of the test structure and to improve the bulk CNT model.

REFERENCES


