A 1 mW Cryogenic LNA Exploiting Optimized SiGe HBTs to Achieve an Average Noise Temperature of 3.2 K from 4–8 GHz

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Abstract — Low-power cryogenic LNAs are required for readout of fault-tolerant quantum processors, which may have a million or more qubits. While InP HEMT LNAs are used for qubit readout today, SiGe HBTs are attractive for future systems due to their excellent noise and potential for low power operation. Here, we optimize a high performance SiGe technology to further improve its cryogenic noise properties. After extracting simulation models from standard and optimized HBT test structures, we employ these transistors in cryogenic LNAs and show that the cryogenic noise achieved with the optimized transistor is significantly better than that achieved using the standard device. Moreover, while dissipating just 1 mW, the amplifier using the optimized HBT had an average measured $T_e$ of 3.2 K from 4–8 GHz, which is more than 2× better than the previous state-of-the-art SiGe LNA operating in this band.

Keywords — cryogenic low noise amplifier, silicon germanium heterojunction bipolar transistor, quantum computing readout.

I. INTRODUCTION

Over the past decade, there have been significant advances in the field of quantum computing, culminating in the recent demonstration of a 54 qubit quantum processor with sufficiently low error rates to enable a computation that is impractical for the current best supercomputers [1]. However, despite this progress, quantum computing technology is still far from what is required to operate reliably in the unavoidable presence of noise. For this, quantum error correction codes must be implemented and these algorithms carry an overhead of a thousand or more physical qubits per error-protected logical qubit [2]. Scaling quantum computing technology to the million qubit level, as needed for fault-tolerant quantum computing, demands the implementation of the high performance mixed-signal control and measurement systems that are required to operate a million qubit quantum computer. Several groups are currently investigating circuit solutions to this challenge [3], [4].

Here, we focus on the cryogenic semiconductor LNAs that are required for qubit readout. Today, one cryogenic LNA is required for every 5–10 qubits. Since these devices must have as low of noise as possible, they are almost exclusively implemented using InP HEMT technology, and even the most power efficient of these amplifiers dissipates several milliwatts of dc power [5]. This power must be reduced before considering integrating hundreds of thousands of these devices into a single cryogenic cooling system.

Cryogenic LNAs based upon SiGe HBTs have been shown to operate at power levels in the low hundreds of microwatts [6] and, as such are a very promising candidate for large-scale quantum readout systems. However, to be used in these systems, the amplifiers must operate in the 4–8 GHz frequency regime, and LNA results to date have had significantly higher noise temperature ($T_e$) in this frequency range than their InP HEMT counterparts [7]. However, no effort to optimize the properties of SiGe HBTs specifically for cryogenic noise performance has been previously reported.

Here, we investigate the feasibility of adjusting the fabrication parameters of a SiGe HBT to optimize the cryogenic noise performance. After describing the optimized transistors as well as the standard devices used for comparison, we present the characterization and noise modeling of these devices. We then leverage the optimized transistors to implement an amplifier with an average $T_e$ of 3.2 K from 4–8 GHz. In comparison to an identical amplifier using the standard HBT, this amplifier achieves $\approx 0.74$ K lower $T_e$.

II. TRANSISTOR OPTIMIZATION

We fabricated SiGe HBTs using the IHP SG13G2 130-nm BiCMOS technology. At a current density of 20 mA/μm², the HBTs feature peak room temperature $f_t$ and $f_{max}$ values of 350 and 450 GHz, respectively. The present study utilizes two flavors of these devices. The first group of devices was fabricated in the standard process technology. The second group of devices was fabricated in a process variant that was optimized for reduced noise at cryogenic temperatures. For this purpose, the doping profiles of the base and emitter and the Ge profile of the SiGe layer were modified. The optimization was guided by the basic dependencies of $T_{MIN}$ on dc current gain ($\beta_{DC}$) and transconductance ($g_m$) of the transistor. Based on a description of the transistor by an equivalent-circuit noise model, $T_{MIN}$ can be expressed as [8]

$$T_{MIN} \approx \sqrt{\frac{n_c^2 T_A^2}{\beta_{DC}}} + \frac{2qI_c T_A}{k} \left( \frac{1}{\beta_{DC}} + \frac{f_i^2}{f_t^2} \right),$$

(1)

where $T_A$ is the bath temperature; $n_c = qI_c/(kT_A g_m)$ is the collector current ideality factor; $q$ is the elementary charge; $k$ is Boltzmann’s constant; $R_B$ and $R_E$ are the base and emitter resistances, respectively; and $f_i$ is the unity current...
gain cutoff frequency. High-speed SiGe HBTs are optimized for high \( f_t \) and low \( R_B \) and \( R_E \). This is advantageous for low thermal noise of \( R_B \) and \( R_E \), described by the second term in Eq. (1). At cryogenic temperatures, thermally activated currents vanish and the collector current is dominated by tunneling and becomes independent of temperature \([9], [10]\). In this regime, \( n_c \) is inversely proportional to \( T_A \) and the first term of Eq. (1), which is related to shot noise of the collector current, no longer decreases with \( T_A \). On the other hand, the thermal noise of \( R_B \) and \( R_E \) decreases considerably with cryogenic cooling. In the low-frequency limit, Eq. (1) can be approximated by \([11]\):

\[
T^*_{\text{MIN}} = \frac{qI_C}{k g_m \sqrt{\beta_{\text{DC}}}}. \tag{2}
\]

In accordance with Eq. (2), our transistor optimization for low noise at cryogenic temperatures addressed the realization of high \( \beta_{\text{DC}} \) and high \( g_m \) at these temperatures. The optimized HBT features about five times higher \( I_C \) and \( \beta_{\text{DC}} \) at room temperature due to increased Ge content in the SiGe base layer. The standard HBT and the optimized HBT have similar base sheet resistance values of 2.8 and 2.6 \( \Omega \), respectively.

Measured DC and RF characteristics of the standard and optimized HBTs are compared in Fig. 1. The strongly enhanced \( I_C \) at 7 K for the optimized HBT is also related to the higher Ge content in the base and the resulting reduction of the potential barrier height for electron tunneling. Low base currents at cryogenic temperatures can be realized by minimizing the density of trap states in the base and base-emitter regions, which contribute to the generation of base currents by trap assisted tunneling. The achieved \( \beta_{\text{DC}} \) of the optimized HBT exceeds that of the standard HBT by about 10\( \times \). Measured \( f_t \) and \( f_{\text{max}} \) of the optimized HBT at 7 K (Fig. 1(c)) for low collector current densities show a significant increase at cryogenic temperature. Fig. 1(d) depicts the approximate noise temperature, \( T^*_{\text{MIN}} \), calculated from measured DC characteristics according to Eq. (2) for three devices from each of the two process variants. The lower \( T^*_{\text{MIN}} \) for the optimized HBT results from the enhanced \( \beta_{\text{DC}} \).

III. MODEL EXTRACTION

After measuring the terminal characteristics, we extracted small-signal equivalent noise models \([6]\) for representative devices from each technology. Following the approach described in \([12]\), the small-signal noise models were extracted for a wide range of collector current densities (0.01–20 mA \( \mu \)m\(^2\)). All data were acquired using a commercial cryogenic probe station, which permitted on-wafer measurements at a physical temperature of 7 K. As the transport properties of SiGe HBTs change little below 20 K, these models should be sufficient to predict the noise performance at all temperatures below 20 K.

Next, we used the models to study the noise performance of each of the device variants. The modeled \( T_{\text{MIN}} \) at 5 GHz is shown for each device in Fig. 2(a). As expected, \( T_{\text{MIN}} \) of the optimized transistor was found to be significantly better than that of the standard technology. This is primarily due to a dramatic increase in \( \beta_{\text{DC}} \). For instance, at a bias current of 0.51 mA \( \mu \)m\(^2\), we found that \( \beta_{\text{DC}} \) of the optimized device was over 10\( \times \) larger than that of the standard device (17,000 versus 1,500). Moreover, the general trends are similar to those of Fig. 2, further validating our optimization strategy.
Table 1. Model Parameters at 7 K. Units: Current density–mA/μm², Area–μm², Res.–Ω, µm², Cap.–fF/μm², Transcond.–mS/μm², Delay–ps

<table>
<thead>
<tr>
<th>Process</th>
<th>(J_c)</th>
<th>(R_B)</th>
<th>(R_e)</th>
<th>(R_C)</th>
<th>(C_{CB})</th>
<th>(C_{CS})</th>
<th>(C_{BE})</th>
<th>(\gamma_m)</th>
<th>(\tau)</th>
<th>(\beta)</th>
<th>(\rho_{be})</th>
</tr>
</thead>
<tbody>
<tr>
<td>IHP (SG13G2, Optimized)</td>
<td>0.51</td>
<td>4.56</td>
<td>2.3</td>
<td>2.8</td>
<td>5.2</td>
<td>14.9</td>
<td>4.4</td>
<td>37.1</td>
<td>71.2</td>
<td>0.3</td>
<td>1.7e4</td>
</tr>
<tr>
<td>IHP (SG13G2, Standard)</td>
<td>0.51</td>
<td>4.56</td>
<td>5.9</td>
<td>3.9</td>
<td>4.8</td>
<td>14.1</td>
<td>2.2</td>
<td>46.8</td>
<td>76.7</td>
<td>0.3</td>
<td>1.5e3</td>
</tr>
<tr>
<td>GF BiCMOS 8HP</td>
<td>0.69</td>
<td>2.16</td>
<td>6.5</td>
<td>3.3</td>
<td>1.9</td>
<td>15.3</td>
<td>11.5</td>
<td>94.5</td>
<td>87.9</td>
<td>1.14</td>
<td>3.1e3</td>
</tr>
</tbody>
</table>

The simulated optimum generator impedance of a 4.56-μm² device from each technology at a bias current of 2.5 mA is shown from 4–8 GHz in Fig. 2(b). Both the real and imaginary parts of the optimum generator impedance depend on \(\beta_{DC}\) [8], so it is not surprising that the optimum reflection coefficient is different between the two devices. Nonetheless, it is worth noting that \(\Gamma_{OPT}\) for the optimized device has a higher quality factor than that of the standard device (≈2.5 versus 1.0 at 8 GHz). However this quality factor is still relatively low (especially in comparison to cryo CMOS [13]) and should not cause problems in terms of broadband matching. A summary of model parameters for each device appear in Table 1, along with the parameters of a third HBT from a different process, which was used in a demonstration amplifier described below.

IV. AMPLIFIER DESIGN AND IMPLEMENTATION

A two-stage 4–8 GHz discrete transistor amplifier has been designed and built both to compare the performance of the two HBT variants and also to explore the limits of the optimized HBT technology. A schematic of the amplifier is shown in Fig. 3 and photographs of an assembled device are shown in Fig. 4. The amplifier was designed for nominal performance when a device from the optimized HBT technology with an emitter area of 4.56 μm² is employed as the first-stage transistor. Due to a limited supply of transistors from the two process variants, we used a transistor from a different SiGe HBT technology in the second stage of the amplifier. The size of this transistor was set to 2.16 μm², since this value was readily available. Versions of the amplifier have been built using both standard and optimized HBTs as first-stage transistors to enable comparison.

The amplifier was designed following standard low noise techniques. The transistors were mounted within a pocket of a 200 μm thick RO4003C PCB, with the HBTs attached directly to the OFHC copper chassis using silver epoxy, ensuring an excellent thermal contact. An emitter degeneration inductance of \(\approx 0.18 \text{nH}\), as required to achieve simultaneous impedance and noise matching, was realized using a single bondwire. Solid copper grounding shims were placed in close proximity to the HBT chips to realize this small inductance, despite the 300 μm thickness of the HBT dies (see Fig. 4(b)).

The generator impedance was transformed to present an impedance close to \(\Gamma_{OPT}\) using a simple transmission line transformer network, followed by a 1.7 nH inductor that was realized using a combination of two bondwire inductances (see Figs. 4(a) and 4(b)). DC bias was supplied to the base of the transistor through the shunt line. The inter-stage matching network was designed to flatten the gain while dissipating a minimum amount of power by avoiding the flow of dc current through resistors where possible. The second-stage transistors were mounted similar to the first stage transistors (see Fig. 4(c)). Finally the output matching network was designed as a trade off between \(S_{22}\) and gain flatness.

The amplifier performance was simulated using the models provided in Table 1. For simulation purposes, the bondpads and feed networks have been re-embedded around the transistor models to enable more accurate modeling. From 4–8 GHz, the simulations predicted a gain and noise temperature for the amplifier with the optimized (standard) first-stage HBT of 27–31 (27–31) dB and 2.2–3.2 (3.6–4.9) K, respectively. In both cases, the associated power dissipation was predicted to be approximately 1 mW.

V. RESULTS

The amplifier modules were characterized at a physical temperature of 17 K using a closed-cycle cryostat which can be configured for scattering parameter measurements as well as noise temperature measurements using the cold attenuator method [14]. The noise test-set has been calibrated to an absolute accuracy that is believed to be \(\leq \pm 1\text{ K}\). All measurements were carried out at a dissipation of approximately 1 mW. We have not deembedded several ohms of wiring resistance from this power estimate.

The measured reflection coefficients of the amplifier with the optimized first-stage transistor appear along with simulation results in Figs. 5(a) and 5(b), respectively. As it was not feasible to perform a VNA calibration within the cryogenic system, the reference plane for these measurements was at the cryostat wall, which explains the significant ripple appearing on the experimental results. Nonetheless, the measured results agree well with simulation. The amplifier with the standard input-stage HBT had similar reflection coefficients.

The gain of the amplifiers, measured using the noise test-set, appears in Fig. 6 along with the simulated gain of the amplifier with the optimized first-stage transistor. The RMS
difference between the gain of the two measured amplifiers was just over 0.1 dB from 4–8 GHz. The disagreement in gain flatness between the simulation and measurement is believed to be related to the inter-stage matching network.

Finally, the measured noise performance of the amplifiers is shown in Fig. 7. We found that, in the 4–8 GHz band, the amplifiers with the optimized and standard first stage HBTs displayed average noise temperatures of 3.2 and 3.94 K respectively. While the simulated value for the amplifier with the standard device (3.93 K) agrees very well with measurement, the simulated value for the optimized device (2.45 K) was considerably lower than what was experimentally observed. Further work is required to understand this discrepancy. Nonetheless, in comparison to other state-of-the-art amplifier results (see Table 2), this is an excellent result. In particular, the amplifier with the optimized HBT has well over 2× lower noise than the previous state-of-the-art SiGe LNA, while still dissipating just 1 mW.

VI. CONCLUSION

We have optimized a SiGe HBT for cryogenic noise performance and have shown that its amplifier performance is considerably better than that of the base technology. Using these devices, we have implemented a 1 mW cryogenic LNA with an average noise temperature of 3.2 K from 4–8 GHz. Future work should focus on further optimization of the HBT technology, demonstration of amplifiers with lower noise using the existing technology, further reduction in dc operating power, and system demonstrations with these technologies.

REFERENCES


Table 2. Comparison of State-of-the-Art Cryogenic LNAs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Technology</th>
<th>Frequency (GHz)</th>
<th>Gain (dB)</th>
<th>Noise (K)</th>
<th>$P_{DC}$ (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[13]</td>
<td>InP-HEMT</td>
<td>0.5–13</td>
<td>38–44</td>
<td>3–7</td>
<td>15</td>
</tr>
<tr>
<td>[5]</td>
<td>InP-HEMT</td>
<td>4–8</td>
<td>39</td>
<td>2.3</td>
<td>4</td>
</tr>
<tr>
<td>[16]</td>
<td>m-HEMT</td>
<td>4–12</td>
<td>31</td>
<td>5.3</td>
<td>8</td>
</tr>
<tr>
<td>[7]</td>
<td>SiGe-HBT</td>
<td>4–8</td>
<td>25–30</td>
<td>8</td>
<td>0.6</td>
</tr>
<tr>
<td>This Work (Standard)</td>
<td>SiGe-HBT</td>
<td>4–8</td>
<td>25–31</td>
<td>3.4–4.7</td>
<td>1</td>
</tr>
<tr>
<td>This Work (Optimized)</td>
<td>SiGe-HBT</td>
<td>4–8</td>
<td>25–31</td>
<td>2.6–3.7</td>
<td>1</td>
</tr>
</tbody>
</table>