Load Modulated Balanced mm-Wave CMOS PA with Integrated Linearity Enhancement for 5G applications

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Abstract— The paper presents an mm-Wave load modulated balanced amplifier (LMBA) architecture across 30-40 GHz. The architecture is implemented with a transformer-based hybrid at input and output to allow wideband power combining and achieve high isolation with a control PA for load-modulation and back-off efficiency enhancement across 30-40 GHz. To overcome the compressive behaviour of an LMBA and enhance linearity, an integrated adaptive biasing is integrated on-chip allowing superior ACLR performance across 30-40 GHz. Under CW excitation, the two-stage LMBA demonstrates output power of 18.5-20 dBm, output drain efficiency >30% across 30-40 GHz. The modulation capabilities of LMBA are tested using a 64 QAM signal with a data rate of 6 Gbps wherein PA demonstrates EVM of -26.4 dB and ACLR of -29 dBc at an average output power of 10.6 dBm. To the best of the authors’ knowledge, this is the first load-modulated balanced PA at mmWave in silicon.

Keywords—load modulation, power amplifier, 5G, mm-Wave, transformer, hybrid.

I. INTRODUCTION

The 5G new radio (NR) bands across 28-40 GHz pose unique design challenges to the transmitter front-end in terms of achievable both peak and back-off efficiencies and linearity across wideband frequencies. Conventionally, ClassA/AB bias PAs show very low efficiency at back-off, while load modulation techniques like Doherty, Outphasing, Chireix have been explored as combining architectures with efficiency enhancement with a relatively narrower bandwidth [1]. While the bandwidth can be enhanced with transformer-based power combining and frequency-dependent load-modulation with mmWave DACs [2,3], this often comes at the expense of linearity and complex high-speed DSP. In addition to enhancement of bandwidth and back-off efficiency, the linearity consideration is particularly important since complex digital pre-distortion operating with Gbps links can be very power hungry and challenging to integrate [4]. Within the class of power combining, load modulation architecture based on balanced amplifier structure has been untapped at mmWave frequencies. For an efficient power combining over a wide bandwidth, a balanced amplifier is a favourable candidate wherein two amplifying devices run in quadrature i.e., they are operating 90 degrees apart in transmission phase. However, the balanced PA cannot exhibit any load modulation or mutual load pulling as both devices are biased under the same class of bias.

In this paper, we present a transformed hybrid based load-modulated balanced PA in 65 nm CMOS across 30-40 GHz to allow wideband back-off efficiency enhancement with integrated adaptive biasing circuitry to enable high linearity and AM/AM flatness. The two-stage LMBA demonstrates output power of 18.5-20 dBm, output drain efficiency >30% across 30-40 GHz and can support a 64 QAM signal with a data rate of 6 Gbps with EVM of -26.4 dB and ACLR of -29 dBc at an average output power of 10.6 dBm. To the best of the authors’ knowledge, this is the first load-modulated balanced PA at mmWave in silicon.

II. LOAD MODULATED BALANCED POWER AMPLIFIER

The balanced amplifier uses the classical quadrature hybrid wherein the two PAs combine through two ports that are isolated with respect to each other [5, 6]. The signals cancel in the isolated port that is terminated with a resistive loading to support balanced operation, delivering the combined power into the desired load (Fig. 1). This isolation of the output port can be exploited to inject a control signal with varying amplitude and phase to load modulate the individual balanced PAs (BPA) which experience the same load modulation.
control PA (CPA) actively synthesizes any targeted impedance at the balanced PA output depending on the power or amplitude \( (c) \) and phase \( (\phi_c) \) of the injected signal. The variation of amplitude, \( c \), changes the load impedance as a function of power which provides back-off reconfigurability while phase, \( \phi_c \), moves impedance on a constant VSWR circle. Through simultaneous control of \( c \) and \( \phi_c \), both the BPAs can be matched to a 2-D plane on a Smith Chart that is necessary of simultaneous wideband and power back-off efficient operation (Fig. 1). It can also be noted that unlike Doherty, wherein the output phase of auxiliary determines load modulation in main and power is only recovered if current combine in phase, LMBA has a distinctive feature given by the fact that the control power is fully recovered at the output port irrespective of load modulation.

To demonstrate the load modulation, both BPAs operate in class AB/B, the CPA is turned off i.e., \( c = 0 \), when input drive \( b \) is below the threshold \( 0 \leq b \leq \beta \), where \( \beta \) is the transitioning or turn off power level of CPA. Beyond this, the CPA is turned ON for \( \beta \leq b \leq 1 \). The control of \( \beta \) synthesizes different loading conditions across various PBO levels shown in Fig. 1. The injection current through the CPA load modulates the BPAs, with the impedance changing from \( R_{\text{opt}}/\beta \) to \( R_{\text{opt}} \) thereby ensuring voltage saturation for BPA after CPA turns on. As mentioned before, the driving conditions of the CPA creates different PBO curves, \( \beta = 0.5 \), corresponds to PBO=3.5 dB as shown in Fig.1, unlike Doherty where same load modulation occurs for PBO of 6 dB.

While LMBA can enable reconfigurable PBO levels, it suffers from an inherent compressive behaviour because the input and output back off are not linear in realistic systems. This compressive nature in presented work is mitigated using an adaptive biasing circuity, that allows reduced gain compression in the main BPAs and gain expansion in the CPA to minimize overall AM-AM distortion. The presented mm-Wave LMBA architecture consists of two-stage BPAs and CPA with transformer-based hybrids in the input/output stage and transmission-line based matching, as shown in Fig. 2 (a).

The CPA is sized at 1/2 the size of the BPA to allow a load-modulation enhancement at 4.0 dB PBO under full injection. In the proposed architecture three hybrids are used: two as input splitters and one as combiner at the output. The lumped equivalent model for transformer-based hybrid is shown in Fig. 2 (a) and is used as a design starting point. Firstly, to improve isolation at the injection CPA port, a second-order hybrid is implemented that improves isolation by around 15 dB (Fig. 2 (b)). Secondly, mutual coupling and capacitance between the transformers (with 1:1 turn ratio) are optimized for wideband impedance transformation and to ensure high isolation (> -20 dB) and combining efficiency (> 80%) across 30-40 GHz (Fig. 2 (b), bottom cell). Likewise, the input RF signal is divided into BPA and CPA branch respectively using a hybrid that is designed to simultaneously maintain the desired power splitting ratio and the targeted phase difference for frequency reconfigurability (which is co-optimized with input hybrid and
input matching networks). All the three branches namely, BPA1, BPA2 and CPA (active size half of BPA1/2) are driven with a driver amplifier matched using a wideband interstage network and an adaptive biasing circuitry in order to simultaneously optimize back-off efficiency enhancement and linearity [7].

III. MEASUREMENT RESULTS

The proposed architecture is implemented in 65 nm bulk CMOS process. The die photo is shown in Fig. 3 and measures 1.4mm x 1.05mm. Fig. 4 shows the measured operating space of the proposed architecture showing output drain efficiency (DE\textsubscript{out}) and output power. The input gate controls for BPA (V\textsubscript{gs-BPA1}, V\textsubscript{gs-BPA2}) and CPA (V\textsubscript{gs-CPA}) are swept for different input power levels which can be tracked using the integrated adaptive bias circuitry. This circuitry comprises of two cascaded stages as shown in Fig. 2(a). The working principle is similar to [8],[9]. When the input power is low, the input voltage swing to the adaptive biasing section is low which generates smaller low-pass filtered output which is fed as bias to the gate of the PA. Similarly, when the input power is high, the bias voltage increases which in turn increases the gain giving us a flat AM-AM profile. This adaptive biasing can be configured with voltage controls to allow tracking of the various curves in Fig. 4, such as shown in the representative examples of maximum back-off efficiency enhancement and gain flatness. Fig. 4 demonstrates the fundamental trade-offs in AM/AM flatness and linearity, where the single-minded approach of enhancing back-off efficiency comes at a cost of degraded linearity requiring complex digital pre-distortion operating at GS/s. The non-monotonic gain behaviour along with a steep compression at higher power levels directly impacts the ACLR and EVM for a spectrally-efficiency modulation scheme such as 64-QAM. In order to achieve a flat gain over output power (bottom figure on gain flatness), the peak efficiencies are compromised because

![Fig. 3. Chip Microphotograph of the mm-Wave LMBA.](image)

![Fig. 4. Measured operating space of the PA at 33 GHz. The adaptive biasing circuitry allows co-optimization of back-off efficiency and linearity, as shown in the measured PA performance.](image)

![Fig.5. Continuous-wave measurements across 30-40 GHz. (a) Output Drain Efficiency with and without CPA being turned on at 33 GHz. The grey curve represents the trajectory-region of load modulation. (b) Psat and (c) Output Drain efficiency at PBO across frequencies. (d)-(f) Individual drive ups with gain and output drain efficiency at 33, 37 and 40 GHz.](image)
the device is not compressed enough to output the maximum power out of the active cells. Thus, for a pragmatic trade-off between linearity and back-off efficiency, an adaptive biasing objective function is selected such that back-off efficiencies can be traced with a minimal gain compression of 2-3 dB.

A. Continuous-Wave Measurements:

The continuous wave (CW) measurements at the large-signal are reported in Fig. 5. The two-stage PA demonstrates load modulates by turning on and off CPA as shown in Fig. 5(a) (top figure). Under CW excitation the PA delivers an output power from 18.5-20 dBm from 30-40 GHz. The output drain efficiency (DEout) across the band is reported in Fig. 5(b)-(c) for PBO of 0 dB with DEout >30% with a maximum of 38% at 33 GHz. We show drain efficiency Since the CPA is half in size of BPA1, the output drain efficiency (DEout) is reported at 4 dB OBO. The back-off efficiency shows an enhanced from 1.4x-1.8x across the band as compared to Class A amplifiers. The drive-ups at individual frequencies of 33/37/40 GHz with gain compression within 2 dB in order to meet the objective for high AM/AM flatness are plotted in Fig. 5(c)-(e).

B. Modulation Measurements:

The modulated PA performance is evaluated using 16/64 QAM modulation with 1Gs/sec at 33 GHz (Fig. 6(a)). The PA exhibits an EVM of -26.4 dB and ACLR of -29 dB at Pavg of 10.6 dBm (a typical requirement for user equipment PAs) and average efficiency of 12.1% for 64QAM. The measured output spectrum constellations for 1GS/sec and 2Gs/sec are also reported in Fig.6 (a), demonstrating wideband high capacity data rate of up to 6 Gbps. The presented mm-Wave LMBA stands out as one of the first non-Doherty load modulated architecture with the state-of-the-art demonstrated data-rate, linearity and average efficiency amongst silicon PAs and is reported in Fig.6(b).

IV. CONCLUSION

In this paper, we presented the first mm-Wave load modulated balanced PA with adaptive biasing for broadband back-off efficiency enhancement and linearity enhancement. The chip fabricated in 65-nm bulk CMOS process demonstrates a Pout of 18.5-20 dBm and output drain efficiency exceeding 30% across 30-40 GHz. The chip also supports 64 QAM with the data rate of 6 Gbps at EVM of -26.4 dB, ACLR of -29 dB at a typical output power of 10.6 dBm.

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