A W-Band Chip-to-Printed Circuit Board Interconnect

Björn Deutschmann, Arne F. Jacob
Institute of High-Frequency Technology, Hamburg University of Technology, Germany
bjoern.deutschmann@tuhh.de, jacob@tuhh.de

Abstract — An alternative to wire-bonding and flip-chip interconnects of integrated circuits and printed circuit boards (PCB) is presented. The flip-line interconnect combines the advantages of wire-bonding and flip-chip technology while avoiding their disadvantages. It is especially useful for prototype setups where device inspection and repairability are crucial. The proposed structure is analyzed using full-wave simulation software. It is shown, that in contrast to wire-bonding, the transition length is not critical. A transition from a CMOS chip with a pad pitch of 100 µm to a regular PCB is manufactured. Measurements at W-band (75-110 GHz) reveal a return loss better than 12 dB and transmission above −3.4 dB.

Keywords — wire-bonding, W-band, interconnect, flip-chip

I. INTRODUCTION

Modern high-frequency CMOS technology has rapidly evolved in the last decades [1]–[3]. Integrated CMOS circuits operate at frequencies of 100 GHz and beyond [4], [5]. Integrating such devices into communication systems requires interconnects with other components on printed circuit boards (PCB) such as antennas or feed networks. On-chip antennas have been demonstrated in [6]. They consume relatively large areas on the chip and the radiation efficiency is poor. Using off-chip antennas requires a high-frequency signal interconnect from the chip to the PCB. There are two major methods for directly connecting a chip to a PCB, i.e. flip-chip and wire-bonding.

For wire-bonding the chip is mounted to the PCB with its backside. This way a good thermal connection to the substrate is established and thermal vias can be utilized. One also can inspect the chip’s active area and contact pads, which is handy for prototype setups. The disadvantage is the parasitic inductance introduced by the bond-wires, which is why this technique is used mostly below 40 GHz. However, it has been shown, that at higher frequencies narrow band compensation is possible [7]. For broadband millimeter-wave applications wire-bonding is usually avoided.

The most common alternative is flip-chip technology. Here the chip is mounted with the active area facing the PCB [8]. Stud bumps between the pads and the PCB traces make the electrical contact. Due to the reduced parasitic inductance the transition is usable up to very high frequencies [9]. However, disadvantages are proximity effects, mechanical instability (if no underfill is used) and the need for an additional heat sink on the backside of the chip. Additionally, no inspection nor repair of established interconnects is possible.

To achieve well matched interconnects up to very high frequencies while maintaining the advantages of wire-bonding the use of a coplanar line section as illustrated in Fig. 1 is proposed. In the following this is called flip-line. The chip is mounted in a cavity in the substrate with the pads aligned with the line on the PCB. Gold stud bumps are placed on the pads and a coplanar line segment with a defined line impedance placed on top makes the contact. A thermally curable adhesive, not shown in Fig. 1, is used to seal and reinforce the interconnect.

This way the advantages of wire-bonding and flip-chip technology are combined. A good thermal contact can be achieved with a thick metal ground plate. The flip-line is only used for high-frequency connections on the chip. For inputs and outputs at lower frequencies and DC-pads regular wire-bonding can be used. This allows inspection of the chip’s active area and the interconnects. One drawback of the proposed interconnect is an increased insertion loss compared to flip-chip technology, since in principle two flip-chip interconnects are involved per flip-line transition.

The paper is organized a follows. First, basic restrictions for the parameters of the proposed interconnect are introduced and its performance is evaluated by simulation. Section III discusses manufacturing aspects and Section IV reports the measurement results.

II. DESIGN

Some restrictions have to be respected already in the design phase in order to allow reliable manufacturing of the designed components using the in-house production facilities. The smallest via diameter is 150 µm and the gap size between adjacent copper traces must not be smaller than 60 µm. The width of the smallest copper trace is 40 µm. Going to even smaller values is possible only at the expense of a drastically reduced yield.

Fig. 1. 3D view of the proposed interconnect. The flip-line is mounted on the chip and PCB with thermally curable glue (not shown here).
The ground pads on the PCB have a width and length of 50 µm. For the used Rogers 4350B substrate with a height \( h_{\text{PCB}} = 100\mu\text{m} \) the resulting line width \( w_{\text{line}} \) is 200 µm. The ground pads on the PCB have a width and length of \( l_{\text{pad}} = w_{\text{pad}} = 250 \mu\text{m} \). This fits a via with a diameter \( d_{\text{via}} = 150 \mu\text{m} \), leaving a margin of 50 µm. The distance between the line and the ground pads is set to \( d_g = 70 \mu\text{m} \) in order to obtain a compact transition.

The interconnect, i.e., the flip-line should have the same line impedance as the chip and the PCB. It is composed of a coplanar waveguide (CPW) without backside ground plane as shown in Fig. 3. The center line as well as the adjacent ground conductors have a length of \( l_0 \) to bridge the gap between chip and PCB. Then a linear taper is used for each conductor to match the chip pads. The tips of the flip-line are designed according to the chip pad dimensions with a conductor to match the chip pads. The tips of the flip-line are equal to the line width \( w \) in order to obtain a compact transition.

A length of \( l_1 = 100 \mu\text{m} \) is chosen as a smaller value would cause sharp edges, which impairs manufacturing. The length \( l_0 \) is determined such that the gap between chip and PCB is bridged and the flip-line fully overlaps the ground pads on the PCB \( l_0 = m_{\text{Chip}} + l_{\text{Gap}} + l_{\text{pad}} - l_i \). The only remaining parameter is the gap length \( l_{\text{Gap}} \) between chip and PCB.

The proposed structure is modeled and simulated in CST Studio Suite. Figure 4 shows the cross section of the model along its symmetry plane. It also shows the nonconductive glue used to bond the flip-line to the PCB and chip. Assumptions for the simulation are a diameter and height of the gold stud bumps on the chip’s pads of 50 µm and 25 µm, respectively. The flip-line as well as the PCB are made from Rogers 4350B with 100 µm thickness. The chip has a total height of 275 µm but the pads and line (used for the setup) extend less than 50 µm into the die. The rest of the chip is simulated as bulk silicon.

For meaningful simulation results the permittivity of the nonconductive glue (Delomonopox NU257) has to be known. Electrical parameters of the other materials are known or available from data sheets. To characterize the glue, a sample block of 2.54 mm x 1.27 mm x 9.2 mm (WxHxL) is manufactured and placed inside a split block WR-10 waveguide (Fig. 5). Measurements with and without the sample are performed to obtain the permittivity and loss tangent of the material, which are shown in Fig. 6. In the simulation, the mean values of \( \epsilon_r = 3.4 \) and \( \tan(d) = 0.02 \) are used.

Figure 7 shows the scattering parameters of the transition.
Material Under Test

Fig. 5. Sample block of the glue and the split-block waveguide used for the material characterization.

![Split-Block Waveguide](image)

Loss tangent

\[ \begin{align*}
\text{Frequency (GHz)} & \quad \text{Relative permittivity} \\
70 & \quad 3.0 \quad 0.02 \\
80 & \quad 3.2 \quad 0.04 \\
90 & \quad 3.4 \quad 0.06 \\
100 & \quad 3.6 \quad 0.08 \\
110 & \quad 3.8 \quad 0.1
\end{align*} \]

Fig. 6. Measured relative permittivity and loss tangent of the thermally curable glue.

for gap sizes \( l_{\text{Gap}} \) from 30 µm to 300 µm corresponding to \( l_0 \) is 260 µm to 530 µm. The interconnect length has only a minor effect on the insertion loss and the reflections at port 2. At port 1 the reflections vary more but remain at a low level.

**III. MANUFACTURING**

We conduct the experiments with a 50 Ω line on a CMOS chip (see Figure 8). The chip is 275 µm thick, the PCB only approximately 135 µm (including copper layers). In order to vertically align the top surfaces of the stud bumps on the chip and PCB a baseplate with a 115 µm deep cavity is prepared.

The chip is glued in there using thermally curable conductive glue. The same glue is used to place the PCB next to the chip on the baseplate. Here, a gap of 50 µm between chip and PCB is chosen. On the flip-line, the resulting length \( l_0 \) of the straight CPW section is 280 µm. Figure 9 shows the following process steps. First, stud bumps are placed on the chip pads. Then, nonconductive glue is applied onto the stud bumps and the PCB contact pads. The flip-line, which is trimmed to the required dimensions, is placed accurately in the desired position using a Finetec Fineplacer. While the glue is thermally cured at 180 °C for 1 min the flip-line is pressed onto the contacts such that the glue is squeezed away and a reliable electrical contact is established. The PCB and the flip-line are manufactured using standard lithographic processes.

The alignment of the flip-line and the pads on the chip can be realized with placement errors below 15 µm using the fineplacer. A concern is the long-term stability of the bond, since it interfaces different metals, i.e., aluminum, gold, and copper. However, we did not observe any material degradation in our breadboard setups. To avoid long-term corrosion effects, which could impair the interconnect performance, a chip with gold pads and a PCB with nickel-gold coating should be used.

![Reference Planes](image)

Fig. 9. Manufacturing process of the flip-line transition. The chip with stud bumps and line glued in place is depicted in (a). (b) gives enlarged view on the stud-bumps. (c) shows the flip-line segment which is placed on chip and PCB in (d).
The measurements are carried out on an Agilent PNA E8361A with frequency extenders for W-band. To connect the manufactured devices Cascade Infinity Probes are used on a manual probe station. A SOLT calibration is performed with a commercial calibration substrate in order to set the reference plane to the probe tips. Afterwards, the calibration standards depicted in Fig. 10 are measured. The scattering matrix of the probe-to-microstrip transition is calculated from these results in a post-processing step and removed from the actual measurement data of the flip-line transition [10].

Test structures on the chip are measured in the same way to remove the pads and half of the line on the chip from the measurements. The results in Fig. 11 are given with respect to the reference planes indicated in Fig. 9(a).

The measured insertion loss is 2.4 dB at 75 GHz and increases to 3.4 dB at 110 GHz. This is slightly more than the simulated values of 1.8 dB and 2.8 dB. The difference is likely caused by inaccurate material parameters in the simulation such as the surface roughness of the copper traces and the loss tangent of the substrate material. The return loss is also in good agreement with simulation. At port 1 (chip side) it exceeds 14 dB for the entire W-band. At port 2 (MSL) the return loss is better than 15 dB up to 100 GHz and decreases to 12 dB at 110 GHz.

V. Conclusion

A novel high frequency chip-to-PCB transition with broadband performance is presented. In contrast to wire-bonding it is also suitable for relatively long interconnects while offering a good return loss. The transition is useful for prototype setups since it allows visual inspection of the active chip area. The manufactured transition confirms the predicted performance, i.e., an insertion loss below 3.4 dB and a return loss above 12 dB over the entire W-band.

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References