A Low-Loss Balun-Embedded Interconnect for THz Heterogeneous System Integration

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Abstract—An interconnect for THz heterogeneous integration is proposed in this work. Two transmission lines deployed on a 40-nm CMOS chip and an IPD carrier, respectively, are coupled together to form a Marchand balun during a flip-chip packaging process. By doing this, the proposed interconnect can provide packaging and balun functions simultaneously. Two interconnects using the proposed idea are demonstrated with measured and simulated insertion loss of 0.9 and 1.4 dB at 169 and 340 GHz, respectively.

Keywords—heterogeneous integration, interconnect, low-loss, Marchand balun, THz.

I. INTRODUCTION

THz science and technologies have attracted great attention in recent years because it can be used for many useful applications, including biomedical imaging, security screening, and high-speed data communication [1], [2]. Most of the previous studies adopt a system-on-a-chip (SoC) approach to integrate passive devices, active circuits, and antennas into a single chip [3]. However, on-chip antennas not only occupy large chip area, but also exhibit extremely low radiation efficiency, resulting in low-performance and high-cost THz systems. Using a system-on-package (SoP) approach is a good alternative to solve the aforementioned issues. Sub-blocks of a THz system can be implemented in different technologies and then are integrated together on a low-cost and low-loss carrier. Hence the advantages of the different technologies can be fully employed to realize a high-performance and low-cost THz heterogeneous system.

Interconnects are the key for the success of the SoP integration. In THz band, the method of metal packaging to waveguide is often chosen since the induced power loss is extremely low. However, the waveguide is bulky, which is not suitable for realizing a compact system. A THz bondwire interconnect was proposed to work in THz frequencies [4]. Yet its performance is sensitive to the bonding variation. A resonator coupling technique was reported to realize a THz interconnect [5]. However, it requires the signal to be in a differential form, which is usually not available in THz frequencies. THz signals are frequently generated by using frequency multipliers [2]. They only support single-ended output. If differential output is desired, additional lossy baluns are required, causing higher power loss and degrading system performance.

In this work, a THz interconnect which can provide packaging and balun functions simultaneously is proposed. The

![Fig. 1. (a) Concept of the proposed balun-embedded THz interconnect. (b) Cross-sectional views of the adopted technologies. (c) Equivalent circuit.](image-url)
proposed interconnect can be used to transit a single-ended signal from a chip to a differential one on a carrier or vice versa. With the proposed interconnect, additional baluns are not required. This not only reduces the power loss, but also consumes less chip area. For instance, the input balun in the RF port can be removed if the proposed idea in this work is adopted. The proposed interconnect is very suitable for low-loss THz system heterogeneous integration. The following sections will go through the design details.

II. BALUN-EMBEDDED THZ INTERCONNECT DESIGN

Fig. 1(a) shows the concept of the proposed balun-embedded THz interconnect. Two transmission lines are deployed on a 40-nm CMOS chip and an integrated-passive-devices (IPD) carrier, respectively. The cross-sectional views and material properties of the 40-nm CMOS and IPD technologies are illustrated in Fig. 1(b). The chip is then flipped and bonded to the carrier using an Au-Au thermal-compressive technique with 5-μm thick gold bumps. By doing this, these two
transmission lines can be coupled together to form coupled transmission lines. Moreover, the coupled lines are intentionally arranged to a Marchand balun structure as illustrated in Fig. 1(c). Therefore, the proposed interconnect not only can provide signal transition from the chip to the carrier, but it can also give single-ended to differential signal conversion. Note that the maximally achievable characteristic impedance of a microstrip line on the adopted IPD technology is only 43 Ω due to large capacitance per unit length. Hence the proposed interconnect is designed to conduct impedance transformation from a differential impedance $Z_{\text{chip, diff}}$ of 86 Ω on the chip side to a single-ended impedance $Z_{\text{carrier}}$ of 43 Ω on the carrier side. For a Marchand balun with port number designation shown in Fig. 1(c), its scattering parameters $S_{11}, S_{21},$ and $S_{12}$ can be easily derived as $S_{11} = -C^2 + T^4/(1+C^2)$, $S_{21} = -CT + CT^3/(1+C^2)$, $S_{12} = CT - CT^3/(1+C^2)$, where $C$ equal to $(Z_{0e} - Z_{0o})/(Z_{0e} + Z_{0o})$, $T$ equal to $-j \sqrt{1 - C^2}$, $Z_{0e}$, and $Z_{0o}$ are the coupling coefficient, transmission coefficient, even-mode characteristic impedance, and odd-mode characteristic impedance of the coupled line, respectively [7]. The above equations are valid as the multiplication of $Z_{0e}$ and $Z_{0o}$ is equal to $Z_{\text{carrier}}^2$, that is, $Z_{0e}Z_{0o} = Z_{\text{carrier}}^2$. The proposed concept of the balun-embedded THz interconnect is demonstrated by 180- and 340-GHz interconnect designs.

Fig. 2(a) shows the physical structure of the proposed 180-GHz balun-embedded THz interconnect design. The transmission lines on the chip and the carrier are coupled to form coupled lines of $CL_{1,D}$ and $CL_{2,D}$. The length of $CL_{1,D}$ and $CL_{2,D}$ is designed as 322 μm, corresponding to quarter-wave wavelength at 180 GHz. $Via_{2,DS}$ are added to short one end of $CL_{1,D}$ and $CL_{2,D}$ to the ground. The ground on the chip side is connected to the ground of the carrier side through vias of $Via_{1,DS}$. To have the $S_{11}$ of the proposed interconnect zero, the coupling coefficient $C$ must be $1/\sqrt{3}$, i.e., 0.577. In general, the coupling coefficient can be designed by selecting the line width and line spacing of the coupled line for the desired $Z_{0e}$ and $Z_{0o}$ values. However, as shown in Fig. 1(b), the vertical distance of the coupled line is too far as 8 μm, resulting in low coupling coefficient. The implemented $C$ is only 0.48 as the width of the coupled line is 26 μm. If $C$ is lower than the required value of 0.577, the input impedance at 180 GHz is increased to 1.63× $Z_{\text{carrier}}$, that is, 70.1 Ω, leading to low input return loss of only 12.4 dB and narrow operation bandwidth. A quarter-wave transmission line can be used to conduct the impedance matching for better return loss and wider bandwidth. To convert the input impedance of 70.1 Ω to the desired 43 Ω, the quarter-wave transmission line should have the characteristic impedance of 54.9 Ω. However, as mentioned before, the maximally achievable characteristic impedance of an on-carrier transmission line is only 43 Ω. The input impedance cannot be matched by just using a single quarter-wave transmission line. To solve the issue, two quarter-wave transmission lines $TL_{1,D}$ and $TL_{2,D}$ are added to achieve the impedance matching condition. The characteristic impedance of $TL_{1,D}$ is designed as 43 Ω by choosing the line width of 10 μm. The line length of $TL_{1,D}$ is 285 μm, corresponding to quarter wavelength at 180 GHz. With $TL_{1,D}$ the input impedance can be transformed from 70.1 Ω to 0.59× $Z_{\text{carrier}}$, that is, 25.4 Ω. In the next step, $TL_{2,D}$ with the line width of 17.4 μm for 33-Ω characteristic impedance and line length of 245 μm corresponding to quarter wavelength at 180 GHz is employed to transform the impedance of 25.4 Ω to the final desired value of 43 Ω. Hence the impedance matching condition is fulfilled. Fig. 2(a) and 2(b) illustrate the simulated $S$-parameters and amplitude and phase imbalances of the differential output of the 180-GHz interconnect, respectively. Note that the differential $S$-parameter $S_{22}$, not single-ended ones, is reported in Fig. 2(b). The simulated insertion loss is only 1.4 dB at 180 GHz while the input and output return loss can be higher than 10 dB from 170 to 192 GHz. The amplitude and phase imbalances can be kept smaller than 0.7 dB and 1° from 140 to 200 GHz.
The same operation principle is also applied to design a 340-GHz balun-embedded THz interconnect as shown in Fig. 3(a). The length of \( CL_{1T} \) and \( CL_{2T} \) is designed as 186 \( \mu \)m, corresponding to quarter wavelength at 340 GHz. The width of the coupled line is designed as 21 \( \mu \)m to maximize the coupling strength. Two quarter-wave transmission lines \( TL_{1T} \) and \( TL_{2T} \) with line width and length of 133, 10, and 130, and 25.5 \( \mu \)m, respectively, are added to conduct the required impedance transformation so that the input can be power matched at 340 GHz. Fig. 3(a) and 3(b) exhibit the simulated S-parameters and amplitude and phase imbalances of the differential output of the 340-GHz interconnect, respectively. The insertion loss is only 1.4 dB at 340 GHz while the return loss can be kept higher than 10 dB from 326 to 352 GHz. The amplitude and phase imbalances can be smaller than 0.6 dB and 0.8° from 300 to 380 GHz. Obviously, the proposed interconnect not only provide low-loss package, but it can also give excellent signal conversion from a single-ended form to a differential one. Such a multi-function interconnect is very suitable for THz heterogeneous system integration.

III. Experimental Results

As shown in Fig. 4, a back-to-back configuration is designed to verify the proposed idea. An on-chip coplanar strip (CPS) line with an odd-mode characteristic impedance of 86 \( \Omega \) and length of 345 \( \mu \)m is inserted to connect the two proposed interconnects (THz Interc.). Therefore, the measured and simulated results reported later will include the characteristics of the two proposed interconnects and the on-chip CPS line. Fig. 5 illustrates the photos of a 40-nm CMOS chip, an IPD carrier, and a packaged interconnect. The Thru-Reflect-Line (TRL) deembedding technique is used to move the reference plane of the S-parameters at the desired position. Due to the measurement equipment limitation, only the performance of the 180-GHz interconnect can be measured.

Fig. 6 shows the measured and simulated return loss and insertion losses of the combination of the two proposed interconnects and the on-chip CPS line. The measured minimum insertion loss is 2.2 dB at 169 GHz while the input and output return losses can be kept higher than 10 dB from 160 to 176 GHz. Essentially, the measured results follow well with the simulated ones. The operation frequency is shifted to a lower band. This might be due to the fact that the material parameters are different as those used in the simulation at such a high operation frequency. Moreover, \( S_{11} \) and \( S_{22} \) exhibit different frequency responses, which is different from the simulated results. If the interconnect is fully symmetric with respect to the interconnect center, \( S_{11} \) and \( S_{22} \) should be the same. Hence this discrepancy might be caused by the misalignment between the chip and the carrier during the flip-chip bonding process, leading to an asymmetric structure. As mentioned before, the measured insertion loss of 2.2 dB actually includes the loss of the two proposed interconnects and one on-chip CPS line. Due to the chip area limitation, no testkey is designed to measure this CPS line. According to the simulation result, the CPS induces insertion loss of 0.4 dB at 169 GHz. So the insertion loss of a single interconnect can be estimated as (2.2–0.4)/2, that is 0.9 dB at 169 GHz. Obviously, the proposed interconnect shows low-loss performance. The consistency between the measured and simulated results also verify the proposed interconnect can also provide excellent balun function simultaneously. Moreover, the success of the 180-GHz interconnect implies that the 340-GHz interconnect should also function well. Such a low-loss and multi-function interconnect is very suitable for THz heterogeneous system integration.

IV. Conclusion

A low-loss and balun-embedded THz interconnect is proposed and verified by the experimental results. By intentionally arranging two transmission lines as a coupled Marchand balun structure during a flip-chip packaging process, the proposed interconnect not only can provide low-loss packaging, but it can also give balun function simultaneously. The measured insertion loss of a single interconnect is only 0.9 dB at 169 GHz while the return loss can be higher than 10 dB from 160 to 176 GHz.

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