Efficiency Enhancement Technique using Doherty-Like Over-The-Air Spatial Combining in a 28 GHz CMOS Phased-Array Transmitter

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Abstract— This paper presents an efficiency enhancement technique for high bandwidths and high PAPR signals using over-the-air spatial beamforming implemented in a 4-element phased-array transmitter at 28 GHz. The baseband signal is decomposed in the time domain into two streams. One is the signal with PAPR reduction, and the other consisting only the signal peaks, which are of low occurrence. These two streams are up-converted and transmitted through different RF chains, each optimized for the corresponding output power, and recombined over-the-air to reconstruct the original signal. An LO-phase-shifting architecture using sub-sampling PLL is employed per array element, where the PLL serves also as a phase shifter with sub-1° phase resolution. The transmitter was fabricated in 65 nm CMOS process. The measurements show efficiency enhancement of 75% relative to a 3-element linear phased array with similar output power for a 320 MHz signal with 9 dB PAPR and EVM of -31 dB at 21 dBm EIRP.

Keywords— 5G, CMOS, phased-array, spatial combining, transmitter, efficiency enhancement.

I. INTRODUCTION

In recent years, we have witnessed intensive research on integrated phased-arrays with beamforming capabilities to support Gb/s data-rates for the next generation of communication systems (5G). The main challenges in the realization of such systems is to achieve low-cost and high energy-efficiency, particularly for high peak to average power ratio (PAPR) signals, in order to provide a solution to handsets and base-stations, especially at the 28 GHz band [1][2][3]. Recent studies utilized over-the-air combing of the different data streams instead of combining them on die [4],[5] to enhance the transmitter efficiency. However, these techniques require several additional antennas and chains and are therefore less suitable for handset applications.

In this paper, we propose an over-the-air combining technique for efficiency boosting in a 4-element phased array transmitter (TX) system operating at the carrier frequency of 28 GHz, requiring only one additional antenna. This technique relaxes the power back-off at all chains by transmitting clipped signals with PAPR reduction, except in the extra element that transmits only the signal peaks, which are of low occurrence, while meeting the standard spectral emission masks. In addition, our technique enables wider reception spatial angle compared to [4],[5] and provides better robustness to inaccuracies in the spatial recombining of the transmitted signal.

Previously, we demonstrated this technique at the 5 GHz band [6] using a simple RF front end. This work features a fully integrated 4-element phased array at 28 GHz, along with an integrated up-conversion mixer and a local sub-sampling PLL (SSPLL) per array chain, which also serves as phase shifter with 10-bit resolution for accurate beam steering. The combination of over-the-air combining with local LO phase-shifting architecture and a SSPLL per chain provides a compact, efficient and scalable phased array implementation.

II. PRINCIPLE OF OPERATION

The transmitter architecture is shown in Fig. 1. The transmitter consists of 3 identical chains, denoted as main, and one higher power chain, denoted as peaking. At full transmit power, all the main chains transmit clipped signal, while the peaking chain transmits the residual peaks, in similarity with the Doherty amplifier technique. However, unlike the Doherty amplifier, the peaks are recombined coherently over-the-air at the receiver antenna to reconstruct the desired signal, as shown in Fig. 1. Owing to the reduction in power back-off requirement from each chain, along with the infrequent peaking events at which the peaking amplifier is active, the proposed technique has potentially higher energy efficiency compared with uniformly excited linear phased arrays (UELA). To obtain coherent operation, all SSPLLs are locked using the same reference.

![Fig. 1. Block diagram of the 4 channels phased-array. The envelope waveform is split between the transmission chains and combined over the air at the receiver.](image-url)
have a similar linear bandpass frequency response, the combined signal experiences the same linear bandpass filtering, ensuring correct signal reconstruction. Achieving identical frequency response among all channels is achieved fairly easily by integrating all chains on the same chip.

III. TRANSMITTER ARCHITECTURE

The transmitter IC includes 4 chains. Each chain includes a 2-stage PA, an IF input around 5 GHz, an up-conversion mixer to 28 GHz, a SSPLL, and a buffer that drives the mixer. The chains are completely independent, and all the PLLs are synchronized using a common clock at 1 GHz for coherent operation. The LO signal is fed into the mixer through a capacitive-neutralized buffer with high isolation to prevent pulling effects on the VCO. The circuit building blocks are fully differential with transformer-based matching networks and single ended IF and RF baluns. High-side up-conversion was selected to reduce the size of the VCO inductor and improve the isolation to the IF stage.

The per-chain SSPLL enhances the design scalability and power efficiency, and alleviates the power losses associated with high-frequency centralized LO distribution and phase shifting networks [7]. The SSPLL technique is selected owing to its inherent low power consumption and low noise characteristics [8]. Furthermore, the need for mm-wave phase shifters is obviated by integrating phase shift capabilities within the SSPLL.

IV. CIRCUIT DESIGN AND BLOCKS MEASUREMENTS

A. Power Amplifiers

The 2-stage PA designated for the main channels was designed with a capacitive-neutralized common source (CS) biased at class AB. Measurements of a PA breakout with a 1.2 V supply show a peak efficiency of 28% at 12 dBm output power and a gain of 16 dB. The peaking 2-stage PA was implemented as a cascode with capacitive neutralization, operating from a 2.2 V supply and biased close to class A. Its measurements show high gain of 21 dB, which is required for achieving the 16 dBm maximum output power target without compressing the mixer. Its peak efficiency is 19 % and it has an ON/OFF switching speed of 0.5 nsec. The 4 dB difference in P1dB between the peaking and main PAs is selected according to an optimization procedure for optimal array power efficiency. Figures 2(a) and 2(b) show the measured results of the PAs.

B. Up-Conversion Mixer

A double balanced mixer with an IF balun instead of the input gm stage is connected directly to the sources of the mixer’s core transistors to insure highly linear operation. The mixer consumes 10 mW power and has a conversion loss of 6 dB and a P1dB of 5 dBm for LO power of -4 dBm. The mixer’s IF BW is 2 GHz.

C. Sub-Sampling PLL

A cross-coupled VCO with current source biasing for minimal power consumption is implemented. The frequency range is 31-33 GHz, distributed over a 4-bit capacitor bank, and the phase noise (PN) is -100 dBc/Hz at 1 MHz frequency offset. The VCO consumes 3 mA from a 1.2 V supply.

10-bit high resolution phase shifter is incorporated within the PLL using a 4-bit digital-to-time converter (DTC) to set the delay of the reference, as well as a 6-bit current DAC that enables to offset the operating point of the gm stage to accurately control the static phase error of the PLL. The measured in-loop 6-bit phase shifting (PS) range is 84° with 0.86° RMS phase error [Fig. 2(c)]. A full 360° PS is achieved with the 4-bit DTC. Large loop BW of 65 MHz is chosen to obtain a fast phase switching of 15 nsec [Fig. 2(d)]. The PLL power consumption is 4.2 mW and 9 mW including the VCO buffer.

The 4-element transmitter IC size (including all the building blocks), is 2.8 mm². The full chip was fabricated in TSMC 65nm bulk CMOS technology (Fig. 3).

V. PHASED ARRAY BOARD DESIGN

The PCB including on-board antennas was designed for the system measurements. The chip die was connected directly to the PCB using wire-bonds. The PCB consists of four layers, with 4 mil Rogers RO4350B as the top and bottom cores and 22 mil prepreg Rogers RO4450F as the middle core (Fig. 4).
Four patch antennas in an H-plane arrangement were designed using CST simulator. The antenna dimensions are shown in figures 5(a) and 6(a). The distance between two adjacent antennas is \( \lambda/2 \), providing isolation of 20 dB. To achieve an operation BW between 27 GHz to 30 GHz, a height of 0.66 \( \mu m \) between the antennas to their ground plane is required. Hence, the antennas were printed at the top layer of the PCB, with an opening down to M3, which serves as ground (Fig. 3).

The antennas are matched to 50 \( \Omega \) using a recessed microstrip-line feed technique. For the receiver, a single patch antenna with the same geometry was fabricated. According to the simulation results, the TX antenna array and the RX antenna gains are 11.2 dBi and 5.5 dBi, respectively [Fig. 5(b) and Fig. 6(b)].

An EM simulation was performed to match the transition between the chip outputs to the antenna PCB feed lines. The transition matching network includes a series bond-wire inductance (a V-bond shape was used to reduce the inductance for broadband matching), a shunt printed parallel-plate capacitor, and an additional series inductor, as shown in Fig. 7. This transition network has a wideband response between 25 GHz to 30 GHz and 0.35 dB insertion loss at 28 GHz.

The routing length from the IC to the antenna is 1.6 mm with a loss of 1 dB.

VI. MEASUREMENTS

The main, peaking and enable signals were synchronized and transmitted at 5 GHz using Keysight M8195A arbitrary waveform generator (AWG). The receiver antenna was located at 50 cm distance from the transmitter antenna. An ERZIA ERZ-LNA-0200-5000-22-6 was used as the LNA. The received signal was recorded using a Keysight 63 GHz DSOZ634A scope running the Keysight VSA 89600 software [see Fig. 8(a)].

Initial calibration was applied to each chain to account for routing mismatches on the PCB as well as for routing mismatches of the 1 GHz reference on-die. The calibration was performed by aligning the phases of the chains and is required only once per setup. Single memory-polynomial-based digital predistortion (DPD) was used for all main chains, allowing operation at higher power and achieving higher system efficiency. DPD for the peaking chain is not required, but phase alignment of the peaking chain is performed after DPD correction of the main paths.

![Fig. 7. Transition matching network between the chip and the PCB.](image)

![Fig. 8. 28 GHz 4 element phased-array transmitter PCB including the measurement setup.](image)

![Fig. 8. Corresponding EVM for a 256 QAM constellation at full operation (3 mains + peaking).](image)
Figures 8(b) and 8(c) show the full system performance using a 256-QAM signal with 9 dB PAPR and 320 MHz BW. EVM of -31 dB was measured at EIRP of 21 dBm. The EVM is limited by the 8-bit resolution of the AWG. The spectrum of the combed signal with the peaking chain enabled and disabled is shown in Fig. 8(b).

The measured EIRP is shown in Fig. 9(b), 21 dBm at 28 GHz with 3 dB bandwidths between 27.5 to 29.5 GHz is achieved and is mainly limited by the patch antenna. EVM better than -30 dB was measured over a spatial angle of 10° at various scanning angles. As can be seen, the signal is recombined perfectly at all scanning angles, and has minor distortion around them, indicating the robustness of the proposed special combining technique. The beam pattern and the corresponding EVM results are presented in Fig. 9(a).

Fig. 9. a) Measured EVM and the corresponding gain around several position angles at EIRP of 21 dBm for boresight. b) EIRP measurement.

The overall system consisting of 3 main PAs and 1 peaking PA achieves an efficiency of 14% at 21 dBm total EIRP (Fig. 10) with EVM of -31 dB. This is an efficiency improvement of 75% compared to UELA consisting of 3 main PAs for similar operating conditions, which has 8% efficiency. The efficiency boost is driven directly from the PAPR reduction, along with a very small penalty of the peaking PA power consumption. When taking the 4th antenna gain into account, the EIRP without the peaking PA improves by 4/3, corresponding to 1.2 dB as shown in Fig. 10. This means that even when no additional antenna is used, the efficiency still increases from 10% to 14%, which is an improvement of 40%.

VII. CONCLUSION

A 4-channel over-the-air combining transmitter architecture and antenna array achieving 14% PA efficiency for -31 dB EVM at 9 dB back-off and 21 dBm EIRP at 28 GHz is presented, compared to 8% or 10% of UELA with 3 or 4 elements, respectively. The architecture utilizes LO phase-shifting with 10° phase resolution with a very low power sub-sampling PLL per transmitter chain. The proposed topology is flexible and can be easily scaled to larger arrays requiring only additional routing of the 1 GHz reference clock. Since the PLL sources are uncorrelated, the phase noise improves as the array scales. The robust over-the-air measurements indicate that this architecture is an excellent candidate for 5G mm-wave phased arrays standards.

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