Abstract—We have developed novel compact suspended stripline filters and low-loss passives based on MMIC wafer fabrication techniques and heterogeneous integration through gold-gold compression bonds. The key features are high precision, on-wafer testable for known-good-die, and high electromagnetic isolation. This approach is best suited to designs in the range of 0.5-100 GHz. As an example of applying this novel capability, a 0-11 GHz & 11-22 GHz contiguous diplexer filter was designed and fabricated to produce a SiC center-conductor die which is bonded and suspended in gold-plated silicon ground cavities using heterogeneous integration. EM modeling accurately predicts filter performance and multiple fabricated copies of the filter have near-identical S-parameters characteristics.

Keywords—suspended stripline filter, low loss filter, diplexer, multiplexer, heterogeneous integration, passive component, microstrip filter, micromachining, silicon carbide.

I. INTRODUCTION

The advantages of suspended stripline have long been understood for filters (diplexers) to generally achieve circuit miniaturization with reasonably low loss. However, limitations in manufacturing have typically necessitated loose specification tolerances or manufacturing accommodations such as high yield loss and/or manual tuning to achieve exacting performance specifications. We present here a novel method of fabricating suspended stripline filters which offer repeatability, manufacturability, mechanical robustness, first pass design success, and a versatile method to isolate filter elements to minimize undesired cross-coupling.

Our manufacturing method combines three emerging microelectronics fabrication technologies: SiC MMIC (Monolithic Microwave Integrated Circuit) processes with high precision metallization features and plated through-wafer vias based on GaN MMIC fab processes [1], silicon deep reactive ion etching (DRIE) micromachining [2], and heterogeneous integration die-to-die by means of gold-gold thermocompression bonding with micron level placement accuracy [3]. These batch fabrication methods are scalable to larger quantities needed for phased array or insertions such as mm-wave 5G.

For frequencies in the range of 2-40 GHz, distributed element stripline filters in printed circuit board and LTCC (Low Temperature Co-fired Ceramic) are common. The limitations of printed circuit board stripline filters include the large size of the through-layer vias, which preclude close spacing for optimal performance as frequencies move above 10 GHz, and significant variation in the physical dimensions and dielectric constant with change in temperature [4]. Limitations of LTCC include the change in z-axis thickness as the LTCC is fired, which can lead to variable manufacturing and challenges in achieving agreement between design and measured performance. While the dielectric constant of typical board materials and LTCC is low, it is still higher than air; consequently stripline that is suspended in an air cavity will have the potential for higher Q [5].

Previous demonstrations that use silicon micromachining to produce filters have primarily focused on cavity filters for frequencies of higher than 90 GHz [6, 7]. For such high frequencies, silicon micromachined cavity filters are a well-regarded solution because the filter DRIE fabrication precision typically results in good performance and a good match of design to measured performance. Cavity filters for frequencies below about 80 GHz are impractical to make with silicon micromachining because the cavity dimensions are larger than that typically offered by silicon wafers.
In the filter fabrication process, the 4-mil (100 um) SiC wafer carries the high precision metallization features with plated gold and through-wafer vias; and the DRIE silicon subcover wafer forms the gold plated silicon cavities that are up to 40 mils (1mm) deep. In the demonstration design discussed in section III, the cavity was etched to a depth of 15 mil using a silicon dioxide pattern mask. The DRIE utilized a Bosch process [2] in a Tegal 110 plasma etch tool. After silicon dioxide mask removal, the silicon subcover cavities were plated with gold. The filter design follows established techniques [8, 9].

After fabrication and dicing of the Si and SiC wafers, the SiC and the upper and lower silicon subcovers were bonded together using a high accuracy chip bonder to form robust gold-gold thermocompression bonds.

A cartoon diagram of a suspended stripline filter made with this fabrication approach is provided in Figure 2.

C. Test

Our suspended stripline filter designs are terminated in conventional ground-signal-ground pads, similar to those used in MMIC chips, which enables probe testing of each filter and delivery of known-good-die to the next higher level assembly. An example is shown in Figure 3.

The diplexer filter was tested on a wafer probe station. The calibration method was SOLT (Short Open Load Thru) on ISS calibration substrates and the S-par tests were conducted with a Keysight PNA-X N5245A with Ports Power < -10dBm. Data is shown in Section III.

Fig. 3. SEM image of the input probe pad. The filter can be tested with wafer probes, and the RF signal enters the silicon cavity by means of mouse holes, as seen in the SEM image.

D. Electromagnetic Isolation

Compact 50 µm (2-mil) diameter through-wafer vias in the SiC center substrate can be realized with minimal limitations on the quantity of vias. The vias are typically used to form high isolation electromagnetic via fences; and because the vias are small and closely spaced, simulation indicates that they can be used to provide high isolation up to 100 GHz. The via fence and silicon subcover walls allow individual elements of the filter to be put into their own electromagnetically shielded cavities; which minimizes cross-coupling, allows compaction and routing flexibility by means of bending of the transmission lines, and reduces design time spent mitigating undesired effects of cross coupling.

Through-wafer via fences in the SiC also ensure ground continuity for the RF return currents between the top and bottom silicon subcovers and enable on-wafer testing of the filter after fabrication.

E. Discussion

Our approach differs from stripline filters fabricated in circuit board or LTCC in two important ways. First, the highly precise metallization dimensions, the dimensional stability of the hard substrates, and extremely compact through-wafer vias of our SiC chip make our approach repeatable with excellent match of measured performance to modelled performance. Second, the large cross section of the air cavity of the suspended stripline and excellent surface smoothness of the plated gold in the DRIE etched cavity offers a fabrication approach that can provide higher Q than stripline filters in PWB (Printed Wiring Board) or LTCC.

By combining silicon DRIE micromachined cavities with a SiC suspended stripline center conductor, we extend the filter design space to much lower frequencies than previously demonstrated silicon DRIE cavity filter designs [6, 7]. Our approach enables bandpass filtering for frequencies less than 20 GHz to be realized.

F. Repeatability and Manufacturability

In developing and combining the processes described above, we have established initial fabrication tolerances to support new
filter designs as shown in Table 1. Tight fabrication tolerances are critical to first pass design success and to manufacturing repeatability, especially for many precision filters which require tight cut-off specs, high isolation requirements and highly repeatable performance.

Table 1. Fabrication tolerances.

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<tr>
<th></th>
<th>Linewidth</th>
<th>+/- 1 µm (0.04 mils)</th>
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<tr>
<td>Metal thickness</td>
<td>3.5 or 5.5 µm, +/- 0.5 µm</td>
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<tr>
<td>Silicon DRIE cavity precision</td>
<td>Cavity width</td>
<td>+/- 3 µm (0.1 mils)</td>
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<tr>
<td></td>
<td>Cavity depth</td>
<td>Up to 1 mm (40 mil), +/- 10 µm (0.4 mils),</td>
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<td></td>
<td>Alignment of SiC to silicon subcover</td>
<td>+/- 5 µm (0.2 mils)</td>
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III. DIPLEXER FILTER DEMONSTRATION

A. Folded Stripline Diplexer Design

A compact, folded stripline diplexer was designed and fabricated to demonstrate the capabilities of this novel fabrication approach (Figure 4).

Fig. 4. Photo of the diplexer. Two side-by-side diplexers are fabricated on this 16 mm x 16 mm chip.

A total of eight test articles were fabricated, of which seven of the test articles had nearly identical performance, with low loss, high rejection, and high Q. (Figure 5a, 5b).

Fig. 5a. Performance of the suspended diplexer. The plot shows the insertion loss of the lowpass channel and the bandpass channel. The median performance is plotted in dark red, while the performance of the other seven diplexers is shown in light red.

Fig. 5b. The same data as Figure 5a, with the y-axis scaled to show the out-of-band rejection. Again, the performance of the eight diplexers is extremely repeatable, with only one diplexer having slightly different performance.

The diplexer was simulated using Ansys HFSS. Excellent agreement of the measured vs. modeled performance was obtained, as shown in Figure 6.

Fig. 6. The diplexer is modeled using Ansys HFSS (blue lines) and is compared to the median of the measured lowpass and bandpass channels (red lines).

B. Filter Robustness

The diplexer was tested at multiple temperatures and showed very small variation with temperature of 0.0013 dB per °C at 15 GHz, as shown in Figure 7. The material properties of the SiC center conductor chip change very little with temperature so frequency response variation with temperature is roughly 3x lower than similar alumina filters. Three diplexers were subjected to 25 temperature cycles from -40 °C to 120 °C and show no change in electrical performance. These initial tests indicate excellent mechanical robustness which is attributed to the well matched coefficient of thermal expansion between SiC and silicon.
Figure 7: $S_{21}$ Mag S-parameter data from one diplexer, tested at 23, 53, and 83 °C. The insertion loss at 15 GHz increased by 0.08 dB as the test temperature was elevated from 23 to 83 °C. Legend: light blue: 23 °C; dark blue: 53 °C; magenta: 83 °C.

IV. CONCLUSION

We have developed and demonstrated a novel and practical fabrication method for compact and high performance filters. This method embodies the following benefits:

High Q: The SiC suspended stripline offers a large cross section primarily composed of air, which enables the design of stripline filters with high Q.

Repeatability: Reproducible precision MMIC processes and heterogeneous integration of die with micron scale placement accuracy using high strength gold-gold bonds provides outstanding electrical test repeatability.

Stable over Temperature: The frequency response variation with temperature of SiC is roughly 3x lower than similar alumina filters.

Compaction: This manufacturing approach offers the possibility of reducing the filter area since the isolation provided by the channel wall allows for aggressive bending and compaction.

Mechanically Robust: The SiC inner core is closely matched in CTE to the silicon micromachined cavities which greatly reduces mechanical strain during temperature cycling.

Low cost mass production. Production can be scaled in volume and wafer size in the same manner as microelectronics wafer processing technology.

Known Good Die: Assembled filters can be designed for probe testing before delivery to the next higher level assembly.

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