A 20.8-41.6-GHz Transformer-Based Wideband Power Amplifier with 20.4-dB Peak Gain Using 0.9-V 28-nm CMOS Process

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Abstract—This paper presents a wideband transformer-based power amplifier applicable for the millimeter-wave (MMW) fifth generation (5G) mobile communication. The proposed power amplifier is manufactured in 28-nm HPC-plus CMOS process. The power stage and driver stage amplifiers are biased in deep class-AB to reduce the dc power dissipation in the linear power region and provide a linear operation close to the saturated output power (P_{sat}) of the PA. In the output matching network, a transformer with two coupled resonant capacitors is designed for broadband power matching. The proposed PA achieves the peak small-signal power gain (G_p) of 20.4-dB at 23 GHz and a measured 3dB small-signal gain bandwidth (BW_{sat}) from 20.8 to 41.6 GHz covering the multiple 5G bands with only 39.6-mW quiescent power consumption. The measured P_{sat} is 16.1-dBm at 30 GHz with over 50% P_{sat} output power 1dB bandwidth (BW_{1dB}) from 23 to 38.5-GHz. Also, this PA reports a 35% peak power added efficiency (PAE_{MAX}) at 25 GHz and a 13-dBm peak OP_{1dB} at 41 GHz. In the 64-QAM OFDM modulated signal measurement, this power amplifier obtains an output power of 7.2/6.9-dBm and a modulated PAE of 8.5%/8.8% at 23 and 41-GHz respectively when keeping the EVM below -25 dBc.

Keywords—power amplifier, wideband, transformer, CMOS integrated circuits, 5G mobile communication.

I. INTRODUCTION

With the continuous growth of fifth-generation (5G) mobile communication, a wide number of millimeter-wave (MMW) frequency bands from 24 to 43 GHz have become crucial in meeting the demand for higher data-rate transmission [1]. Therefore, wideband power amplifiers supporting multiple 5G channels are suitable in MMW transmitter modules, allowing significant flexibility for spectrum utilization while simplifying the assembly process for multi-band transmitters. Several circuit and system designs for the wide MMW frequency band have been demonstrated recently [2]–[9].

For 5G mobile communication, since the transmitter system usually consists of many modules, the power consumption of each component is critical for prolonging battery lifetime [10]. Power amplifiers comprise most of the power consumed in the transmitter system, therefore reducing the utility power consumption and heat dissipation of a power amplifier is essential.

In this paper, a wideband transformer-based power amplifier with saturated output power (P_{sat}) 1dB bandwidth (BW_{1dB}) across 23 to 38.5 GHz with only 39.6 quiescent power consumption is proposed. Two coupled resonant capacitors are added in the output stage to achieve broadband power matching while optimized transistor sizes are chosen to deliver a peak P_{sat} of 16.1 dBm at 30 GHz and 35% peak power added efficiency (PAE_{MAX}) at 25 GHz.

II. CIRCUIT DESIGN

The circuit diagram of the proposed power amplifier is shown in Fig. 1. The PA is realized with a two-stage differential structure. Each stage consists of a common source differential pair with neutralization capacitors to improve stability, power gain (G_p), output power and reverse isolation [10]. The capacitive neutralization using a metal 4 to metal 9 interdigital structure allows for a more compact layout. The total width of the power stage is 384 μm divided into twelve unit cells. Each transistor cell is composed of finger width of 32 fingers with a finger width of 1μm to reduce the parasitic gate resistance then obtaining higher gain and power added efficiency (PAE). To achieve a lower quiescent dc power dissipation and obtain linear operation close to P_{sat}, a deep-class AB bias is applied to both stages [10],[11]. The bias points of the driver stage and power stage amplifier are shown in Fig. 2. The overall quiescent dc power consumption is only 39.6-mW. Also, the third-order derivative transconductance (g_{mn}) is close to zero to ensure the linearity of the power amplifier.

In the output power matching, the load impedance needs to be transformed to the PA differential optimal output impedance (Z_{opt}) which is equal to 7.7 + j12.8 Ω at 39 GHz. The transformer with two coupled resonant capacitors is designed for broadband power matching as shown in Fig. 3. One coupled resonant capacitor is designed according to output signal pad (C_{pad} = 47 fF) while the other one is designed from the output capacitance of the power stage transistors (C_{parasitic} = 477 fF). The total power transmission loss in the output matching network is only 1.2-dB from 22.5 to 39 GHz. The return loss is more than 15-dB from 23 to 50 GHz as shown in Fig. 4. (a). Also, the broadband output matching impedance on the smith chart can be observed in Fig. 4(b). The proposed power
matching network has a high area utilization efficiency and a low matching loss for broadband matching.

In order to maintain the linearity without power distortion and avoid the additional PAE drop due to the inter-stage matching, the size of the driver stage amplifier has to be carefully chosen to be between a half and one third of the size of power stage amplifier. The input and inter-stage matching are also designed using transformer matching to obtain a high area utilization efficiency and broadband matching. In addition to the design of the matching network and device core, the common mode stability is also a critical issue for the power amplifier design. To avoid the common mode oscillation, the gate bypass network consists of a 20-Ω resistor and a 0.77-pF MOM capacitor.

![Fig. 2. Transconductance analysis of a common source NMOS device with 32 fingers and a finger width of 1 μm.](image)

**III. MEASUREMENT RESULTS**

The proposed PA is manufactured in 1P9M 28-nm bulk CMOS process with ultra-thick top metal (UTM), and the chip micrograph is shown in Fig. 5. The core area is 0.1 mm² (500μm x 200μm) excluding the input/output RF pads and the bypass capacitors. The measurement results are performed using on-wafer probing. The RF input and output pads are examined by GSG probes while the PGPPGP probes are used for the dc pads placed on the top and bottom of the chip. An Agilent E8361A vector network analyzer (VNA) is used to measure the PA’s small-signal characteristic. The quiescent power dissipation is 39.6-mW when the gate biases of the driver and power stages are set to 0.38 V and 0.32 V, respectively, with a supply voltage of 0.9 V. The same bias statuses are applied to the large-signal measurement. The small-signal simulation and measurement results are illustrated in Fig. 6. The 3-dB gain bandwidth is approximately 66.7% (20.8 to 41.6 GHz), and the peak small-signal power gain (G_p) is 20.4-dB at 23 GHz.

![Fig. 3. Transformer layout of the output network.](image)

Fig. 4. (a) Return loss of the output matching network when Z_{in} equals to Z_{opt}*, and (b) output matching impedance on smith chart from 20 to 50 GHz.

![Fig. 6. Measured and simulated S-parameters of the proposed PA.](image)

The large-signal continuous-wave (CW) is measured through a Keysight E8267D signal generator (SG) and a Keysight N9030B signal analyzer (SA). Fig. 7 shows the single-tone simulated and measured CW large-signal
characteristics at 23, 25, 30, and 41 GHz, respectively. The proposed PA reaches 30.1% $PAE_{\text{MAX}}$, 15.1-dBm $P_{\text{sat}}$ and 12.4-dBm $OP_{1\text{dB}}$ with 20.4-dB $G_p$ at 23 GHz. The PA obtains 35.3% $PAE_{\text{MAX}}$, 15.5-dBm $P_{\text{sat}}$ and 12.7-dBm $OP_{1\text{dB}}$ with 19.9-dB $G_p$ at 25 GHz. The PA achieves 28.8% $PAE_{\text{MAX}}$, 16.1-dBm $P_{\text{sat}}$ and 9.8-dBm $OP_{1\text{dB}}$ with 17.8-dB $G_p$ at 30 GHz. The PA attains 26.2% $PAE_{\text{MAX}}$, 14.7-dBm $P_{\text{sat}}$ and 13-dBm $OP_{1\text{dB}}$ with 17.6-dB $G_p$ at 41 GHz. Fig. 8 presents the measured $P_{\text{out}}/PAE_{\text{MAX}}$ summary versus carrier frequency. As shown in the figure, the $PAE_{\text{MAX}}$ of the PA stays above 25% from 22 to 41 GHz (60.3% bandwidth) while achieving 35.2% $PAE_{\text{MAX}}$ at 25GHz. Also, the proposed PA reports 50.4% $P_{\text{sat}}$ output power $BW_{1\text{dB}}$ from 23 to 38.5 GHz.

![Image](fig7.png)

**Fig. 7.** Measured CW large-signal characteristics of the proposed PA at (a) 23GHz, (b) 25GHz, (c) 30GHz, and (d) 41 GHz, respectively.

![Image](fig8.png)

**Fig. 8.** Measured CW large-signal $P_{\text{out}}/PAE_{\text{MAX}}$ versus carrier frequency.

The baseband modulated signal is generated with an Agilent M9505A arbitrary waveform generator (AWG), then up-converted to RF signals with a Keysight E8267D SG. After being amplified, the signals are demodulated with a Keysight N9030B SA. The PA was tested by applying a 64-QAM OFDM modulated signal of 9.7-dB PAPR for a 100-MHz channel bandwidth. The measured modulation results of the proposed PA at the carrier frequencies ($f_{\text{carrier}}$) of 24 and 38 GHz are presented in Fig. 9. and Fig.10. Under an EVM of $-25$ dBc, the average $P_{\text{out}}/PAE$ at 23 and 41 GHz are achieved 7.2 dBm/8.5% and 6.9 dBm/8.8%, respectively.

![Image](fig9.png)

**Fig. 9.** Measured 64-QAM OFDM (a) output spectrum and (b) constellation at 23 GHz for a 0.9-V supply at $P_{\text{sat}} = 7.2$ dBm, achieving 8.5% PAE under EVM of $-25$ dBc.

![Image](fig10.png)

**Fig. 10.** Measured 64-QAM OFDM (a) output spectrum and (b) constellation at 41 GHz for a 0.9-V supply at $P_{\text{sat}} = 6.9$ dBm, achieving 8.8% PAE under EVM of $-25$ dBc.

Table 1 summarizes the measured performance of this design and compares it with state-of-the-art 5G mm-wave silicon-based PAs. The proposed wideband PA achieves the widest small-signal 3dB bandwidth of 66.7% and can provide a maximum gain of 20-dB to compensate the MMW package loss, as demonstrated in [5], [6]. Under the same supply voltage condition, the designed PA provides higher $PAE_{\text{MAX}}$ than the PA reported in [6] within the frequency band of 24 to 43 GHz. The PA utilizes a small core area of only 0.1mm$^2$, thus providing a compact layout design.

**IV. CONCLUSION**

In this paper, a wideband power amplifier is presented for the 5G mobile communication in 28-nm HPC-plus CMOS process. An output transformer with two resonant coupling capacitors is introduced to achieve broadband output matching. By biasing in deep class-AB for both stages, the PA obtains the peak small-signal power gain of 20.4-dB at 23 GHz and a 3-dB power gain bandwidth from 20.8 to 41.6 GHz with only 39.6-mW quiescent power dissipation. In addition, the designed PA achieves $PAE_{\text{MAX}}$ of 35% at 25 GHz, peak $P_{\text{sat}}$ of 16.1-dBm at 30 GHz with $P_{\text{sat}}$ 1dB bandwidth of 50.4% across 23 to 38.5 GHz. When measured with a 64-QAM OFDM modulated signal, this power amplifier provides an output power of 7.2/6.9-dBm and modulated PAE of 8.5%/8.8% at 23 and 41-GHz, respectively, while maintaining an EVM better than $-25$ dBc. The proposed PA provides an attractive small signal $BW_{1\text{dB}}$ from 20.8 to 41.6 GHz (66.7%) with an acceptable $PAE_{\text{MAX}}$ and with only 39.6-mW quiescent power dissipation under a 0.9-V supply voltage.
Table 1. Comparison table of the recently published 5G mm-wave Si-based power amplifiers

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<td>25-35</td>
<td>33-41</td>
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<td>22.5-32</td>
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*estimated from figures.

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