Balancing Tradeoffs

Taming Signal Integrity Challenges in Millimeter Wave Antenna-to-Bits Implementations

IMS San Diego | June 15, 2023

R&S

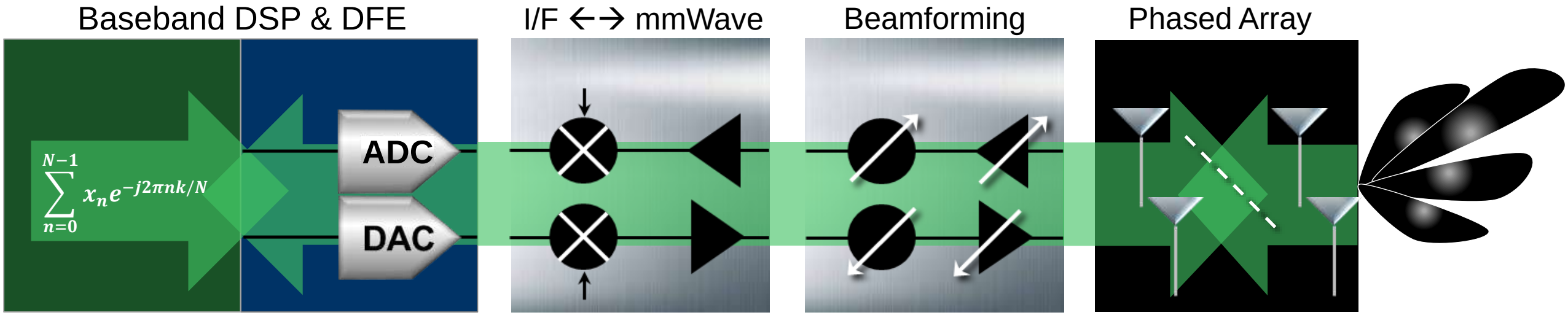
samtec

MathWorks®

AVNET

OTAVA

mmWave Phased Array from Digital to RF



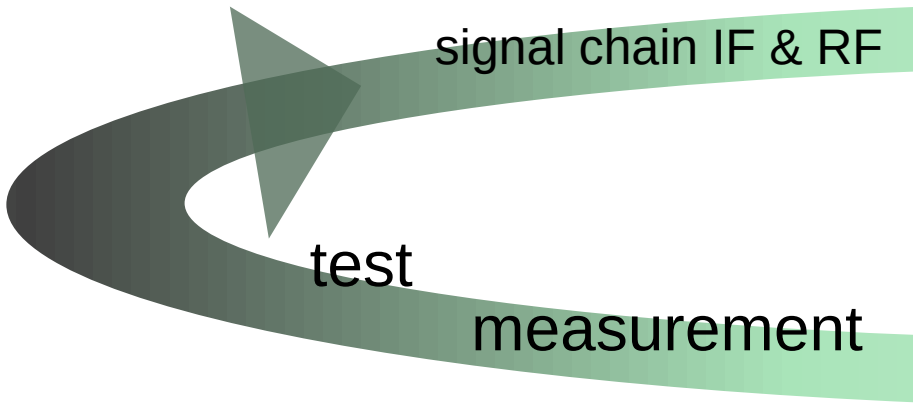
Luc Langlois — AVNET
Director, Advanced Applications / 5G

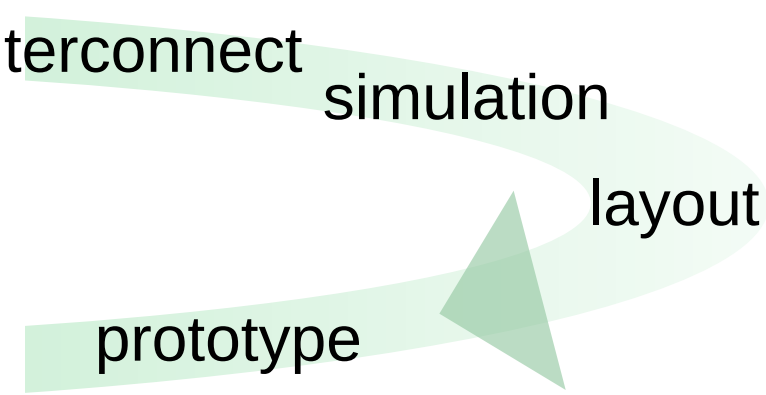
Wen Zheng — OTAVA
VP Engineering

Matt Burns — samtec
Technical Marketing Manager

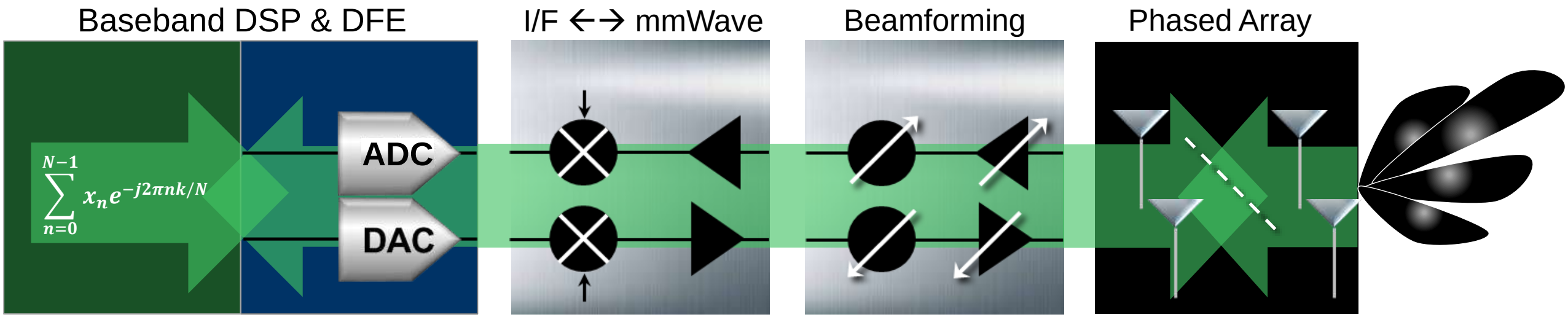
Giorgia Zucchelli — MathWorks
Product Manager RF& AMS

Markus Lörner
Market Segment Manager
RF components





mmWave Phased Array from Digital to RF



Mission: Create a versatile mmWave phased array development system with unified design flow from digital to RF serving a multi-disciplinary team.

Main themes

- Signal integrity within the signal chain from baseband to RF
- Combining RF hardware measurements with MATLAB behavioral models
- Test & measurement techniques

AVNET

Phased Array $80 Billion Addressable Market

5G Millimeter Wave
TAM: $23B, 2026[1]

Modular Phased Array

5G Non-Terrestrial
Communications: $36B, 2028[2]

Automotive Radar
TAM: $11B, 2028[3]

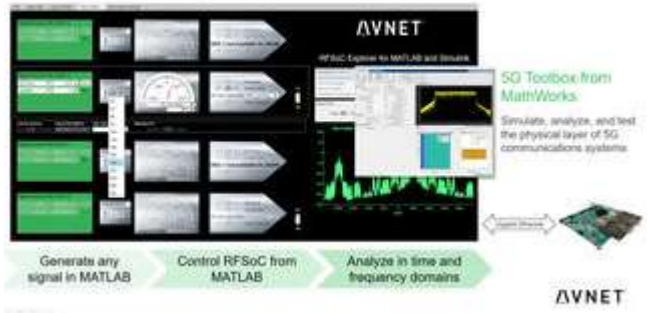
Cost, Power → EIRP

Defense RF Electronics
TAM: $14B[4]

© Otava Inc, 2021

ANTENNA TO BITS REFERENCE CHAIN

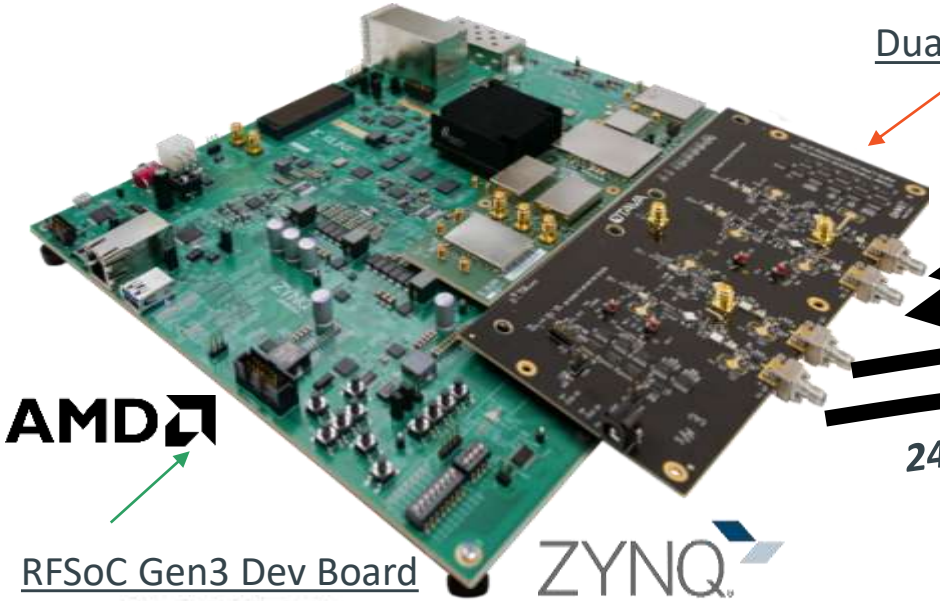
Avnet RFSoC Explorer with MATLAB and Simulink



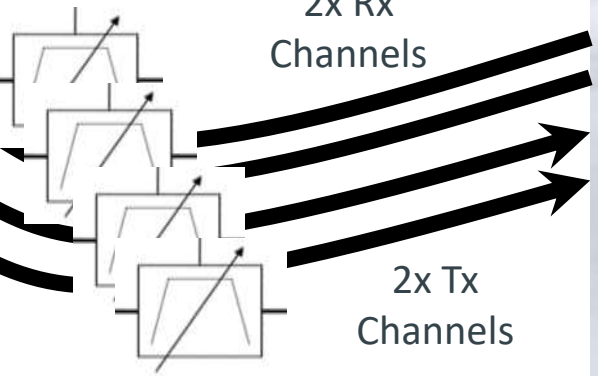
Existing software platform to be expanded to include beamforming algorithms and weight functions for array control

OTFL301, Tunable Filter
24-40GHz

Dual Transceiver Board
19-31 GHz



RFSoC Gen3 Dev Board



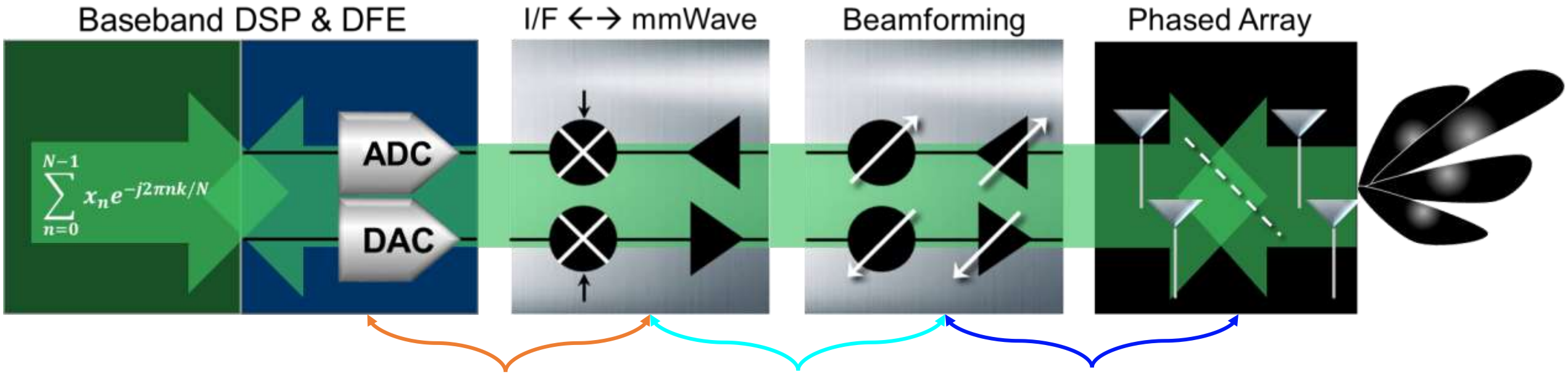
PAAM

Designed to Complement AMD's RFSoC with Otava's Products -> A Complete Antenna to Bits Reference Hardware Chain

© Otava Inc, 2021

ANTENNA TO BITS SOLUTIONS

From mmWave to Baseband



Baseband Digital Front-end (DFE) ⟷ Mid Band Tunable Filters ⟷ Higher Band Tunable Filters ⟷ Higher Band T/R Switches ⟷ Over the Air

A signal's long journey to maintain integrity through complicated systems

- Consist of many elements
- Mixed of different frequencies
- Many ways of configuration

- Interconnect between elements
- mmWave design sensitivity
- Frequency conversion

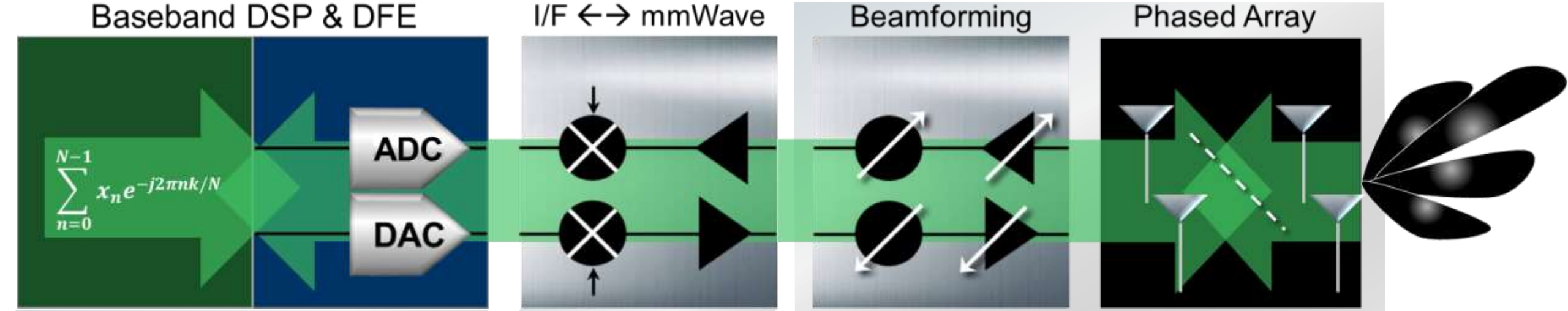
- Interference
- Thermal issue
- Digital control
- Bandwidth limitation

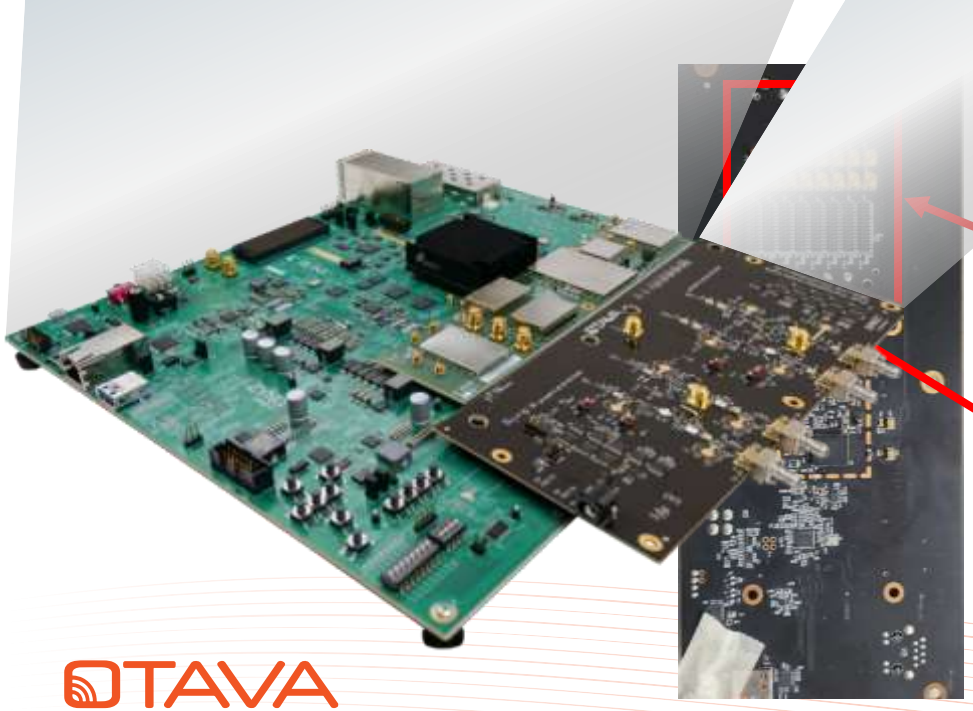
OTAVA

© Otava Inc, 2021

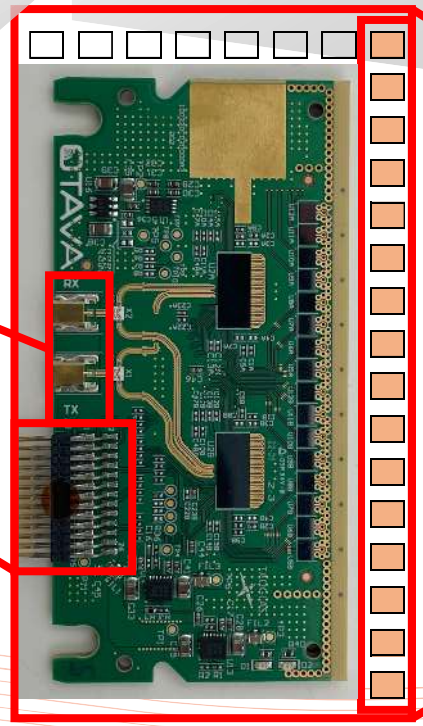
ANTENNA TO BITS HARDWARE COMPONENTS

From mmWave to Baseband

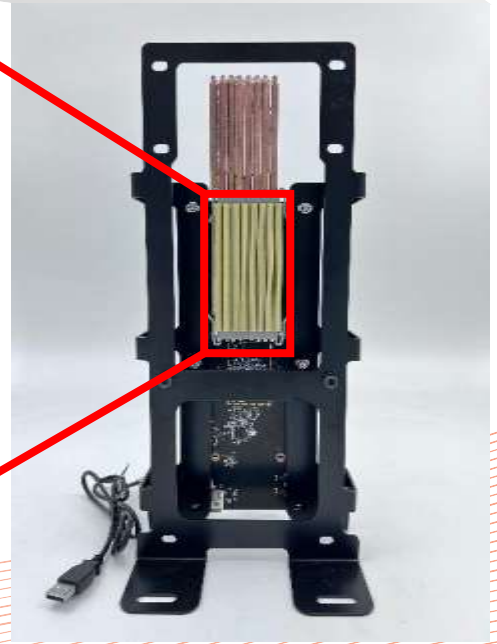




8 Linecards to the Combiner Card



8x16 Array



BALANCING TRADEOFFS: TAMING SIGNAL INTEGRITY CHALLENGES IN MMWAVE ANTENNA-TO-BITS IMPLEMENTATIONS

24-30 GHZ PHASED ARRAY ANTENNA MODULE (PAAM) OVERVIEW

Wen Zheng

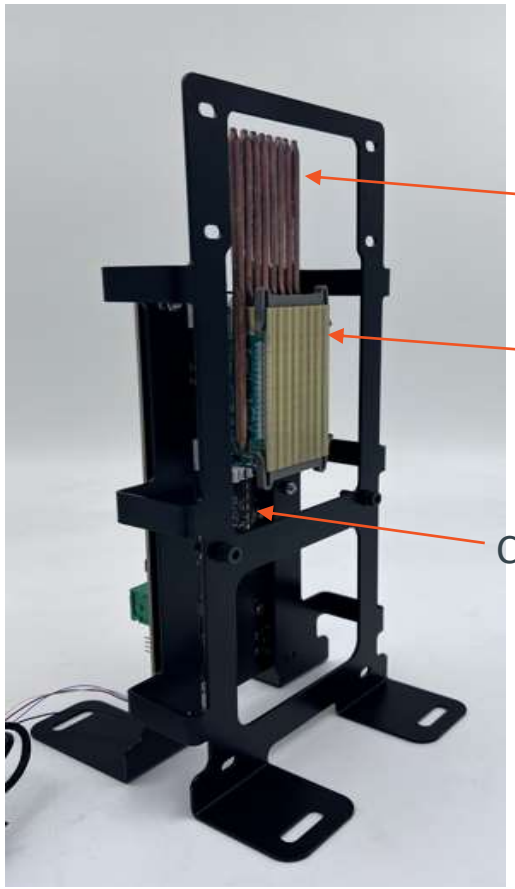
VP of Engineering

Otava, Inc.

© Otava Inc, 2021

PHASED ARRAY ANTENNA MODULE (PAAM) OVERVIEW

PAAM



PAAM
(Front Cover Removed)

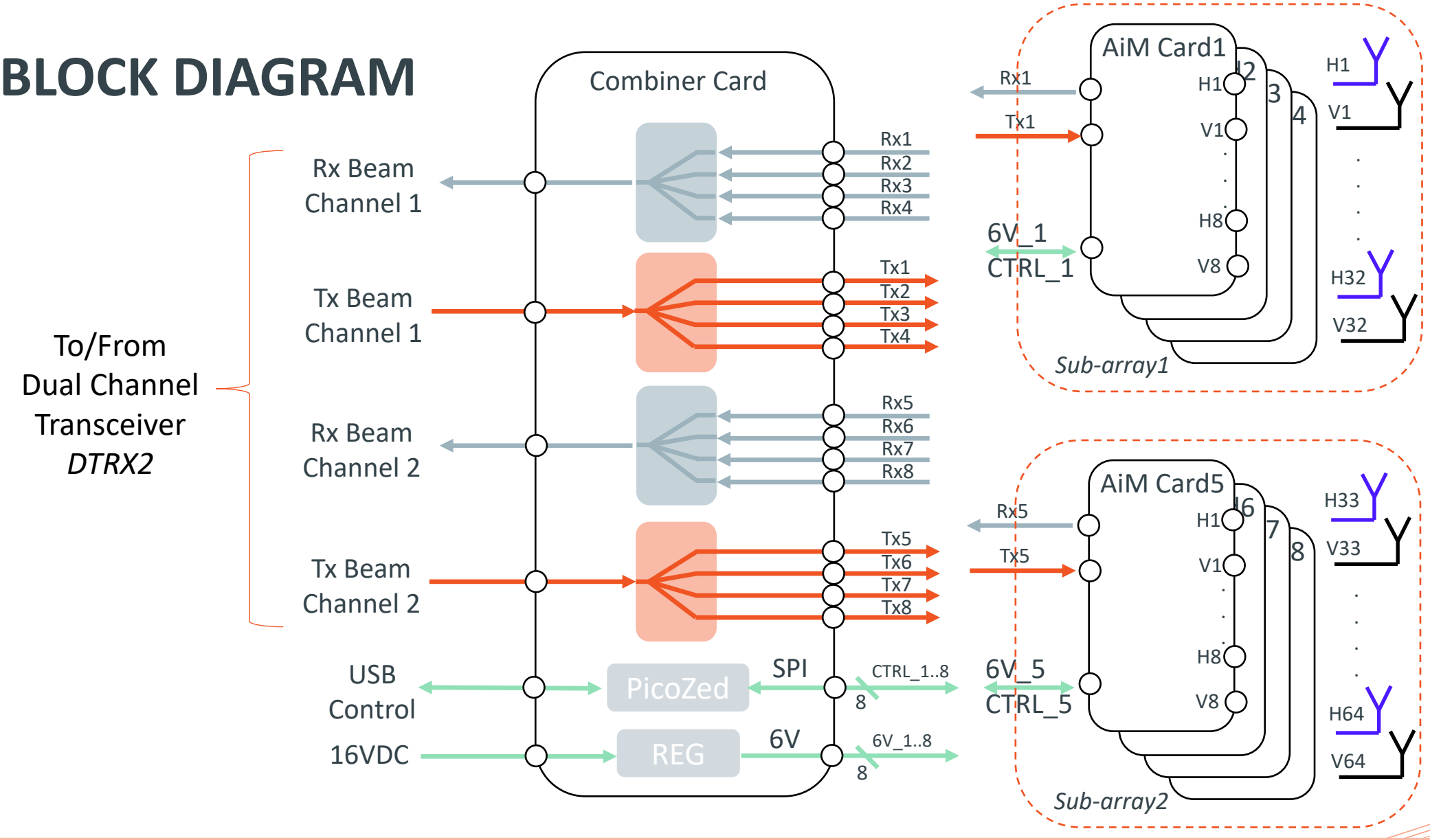
Array Specifications

Parameter	Value
Frequency of Operation	24-30 GHz
Configuration	8x8, 64-Element Dual Polarization
Azimuth Scan	+/-45 Degrees
Elevation Scan	+/- 15 Degrees
EIRP	+47dBm +40dBm (low power mode)
DC Voltage Input	16V
Control Interface	USB (BFIC SPI up to 350MHz)

The Only Wideband PAAM in the Market with Dual Polarization for 5G & Defense Applications

© Otava Inc, 2021

PAAM BLOCK DIAGRAM



Scalable Slat Array Configurations Enables Hybrid Beamforming Architectures & Performance Customization

© Otava Inc, 2021

ANTENNA IN MODULE (AIM) CARD DESIGN

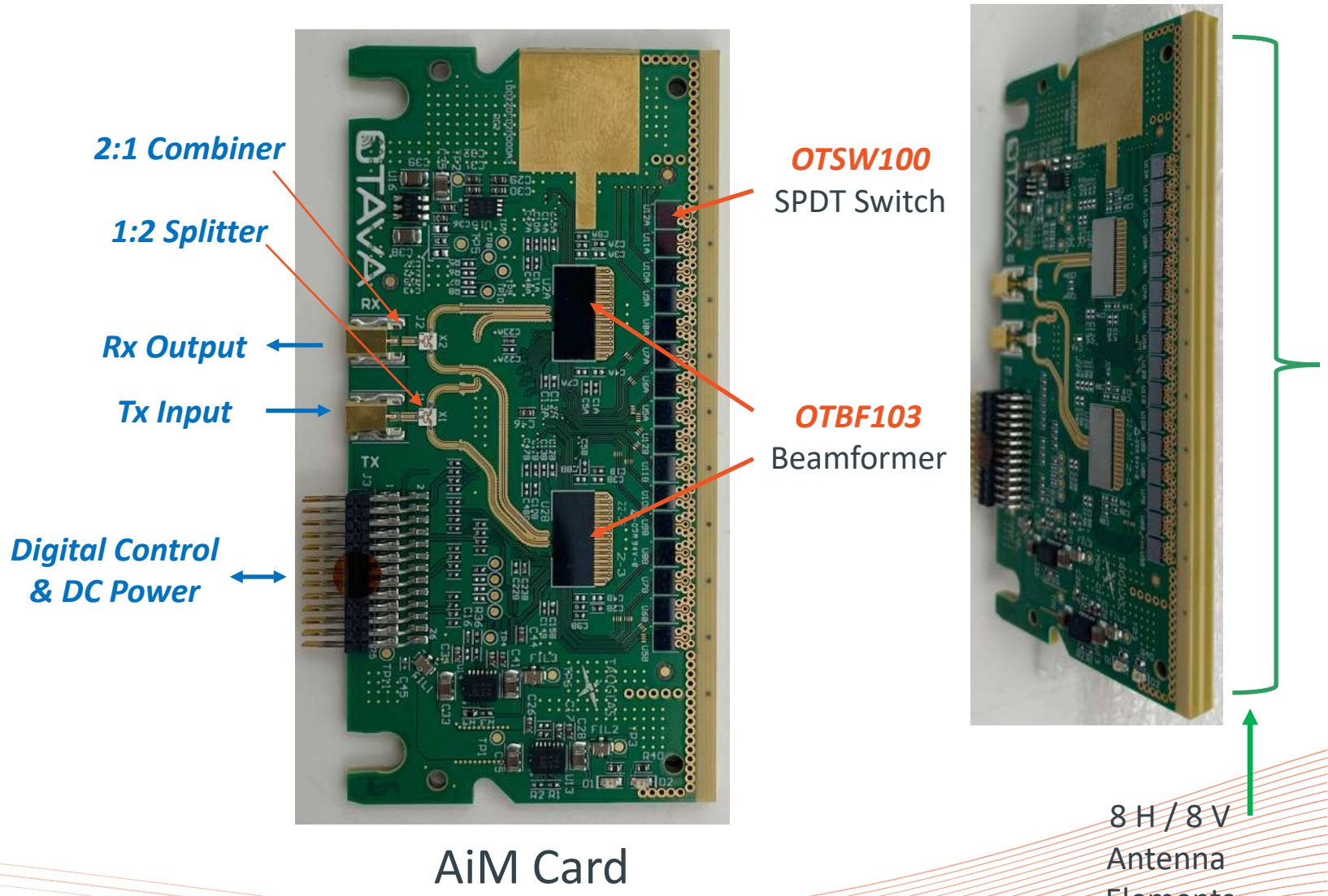
8x AiM Cards in the array

- 64 H-Pol Elements Total
- 64 V-Pol Elements Total

AiM Card Design Includes:

- 2x Otava 24-40GHz Beamformer IC, ***OTBF103***
- 16x Otava DC-40GHz SPDT Switch, ***OTSW100***
- Integrated 8H / 8V antenna element design
- 6VDC input + integrated LDO power regulation

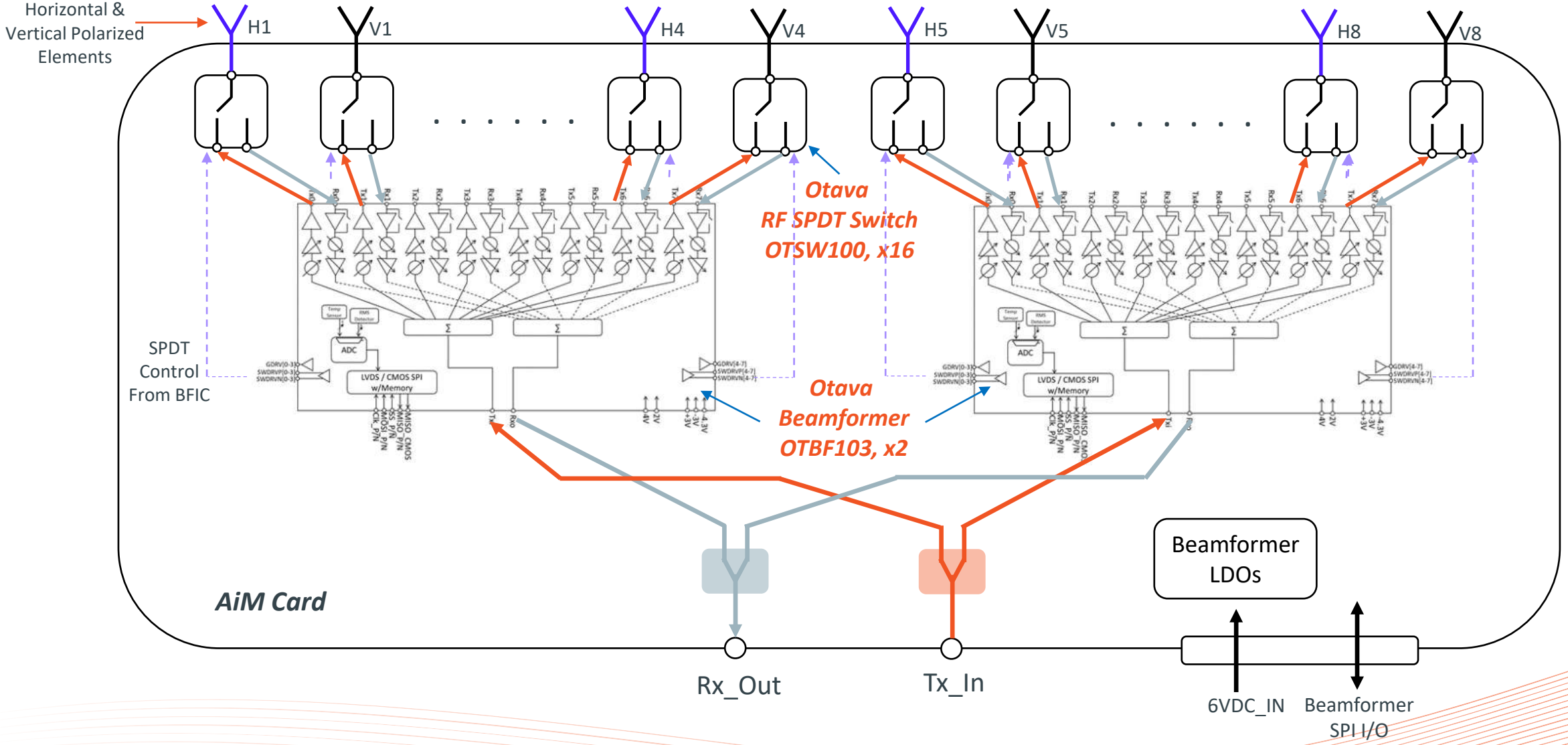
Scalable Building Block of Phased Array System



AiM Card

© Otava Inc, 2021

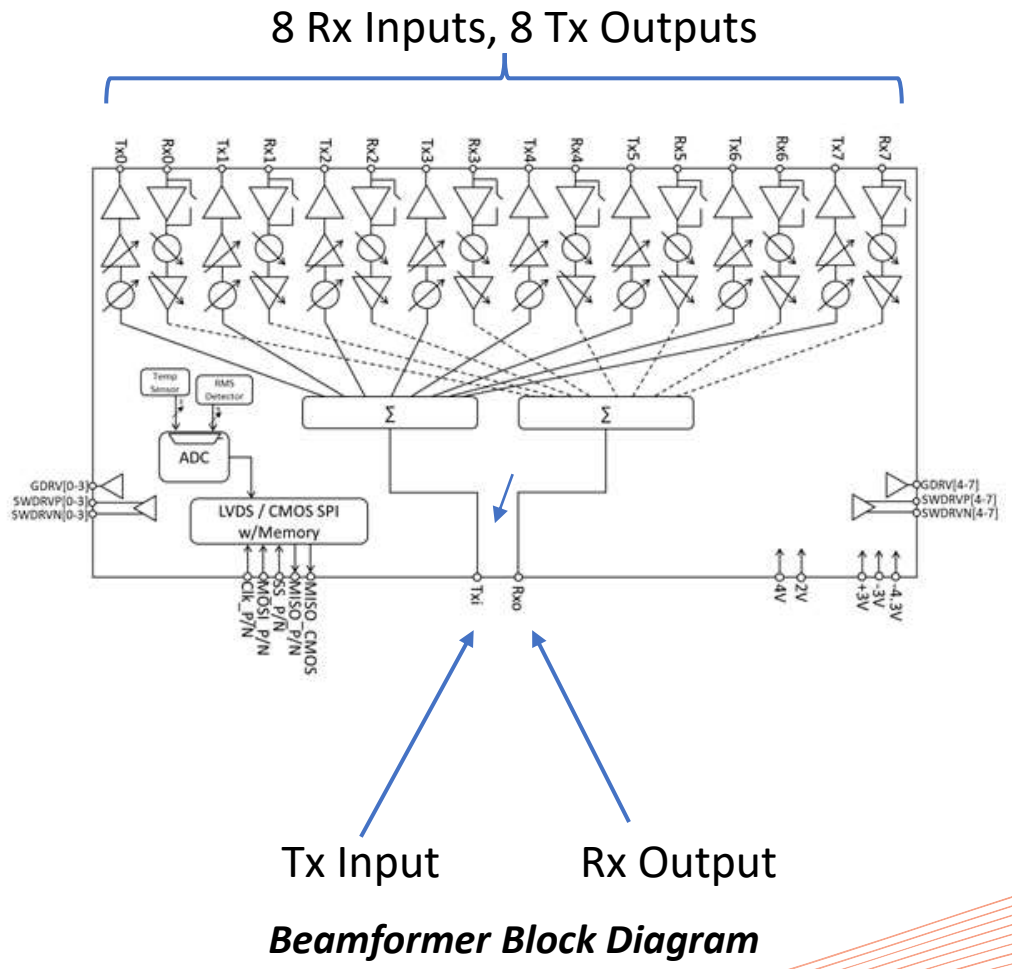
AIM CARD BLOCK DIAGRAM



© Otava Inc, 2021

WIDEBAND 24-40GHZ TDD BEAMFORMING RFIC *OTBF103*

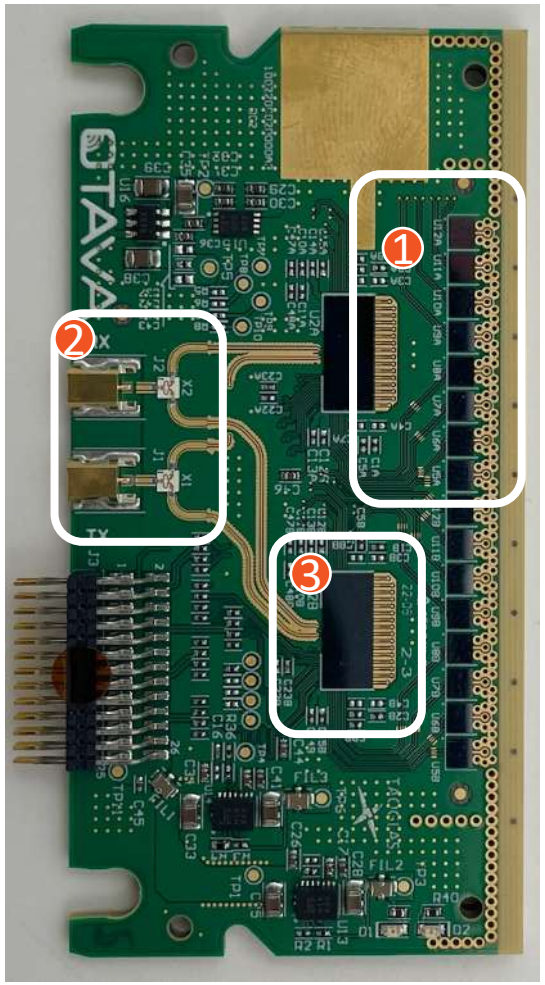
- 24-40GHz mmW Design (covers n257, n258, n260, n261 5G NR bands, LEO Satellite, Defense)
  - 8 Rx Inputs to 1 Rx Output
  - 8 Tx Outputs from 1 Tx Input
  - Independent VGA control (20dB range, 0.5dB step)
  - Independent Phase control (360deg coverage, 5.6deg step)
- Analog Content
  - Temp Sensor / RMS Power Detector capability
  - External Gate Driver operates from -4.3 to +0.3V (x8)
  - External T/R Switch Driver provides +3 and -3V outputs (x8)
- 4-wire Digital SPI Design (LVDS/CMOS Control)
  - SPI operation up to 350MHz for fast on the fly switching of all parameters
  - Integrated memory for fast beam switching (64 states)
- Die Size: 9.8 x 4.2mm, flip chip



Beamformer Block Diagram

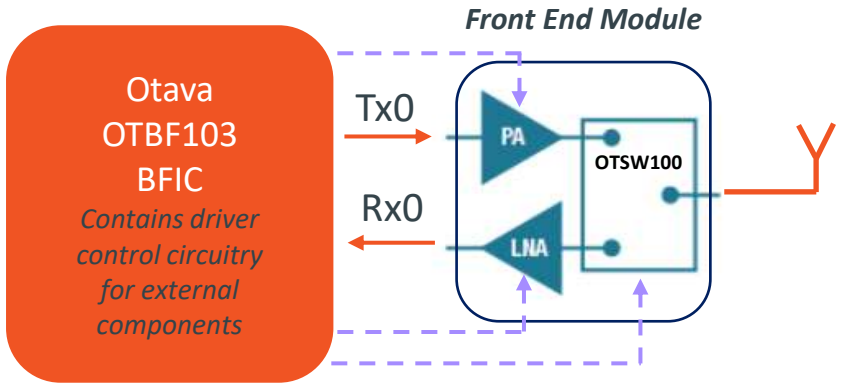
© Otava Inc, 2021

AIM CARD FUTURE CAPABILITIES



1 – **Modified Front End Configuration for Higher Performance**

- Insert optional III-V front end components between BFIC and Element
- Tradeoff between EIRP of array, power consumption, thermal, array size, etc



- Higher Pout per Element (w/PA)
- Lower NF per Element (w/LNA)
- Can delete switch for a Rx only or Tx only array

2 – **Remove combiner/splitter to increase # of Beams**

- 2 Tx or 2 Rx as an example

3 - **Number of BFICs**

- Reduce or scale up # of BFICs/Elements to support system performance goals
- More or less beams per board

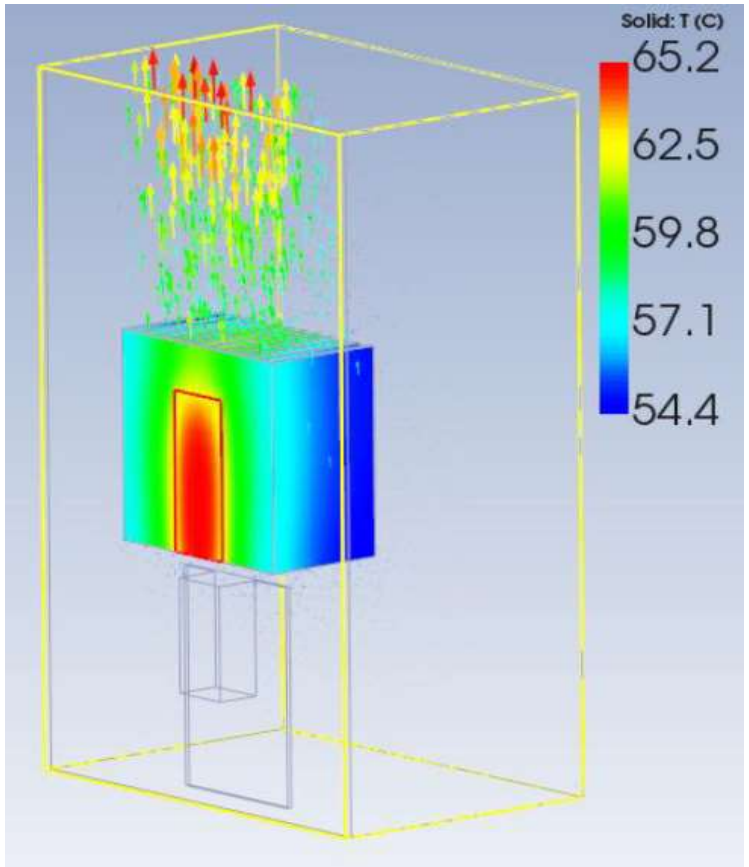
Flexible Architecture Design: Provides Design Options to Address Different System Needs

© Otava Inc, 2021

THERMAL SOLUTION

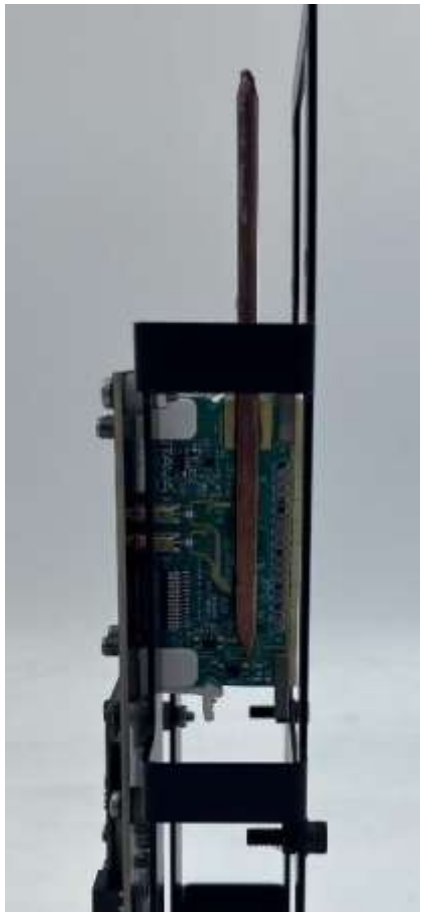
- Fully passive cooling
- Reduce the array temperature from 125C to 75C

CFD Analysis

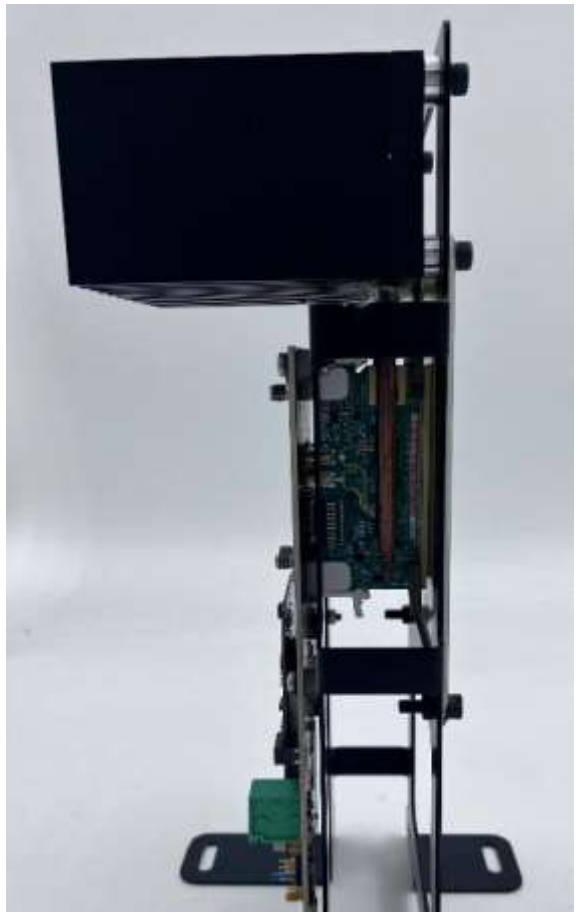


Vertical

Without Heatsink



With Heatsink



Proof of concept: heat pipe solution can effectively cool BFICs in the slat array

© Otava Inc, 2021

COMBINER CARD DESIGN

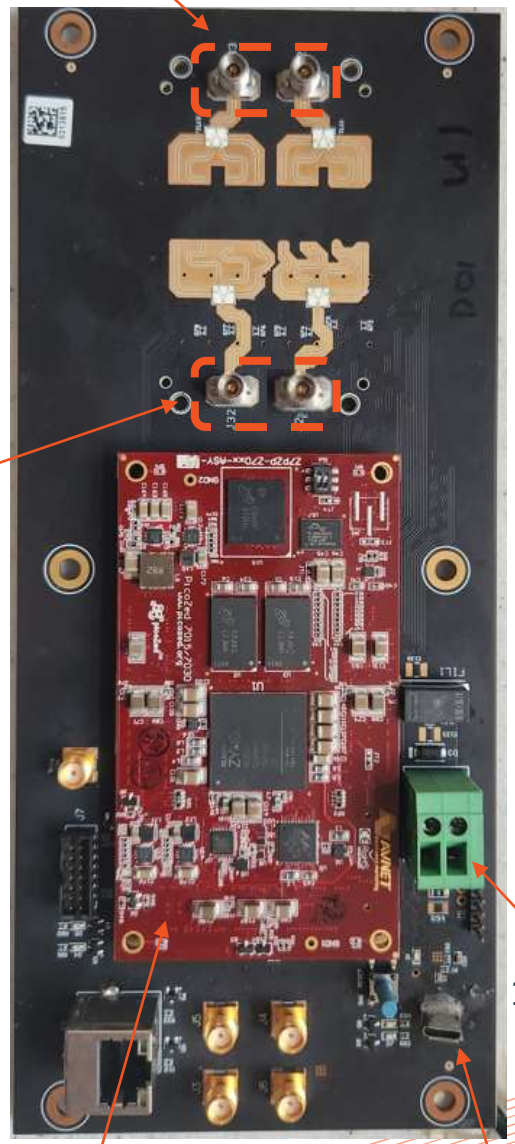
1x Combiner Card in the array

Design Features:

- Combines 8 Rx Beams to 2 Rx Beam outputs -> 2x 4:1 combining sections
- Splits 2 Tx input Beams into 8 Tx Beams -> 2x 1:4 splitting sections
- Functions as the backplane & provides power and control to AiM Cards
  - Avnet PicoZed SOM Digital Controller
  - 16VDC input + integrated LDO regulation
- All connectors are provided by Samtec

Build in digital kit and software GUI: Ready for Evaluation Out of the Box -> Reducing Customer's Development Time

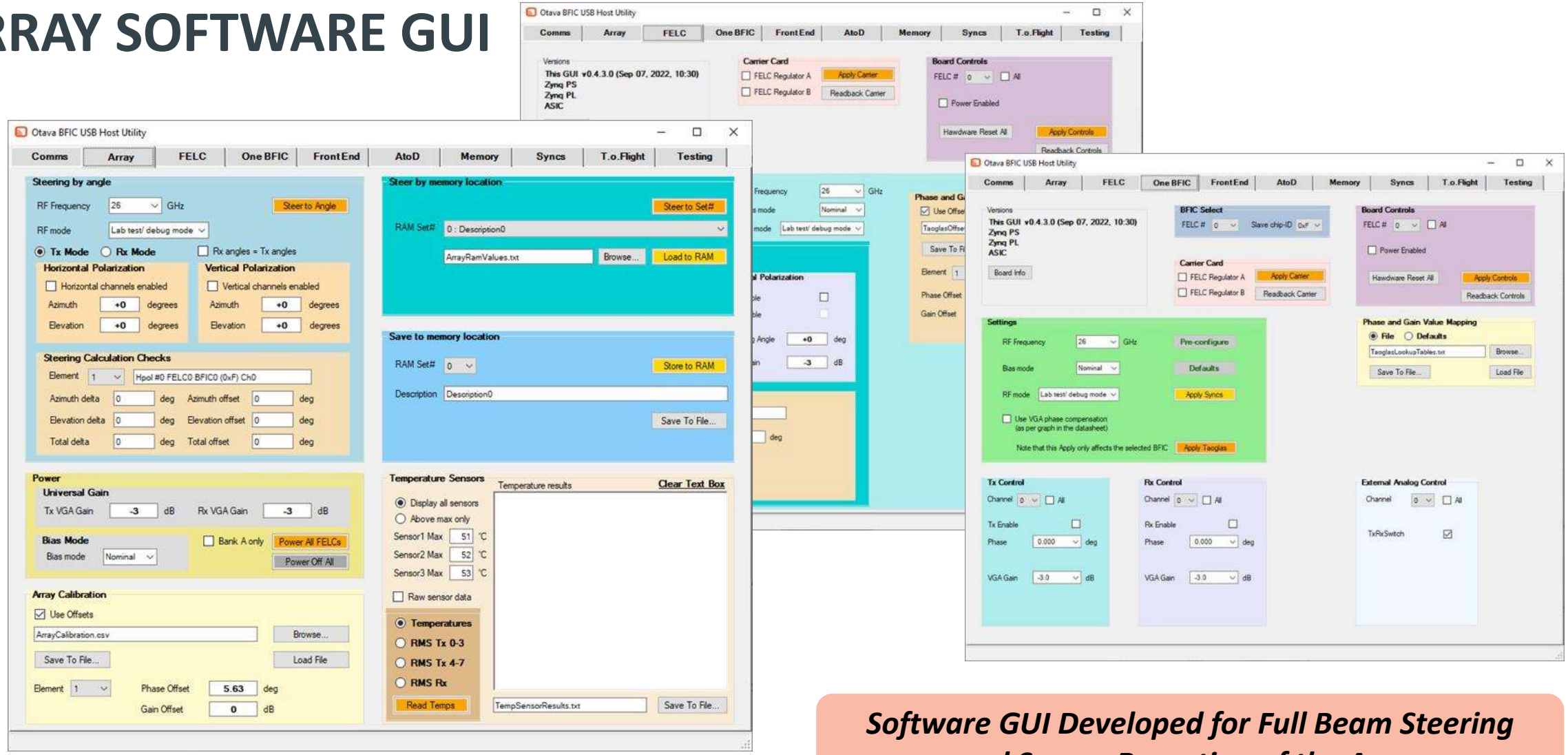
(Front)



(Back)

© Otava Inc, 2021

ARRAY SOFTWARE GUI

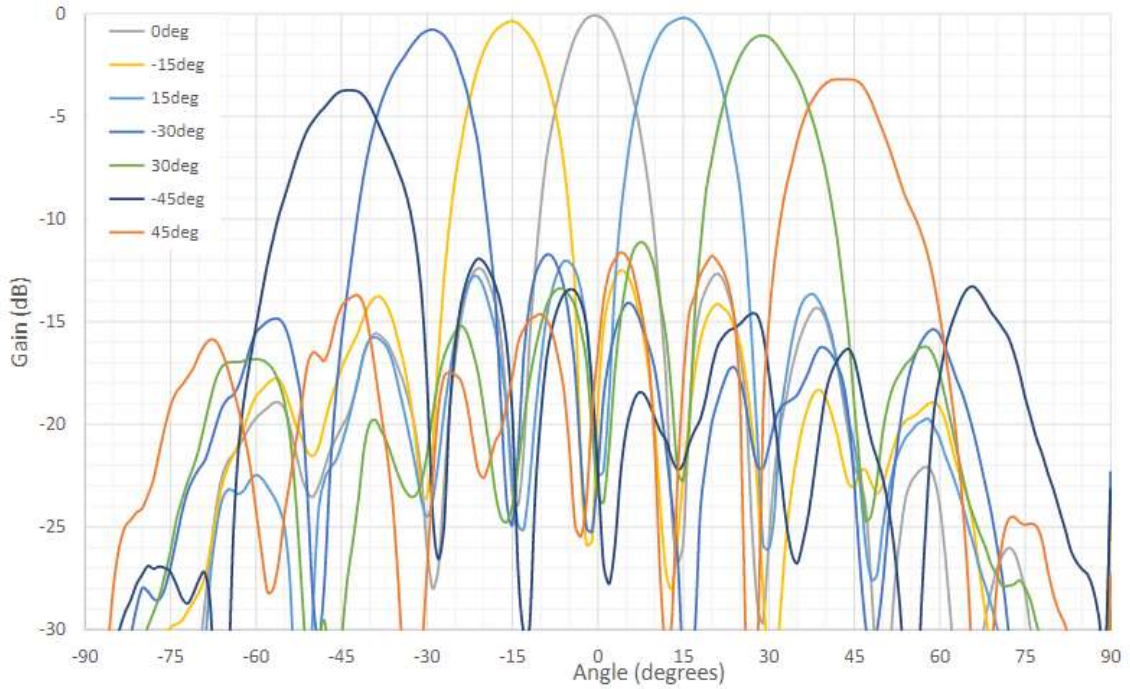


Software GUI Developed for Full Beam Steering and Sensor Reporting of the Array

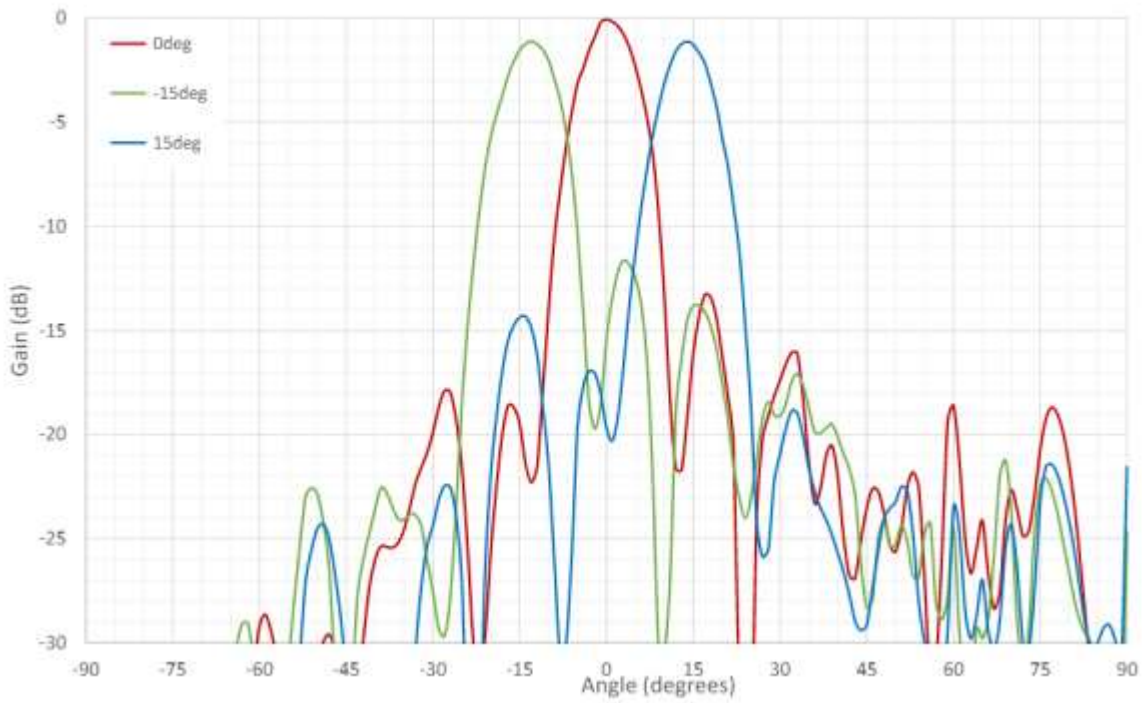
© Otava Inc, 2021

TRANSMIT ANTENNA SCAN PATTERNS, H-POLARIZATION

28GHz Azimuth Scan, +/- 45 degrees



28GHz Elevation Scan, +/- 15 degrees

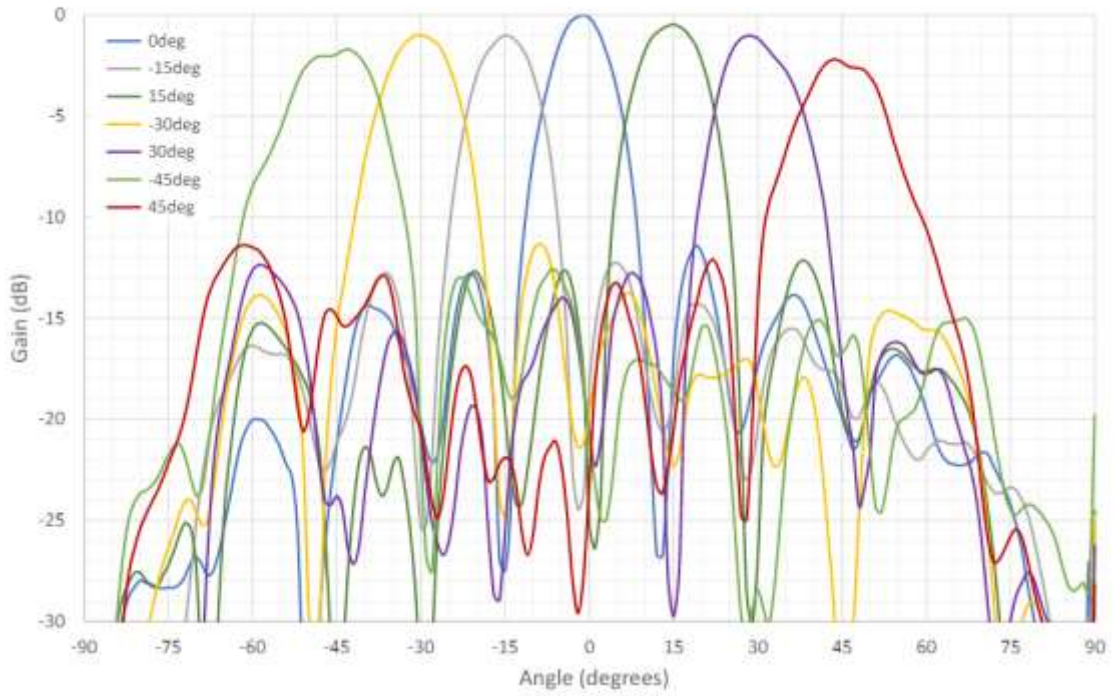


Robust Measured Scan Angle Performance

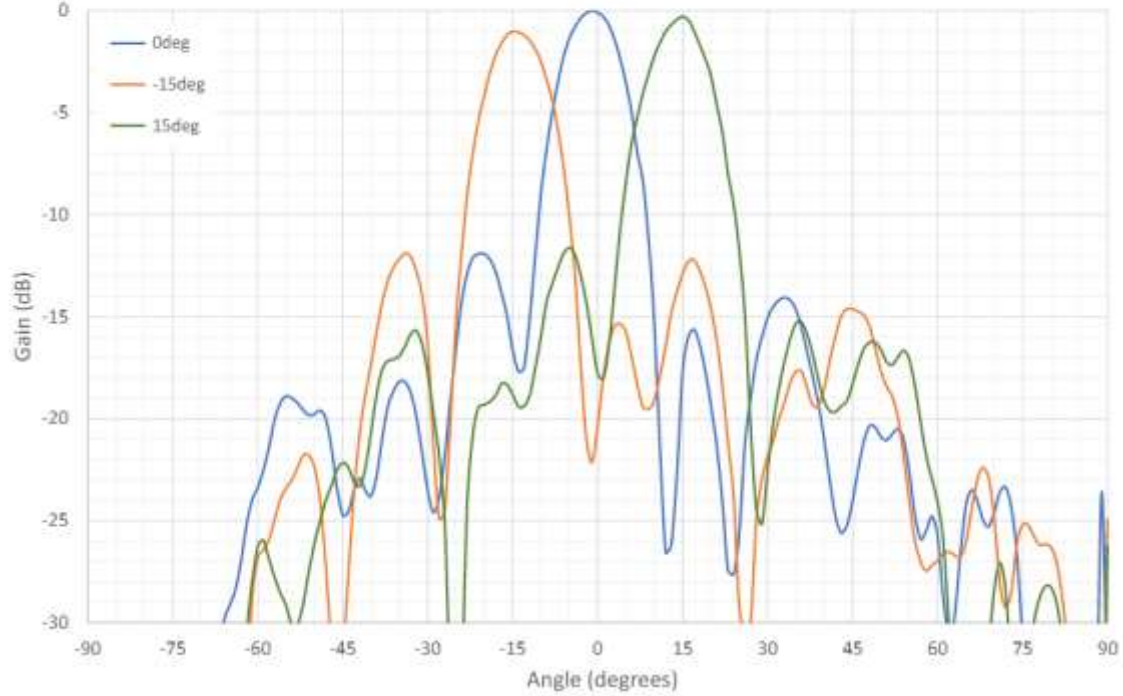
© Otava Inc, 2021

TRANSMIT ANTENNA SCAN PATTERNS, V-POLARIZATION

28GHz Azimuth Scan, +/- 45 degrees



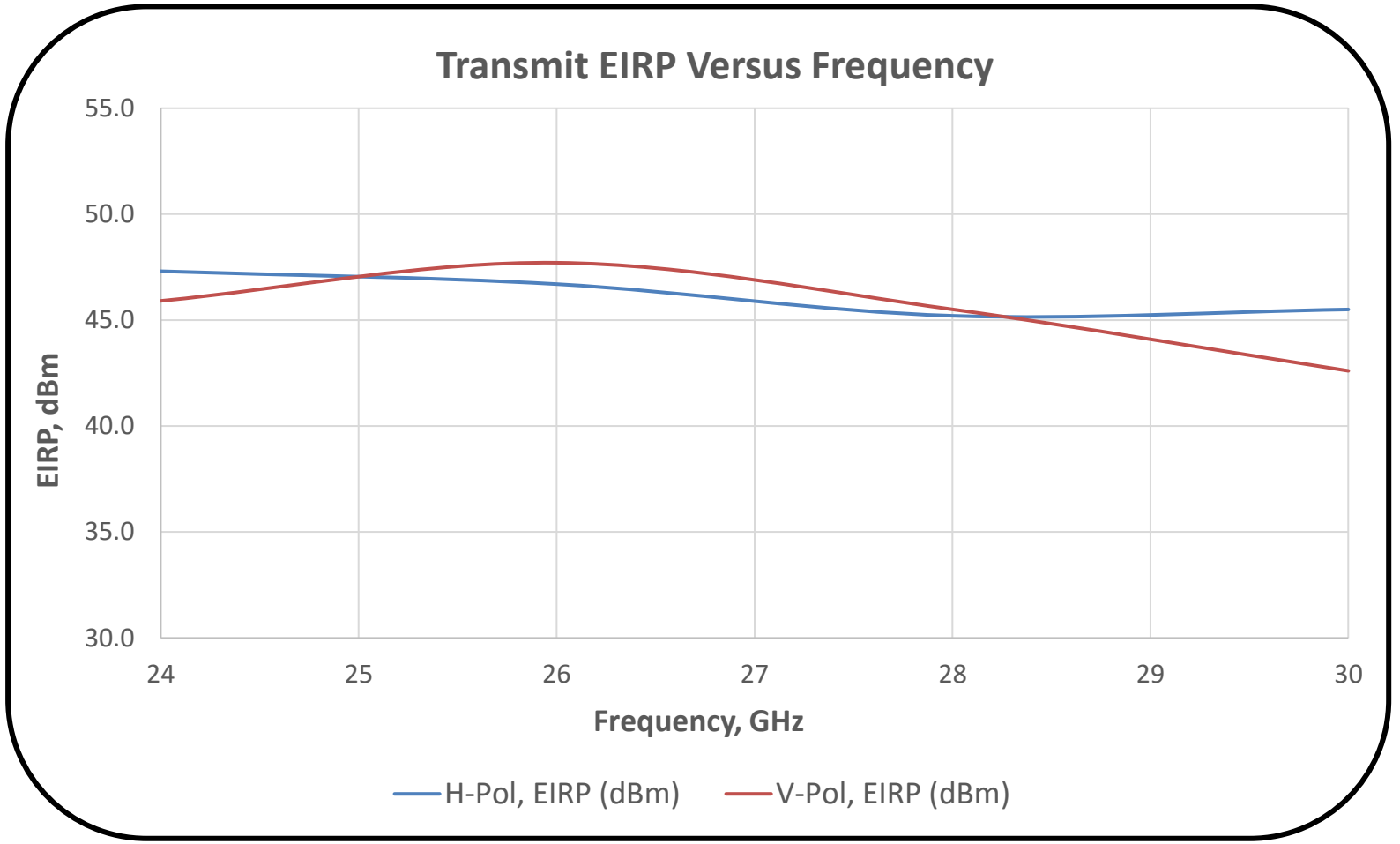
28GHz Elevation Scan, +/- 15 degrees



Robust Measured Scan Angle Performance

© Otava Inc, 2021

TRANSMIT EIRP MEASUREMENT VS FREQUENCY

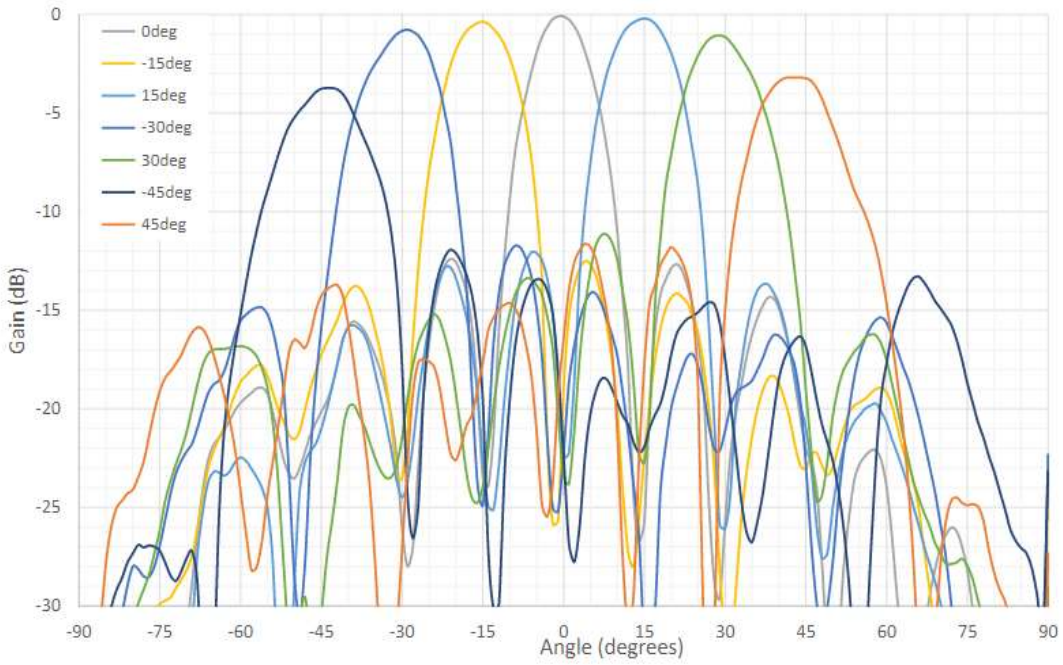


Consistent Measured EIRP Performance over Wideband

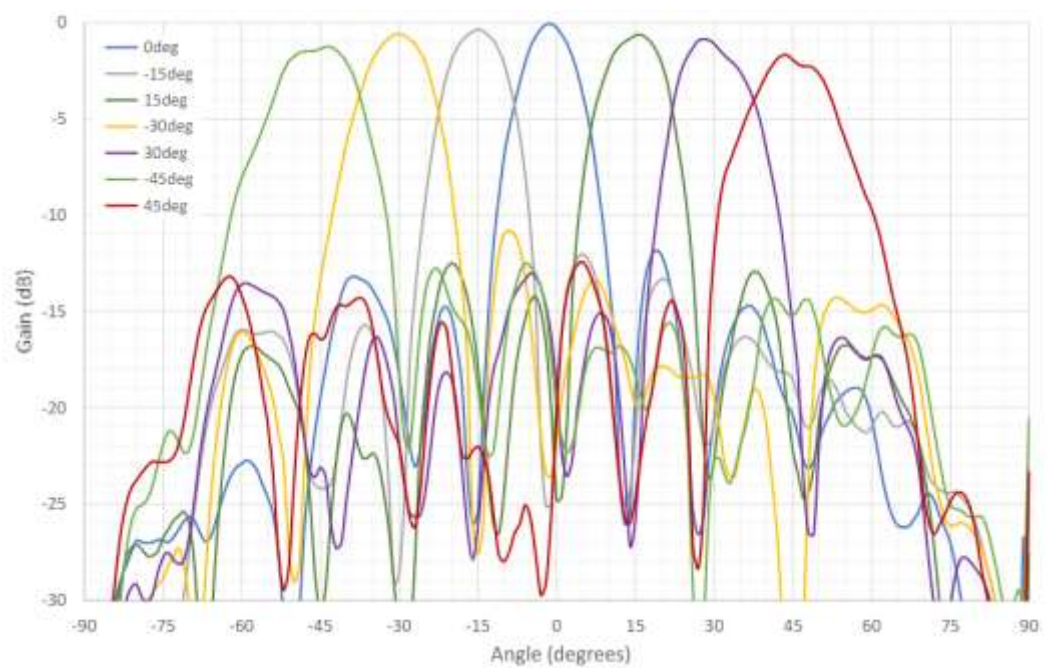
© Otava Inc, 2021

RECEIVE ANTENNA SCAN PATTERNS, H & V POLARIZATIONS

28GHz Scan – H-Polarization



28GHz Scan – V-Polarization

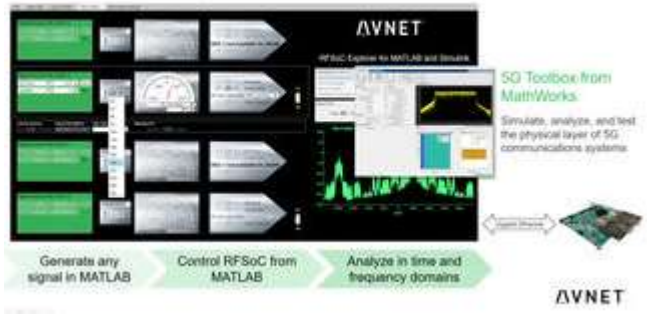


Robust Measured Scan Angle Performance

© Otava Inc, 2021

ANTENNA TO BITS REFERENCE HARDWARE CHAIN

Avnet RFSoC Explorer with MATLAB and Simulink

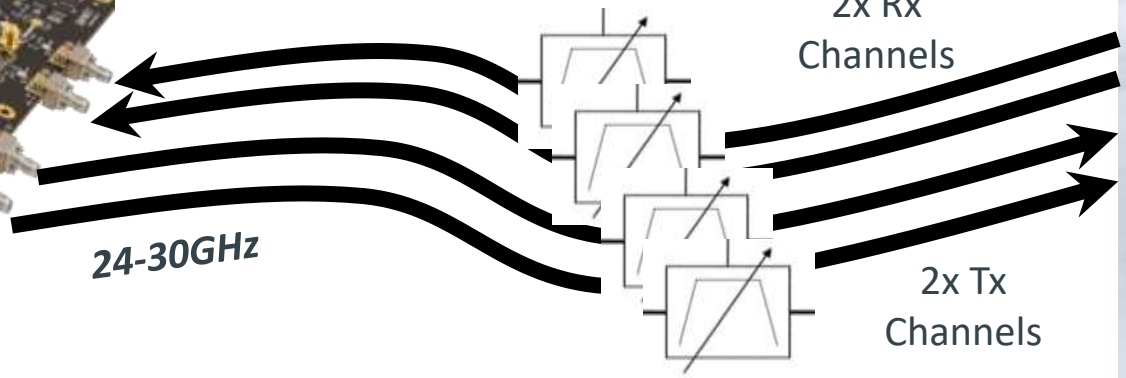


Existing software platform to be expanded to include beamforming algorithms and weight functions for array control

OTFL301, Tunable Filter
24-40GHz

Dual Transceiver Board
19-31 GHz

RFSoC Gen3 Dev Board



PAAM

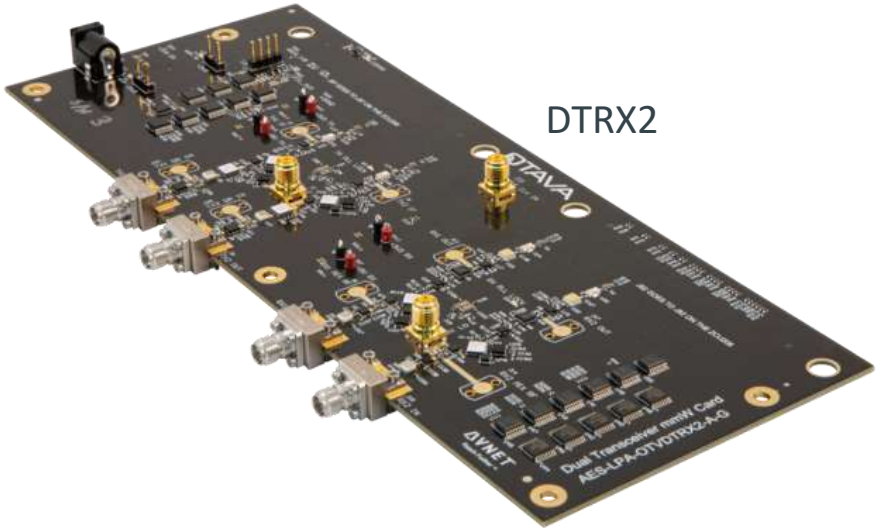
Designed to Complement AMD's RFSoC with Otava's Products -> A Complete Antenna to Bits Reference Hardware Chain

© Otava Inc, 2021

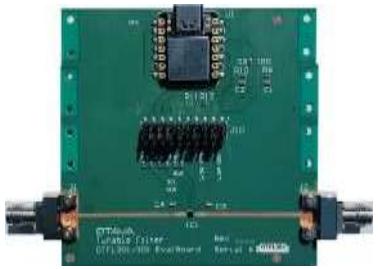
REFERENCES

•For PAAM, BFIC103, DTRX2, Tunable Filters inquiries, please email Otava at hello@otavainc.com

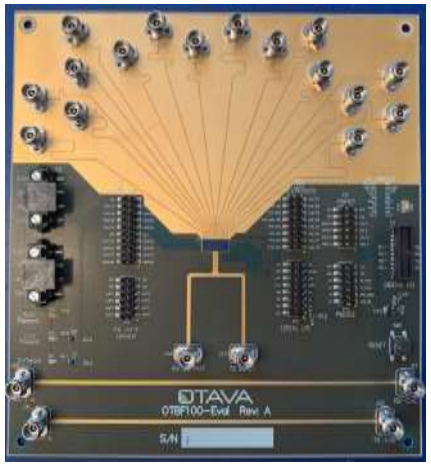
•More information at https://www.otavainc.com/



DTRX2



OTFL301, Tunable Filter
24-40 GHz

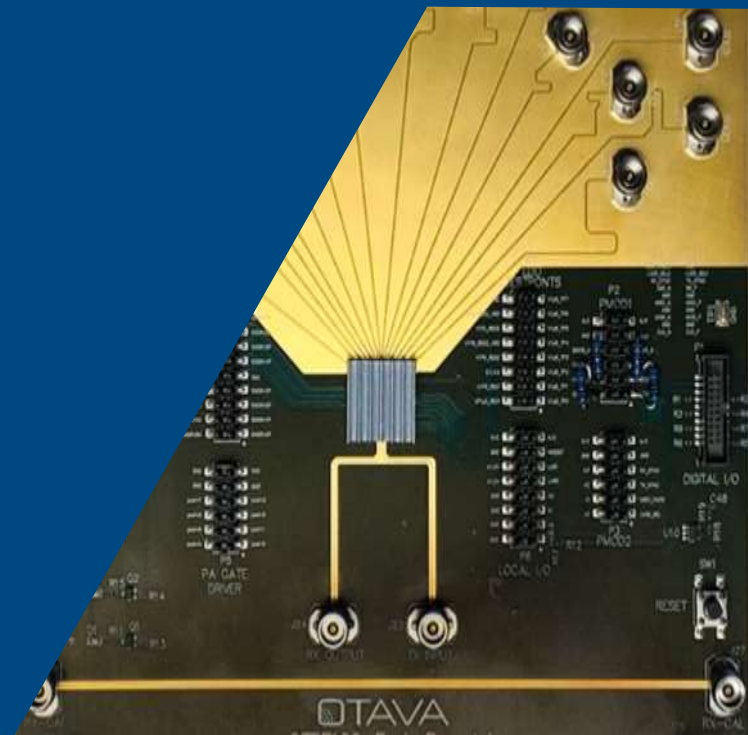


24-40 GHz BFIC

PAAM

Balancing Tradeoffs: Taming Signal Integrity Challenges in mmWave Antenna-to-Bits Implementations

How to Apply Model-Based-Design to mmWave Beamforming Systems



Giorgia Zucchelli

Product Manager RF&AMS
MathWorks

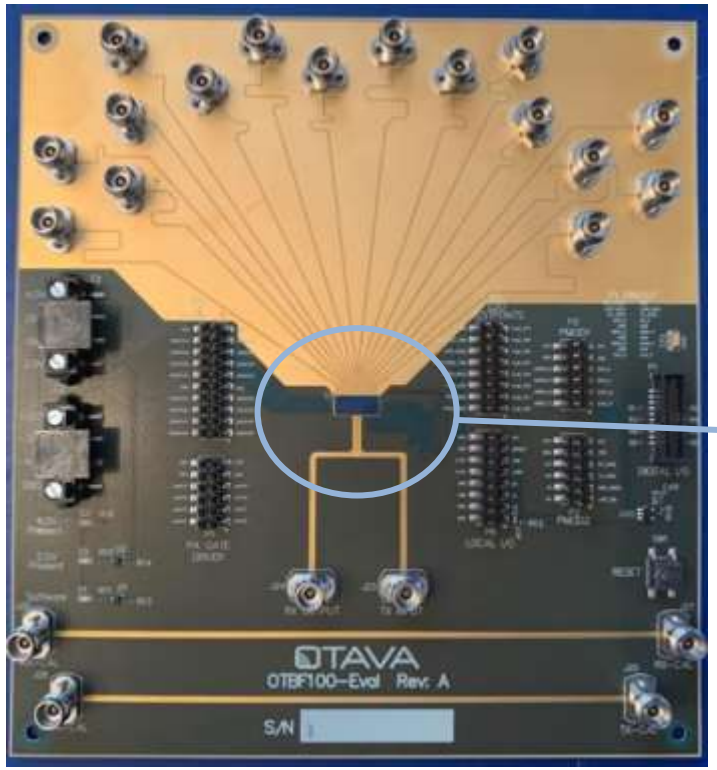
© 2023 The MathWorks, Inc.

Agenda

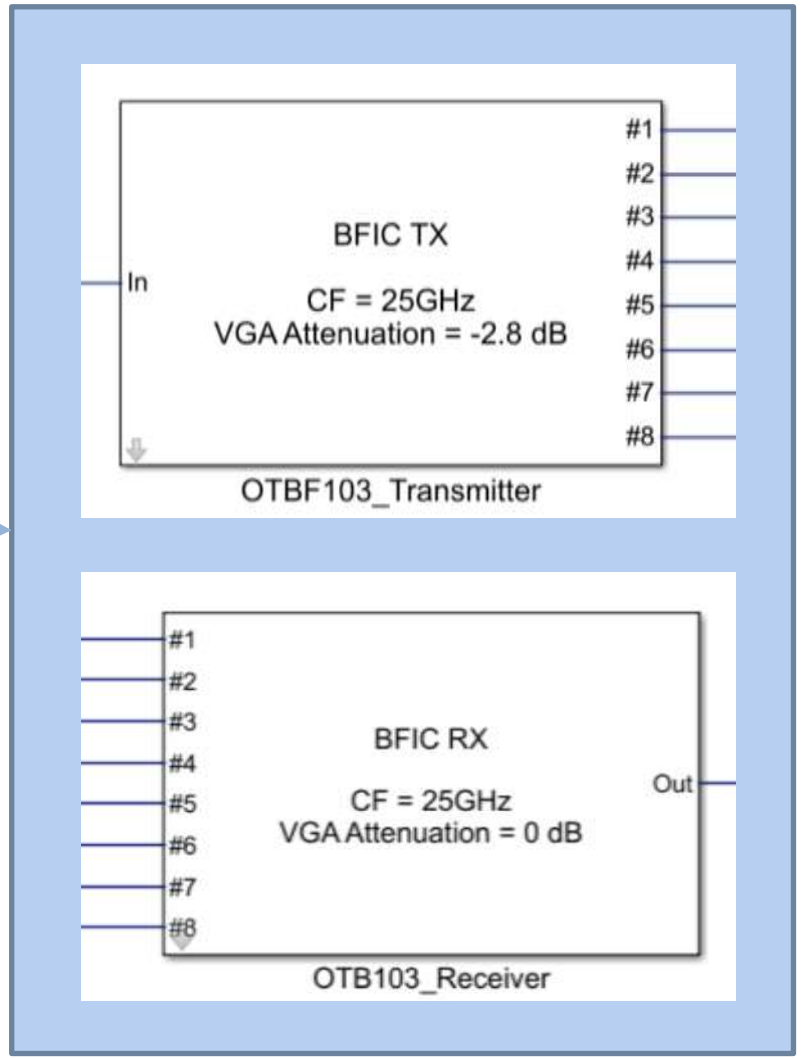
- Introducing a high-fidelity model of the Otava Beamformer IC (BFIC)
- Verifying the model: using RF characterization data and integrating with array arrays
- Understanding the simulation technology behind the model
- Using the model to describe the Antenna In Module (AIM) card and scaling up to the PAAM system
- Conclusions

Introducing the BFIC Model

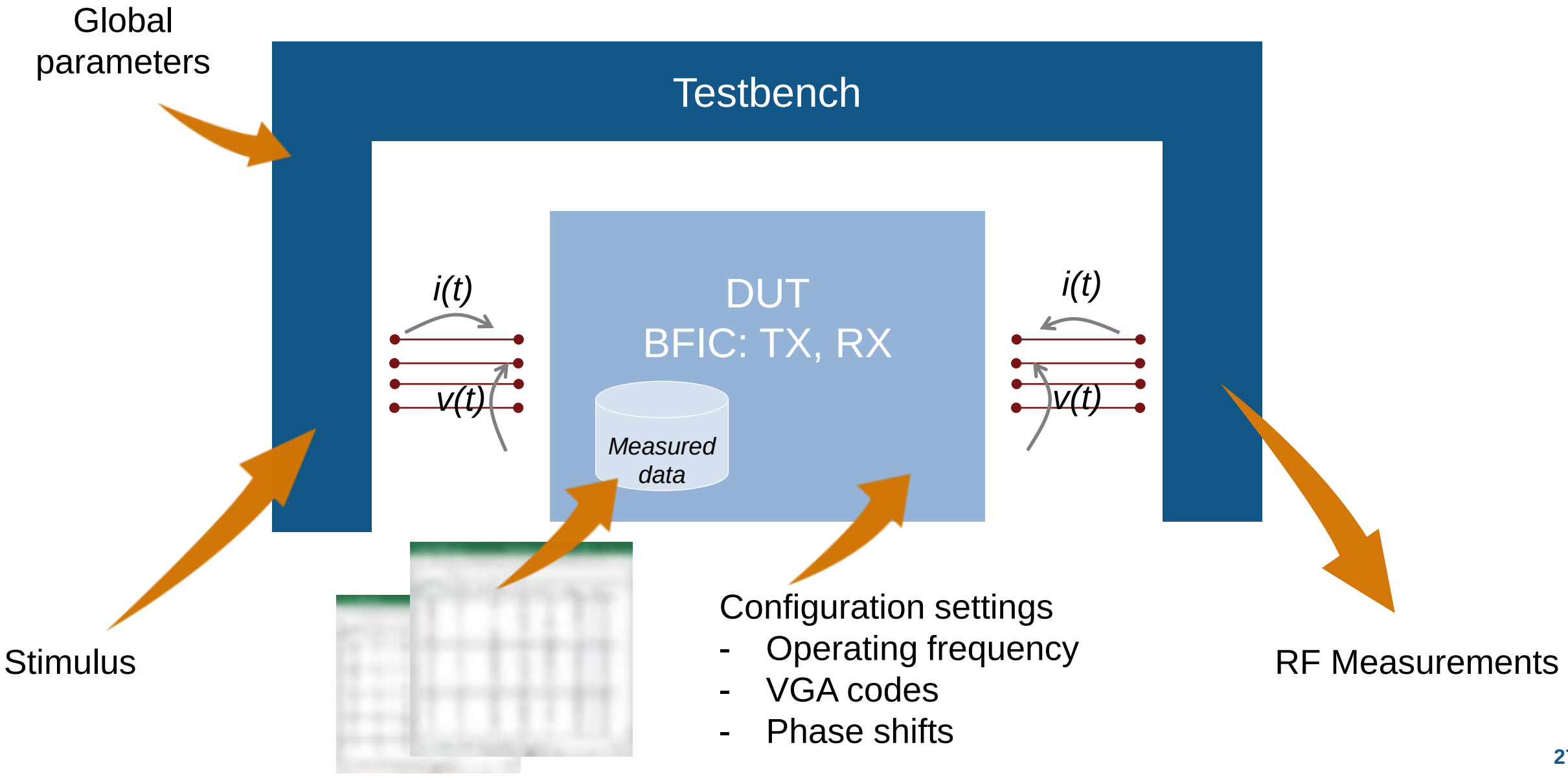
The Eval Board



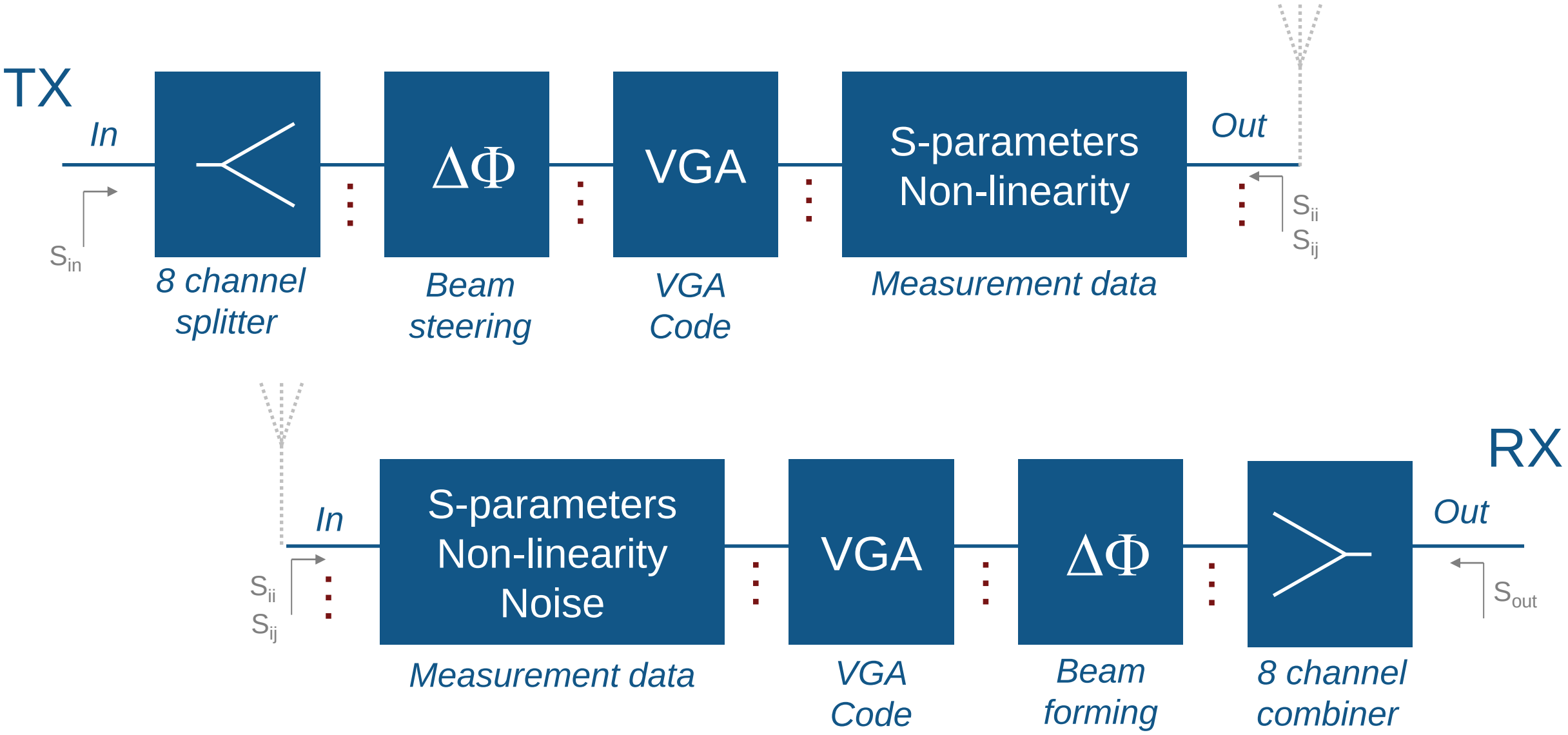
…. AND the MATLAB model



Overall Modeling Guidelines

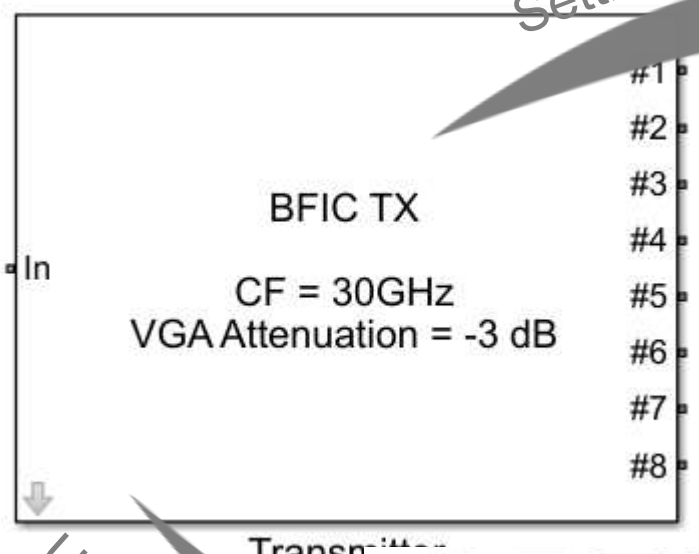


Structure of the BFIC Models

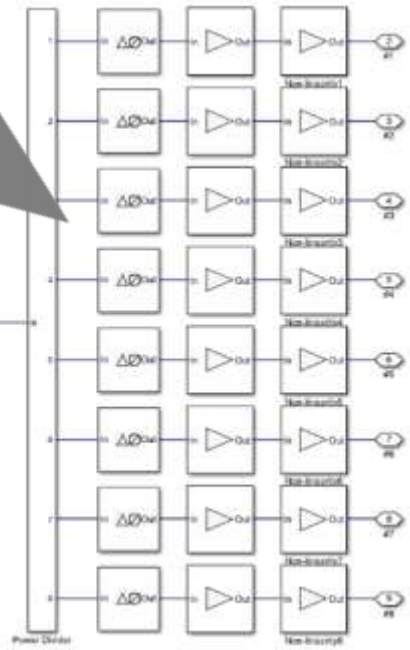


TX Model in Practice

Settings



Underlying structure



Block Parameters: Transmitter

Otava BFIC Transmitter

Center Frequency (Hz) 30e9

VGA Code (0..255) [250 210 180 140 140 180 210 255]

Phase rotation (deg) [1x8] [273.75 349.82 65.89 141.96 218.03 294.10 10.1

Phase shifts

Filter table contents

Index	Phase shift	I code	Q code
1	275.625	29	255
2	348.75	127	141
3	67.5	26	120
4	140.625	243	35
5	219.375	201	250
6	292.5	88	241
7	11.25	127	25
8	84.375	5	124

Plot Characteristics

OK Cancel Help Apply

Operating frequency (24-40GHz)

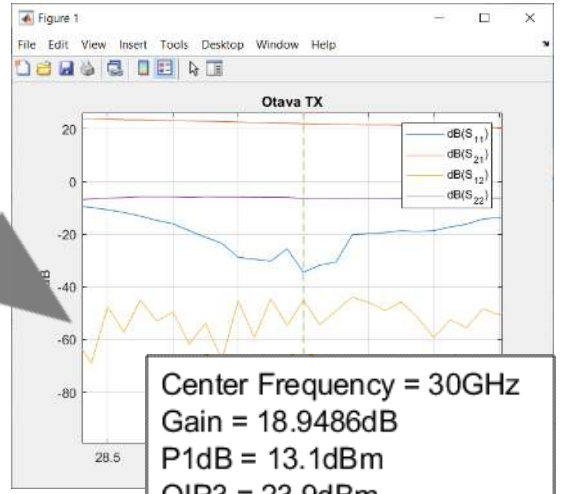
VGA codes (tapers)

Phase shifts

Applied quantized phase shifts

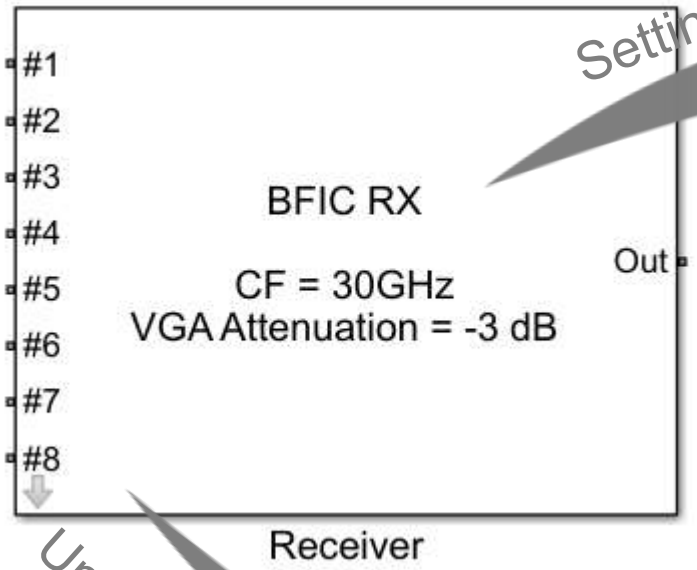
Applied I/Q codes

Nominal specs



Center Frequency = 30GHz
Gain = 18.9486dB
P1dB = 13.1dBm
OIP3 = 23.9dBm

RX Model in Practice



Settings

Operating frequency (24-40GHz)

VGA codes (tapers)

Phase shifts

Applied quantized phase shifts

Applied I/Q codes

Underlying structure

Nominal specs

Block Parameters: Receiver

Otava BFIC Receiver

Center Frequency (Hz) 30e9

VGA Code (0..255) [255 250 245 240 240 245 250 255]

Phase rotation (deg) [1x8] [273.75 349.82 65.89 141.96 218.03 294.10 10.17 86.2

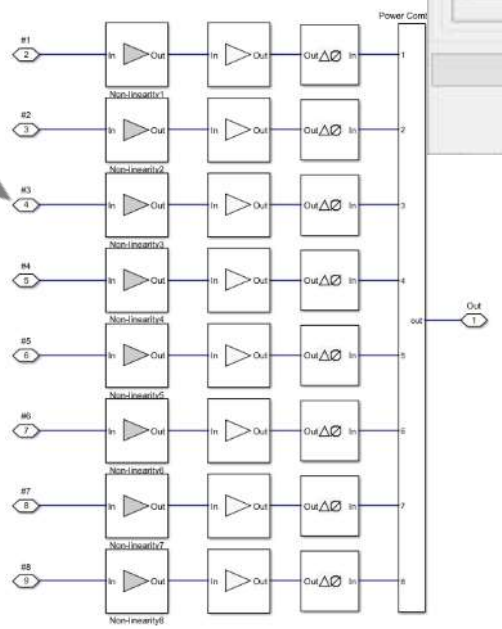
Phase shifts

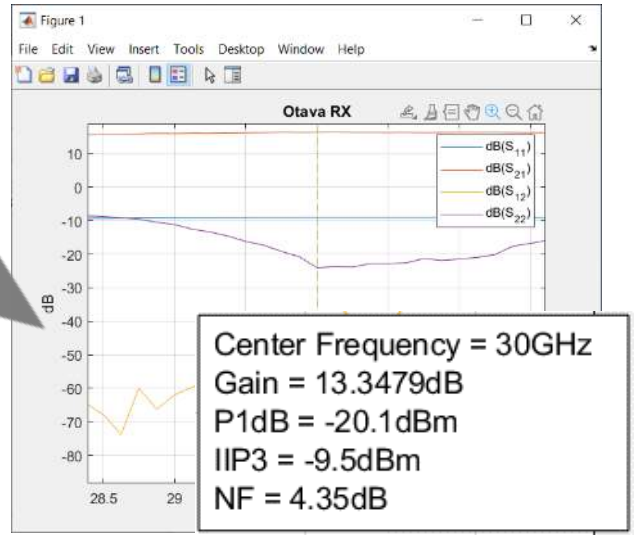
Filter table contents

Index	Phase shift	I code	Q code
1	275.625	29	255
2	348.75	127	141
3	67.5	26	120
4	140.625	243	35
5	219.375	201	250
6	292.5	88	241
7	11.25	127	25
8	84.375	5	124

Plot Characteristics

OK Cancel Help Apply





Center Frequency = 30GHz
Gain = 13.3479dB
P1dB = -20.1dBm
IIP3 = -9.5dBm
NF = 4.35dB

Verifying the Model:
Using RF Characterization Data and Integrating with Antenna Arrays

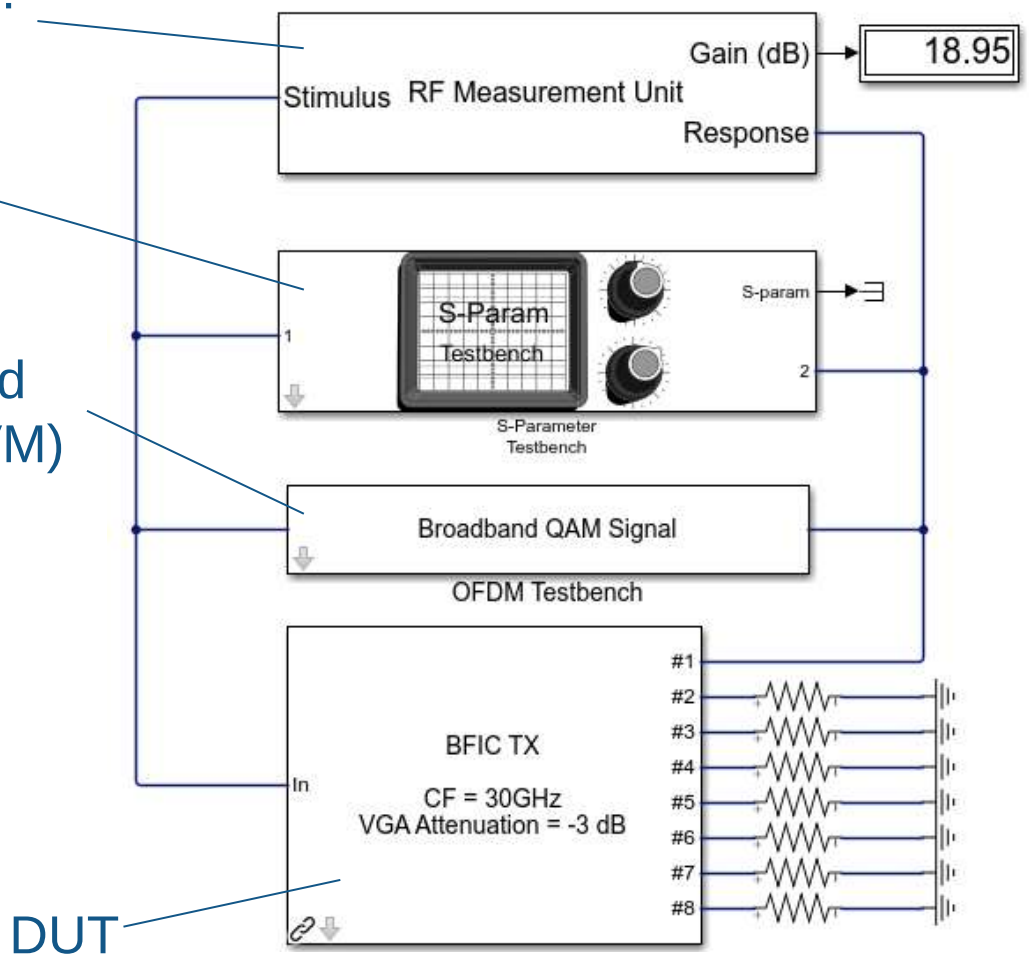
Verifying the BFIC RF Performance

CW measurements:
Gain, IP3, NF

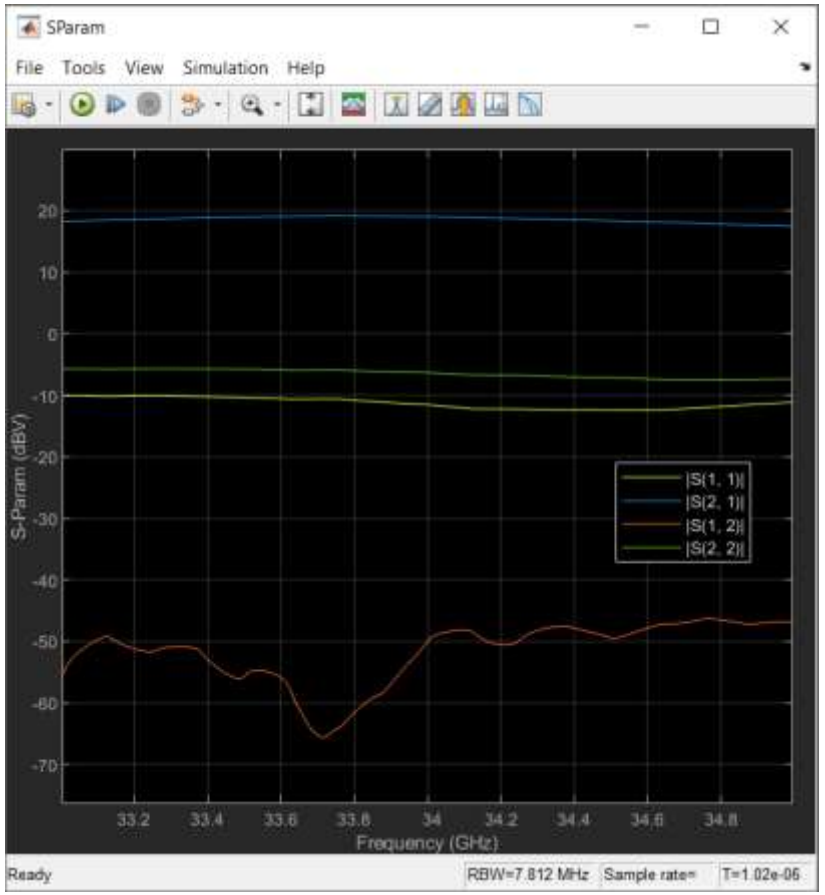
S-parameters

Wideband modulated waveform (ACLR, EVM)

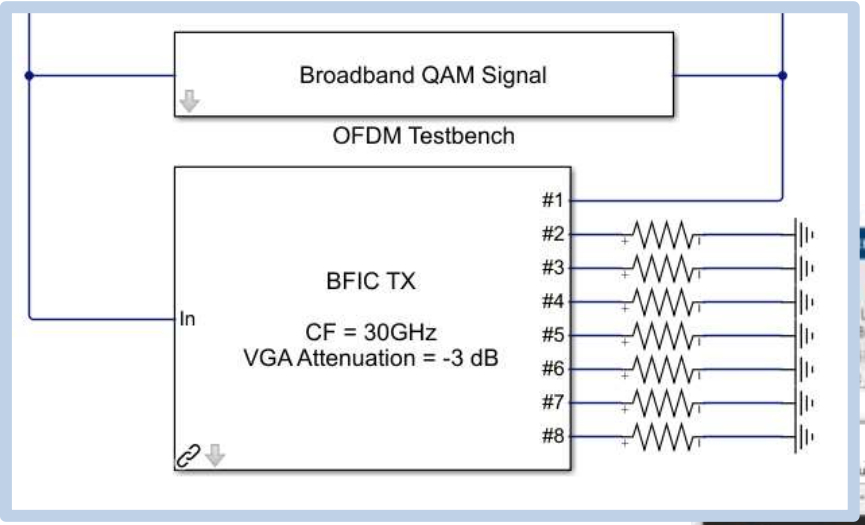
DUT



S-parameter simulation

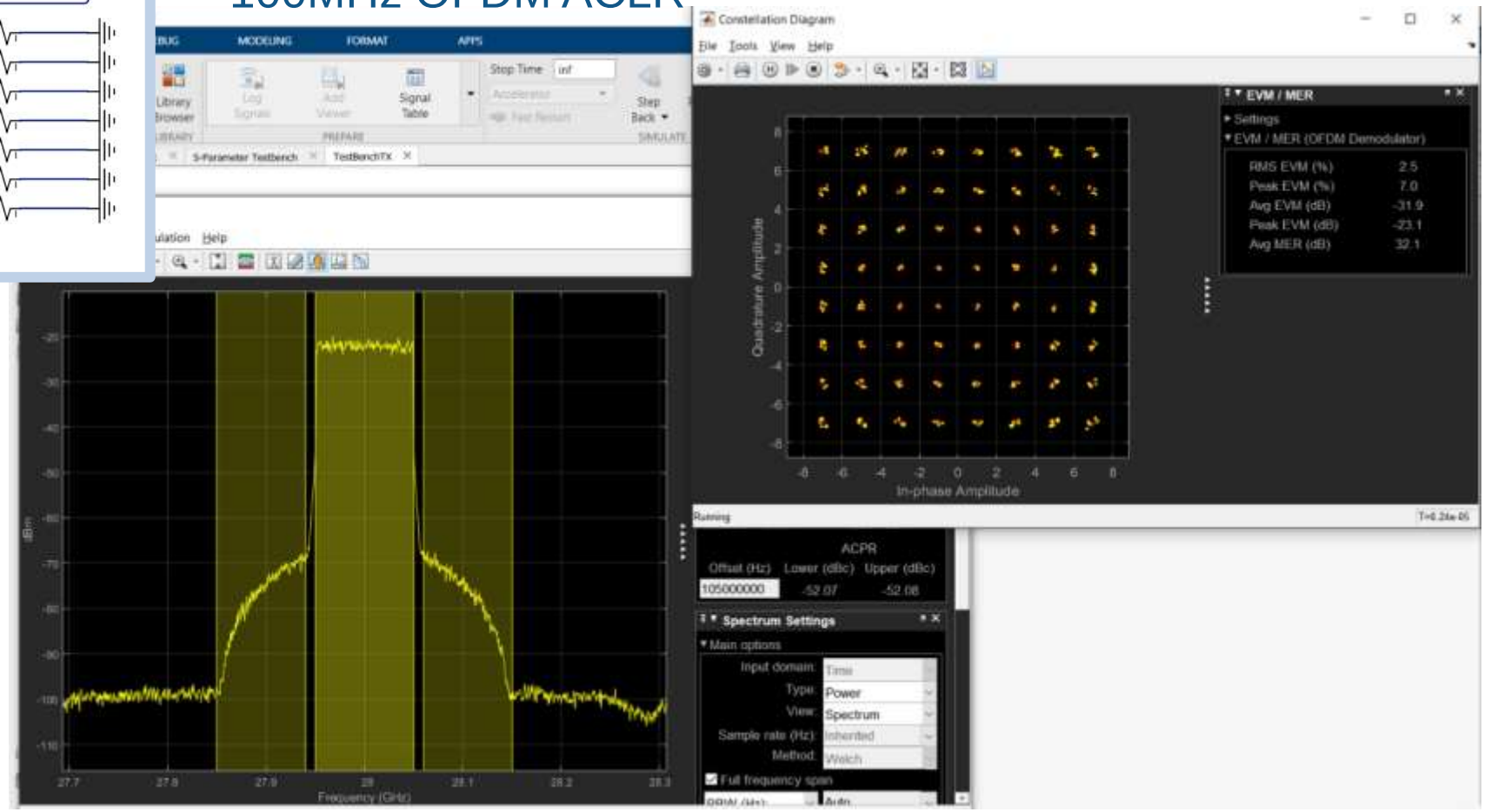


Transmitter Model: Performance Verification



100MHz OFDM ACLR

100MHz OFDM EVM

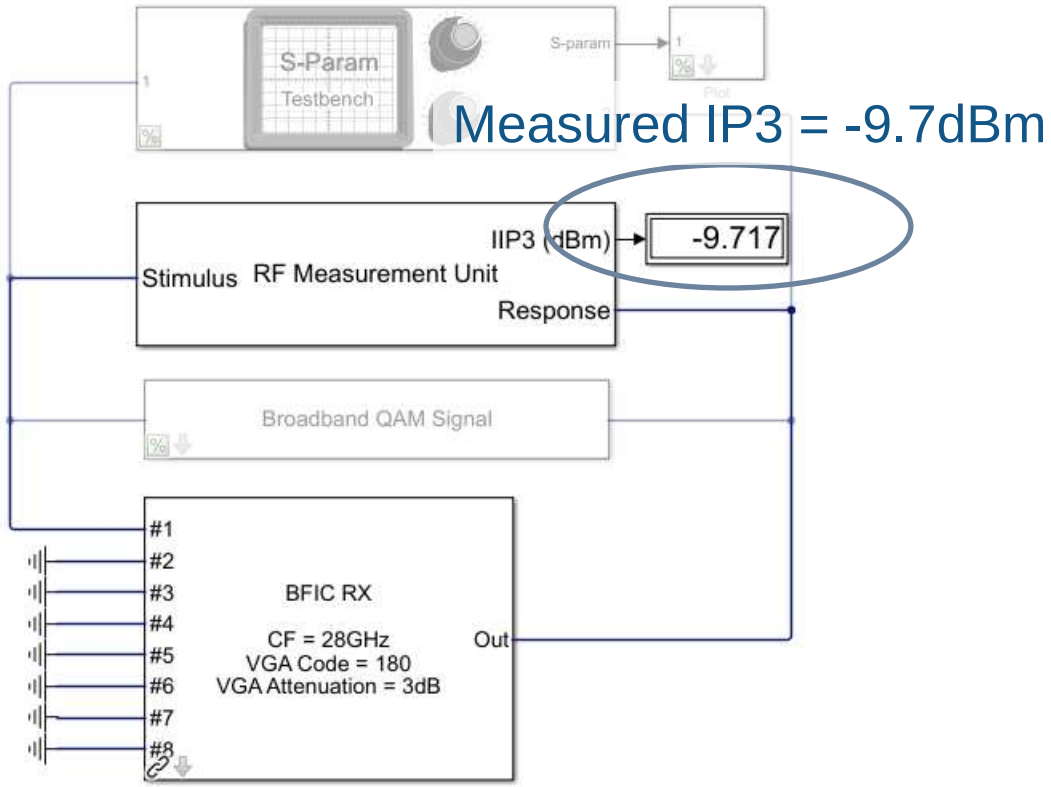


Extract transmitter specs

- ACLR
- EVM
- Noise floor

Receiver Model: Performance Verification

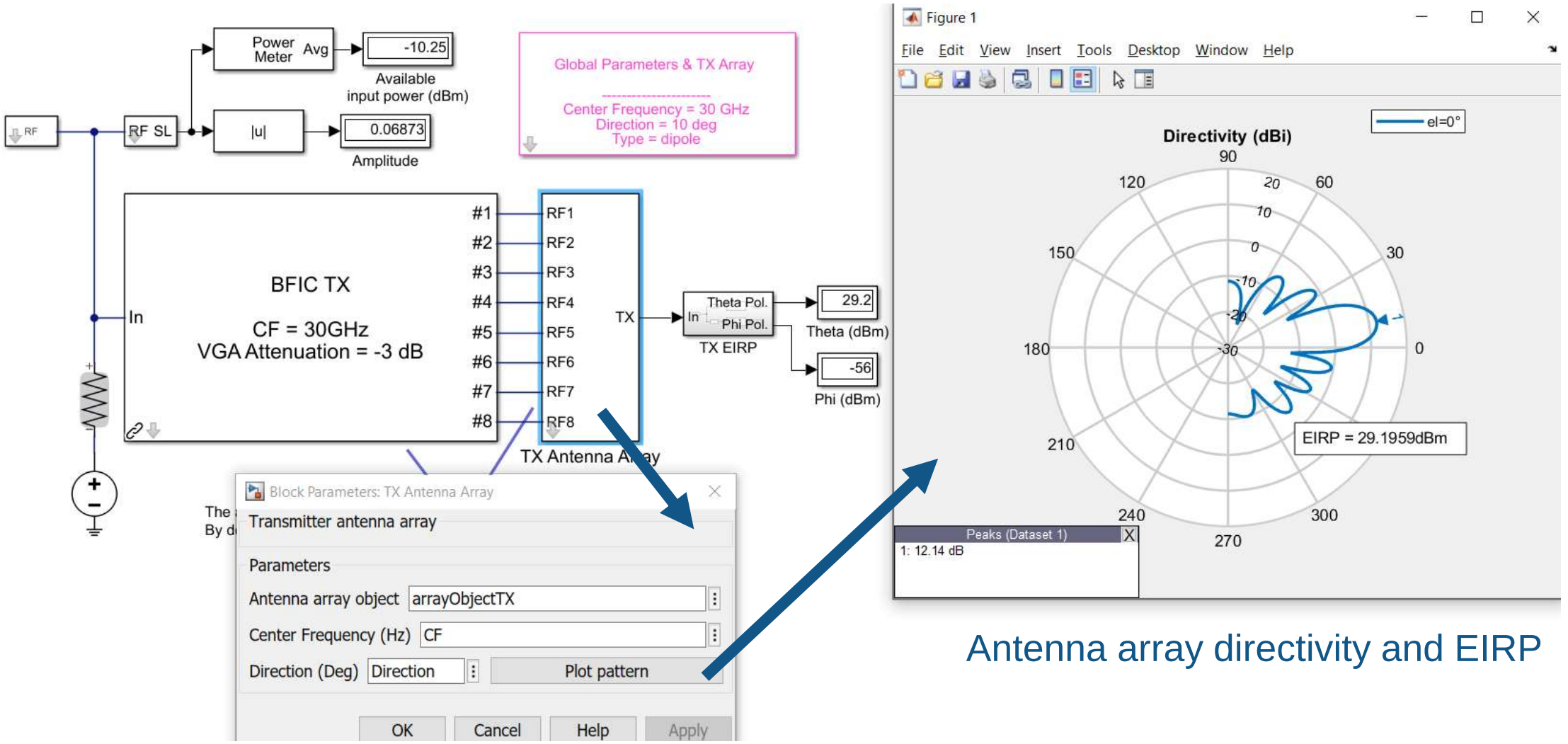
RF Measurement Testbench
Only Uncomment One at the Time



Measured IP3 = -9.7dBm

Single Channel S-parameter simulation results

Now Attaching an Antenna Array Model

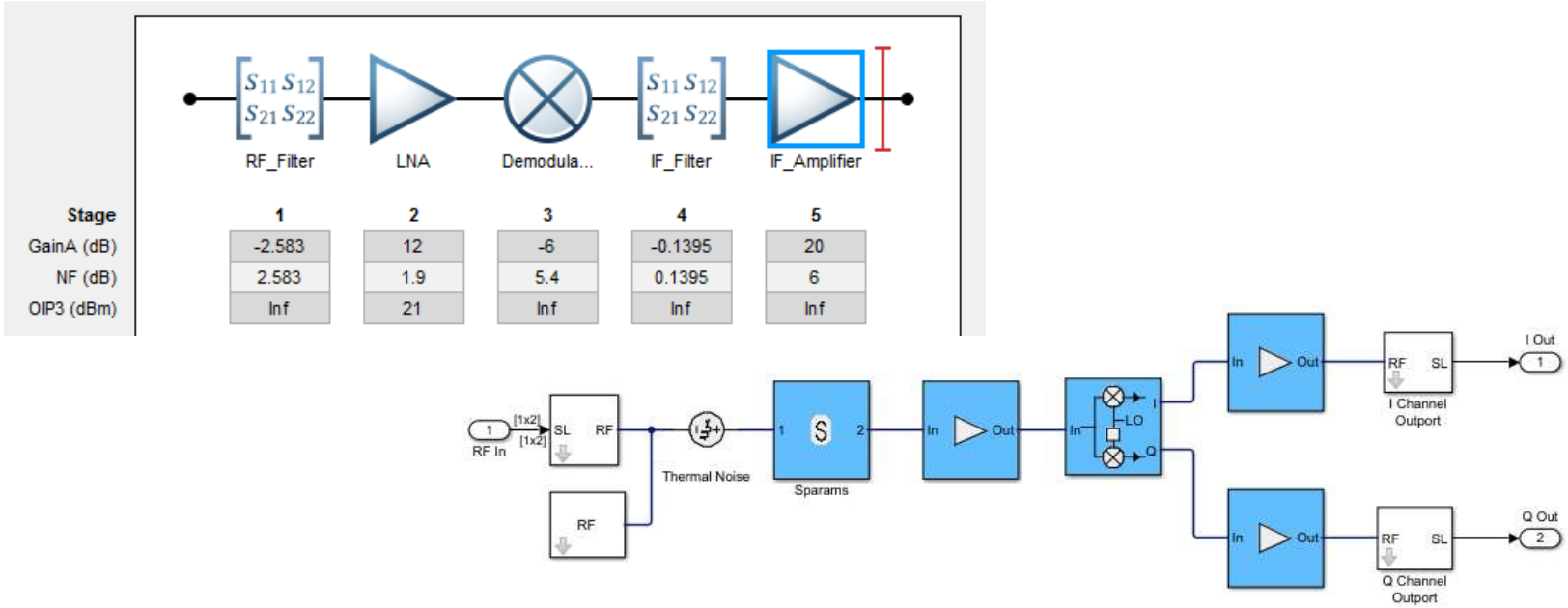


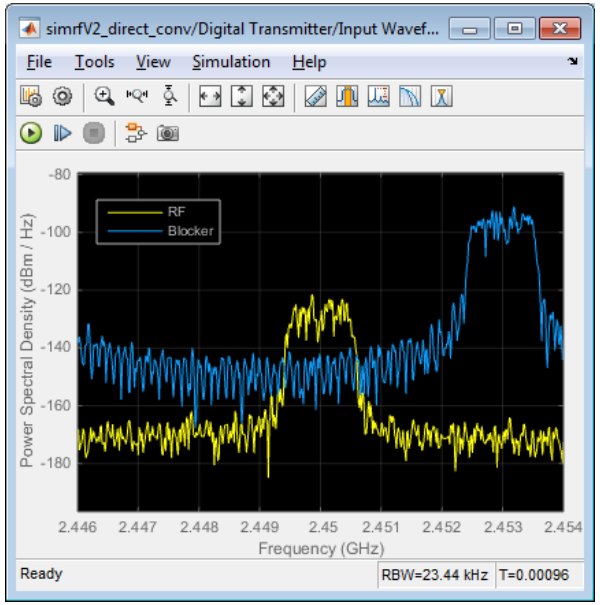
Antenna array directivity and EIRP

Understanding the Technology Behind the Model

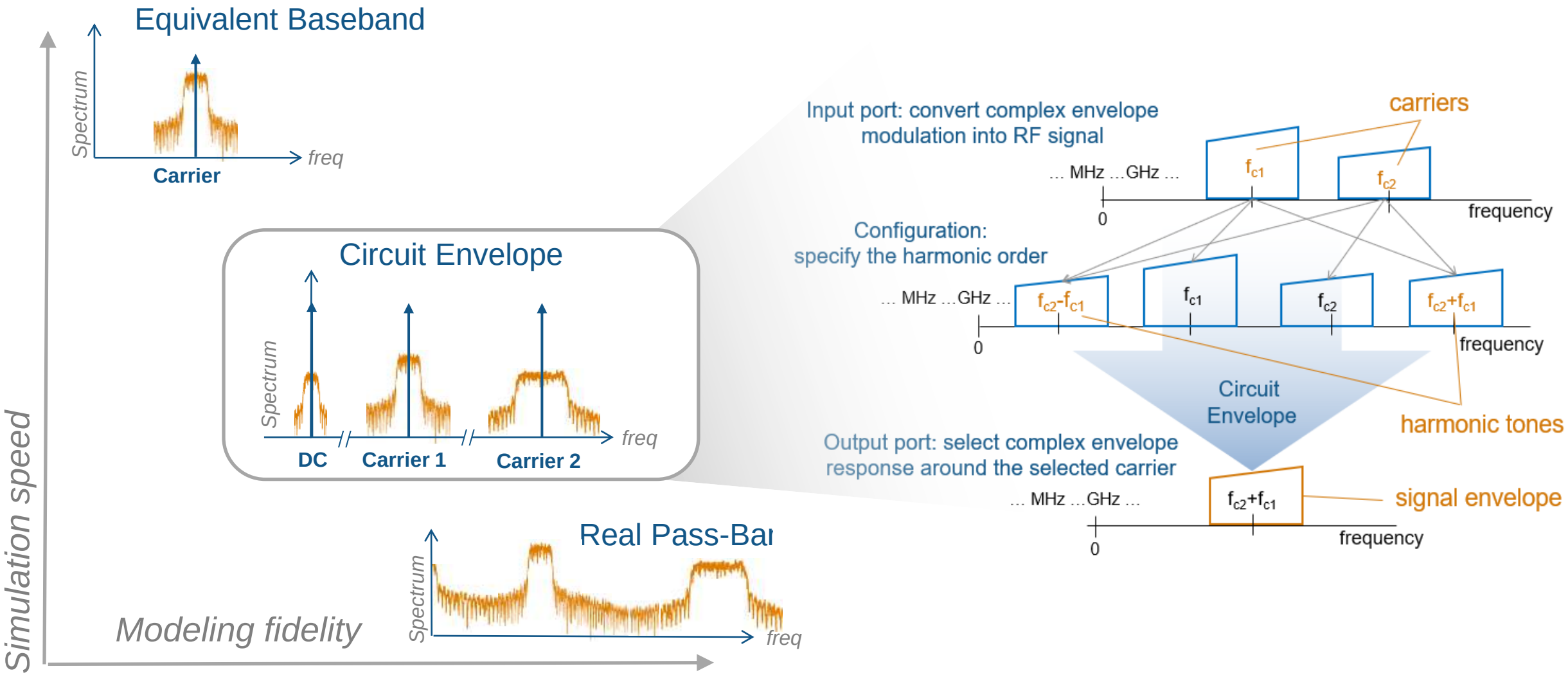
Trade Off Fidelity and Speed with System-Level RF Models

- Design the architecture and define the specs of the RF components
- Integrate RF front ends with adaptive algorithms such as DPD, AGC, beamforming
- Test and debug the implementation of the transceiver before going in the lab
- Use models and measured data to gain insights in your design
- Provide a model of the RF transceiver to your colleagues and customers



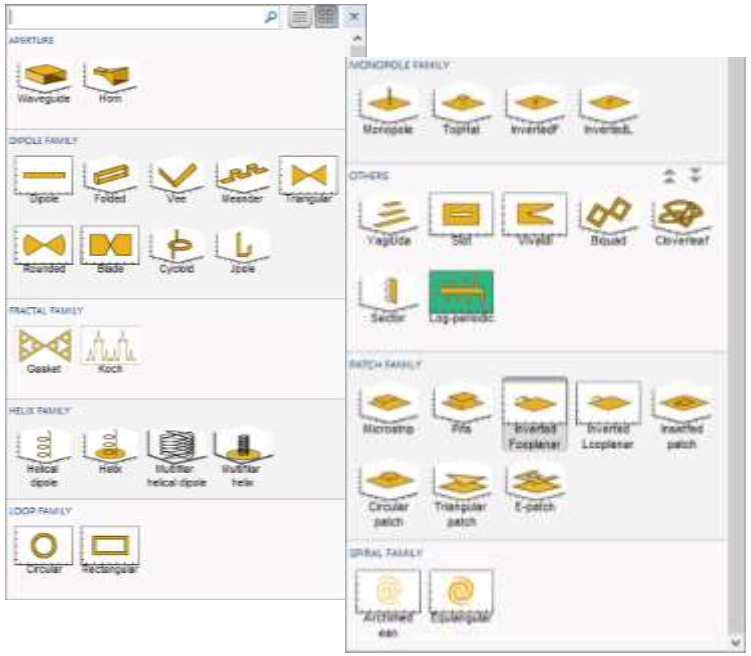


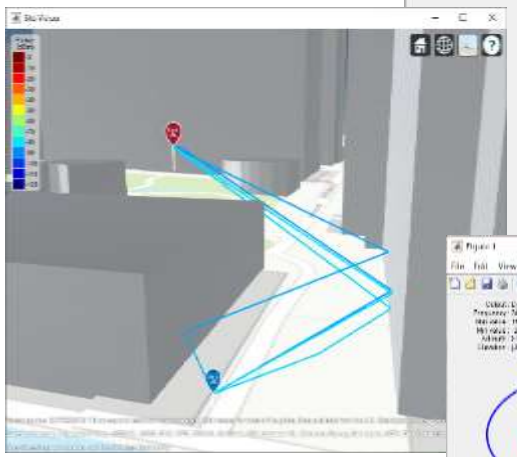
RF System Simulation with RF Blockset

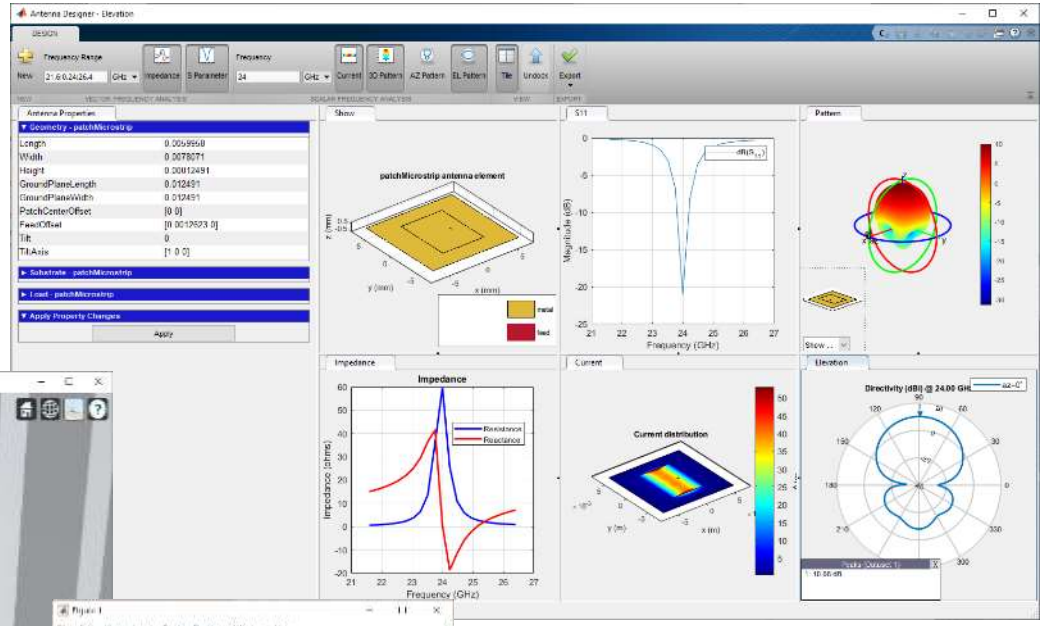


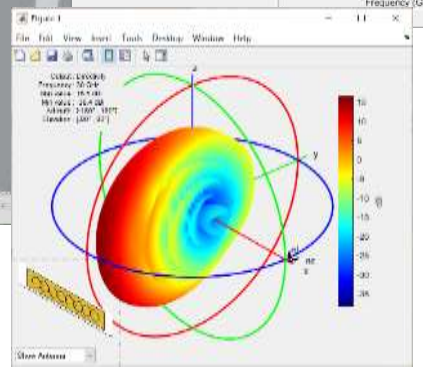
Design, Analyze, and Visualize Antennas

- Get started with antenna and array catalog and apps
- Perform full-wave EM simulation (Method of Moments)
- Improve the performance using surrogate optimization
- Design and fabricate PCBs with Gerber file generation
- Analyze the effects of installation on large platforms
- Include RF propagation effects



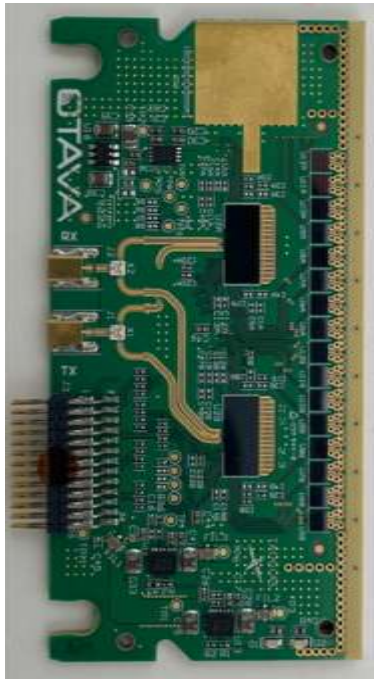






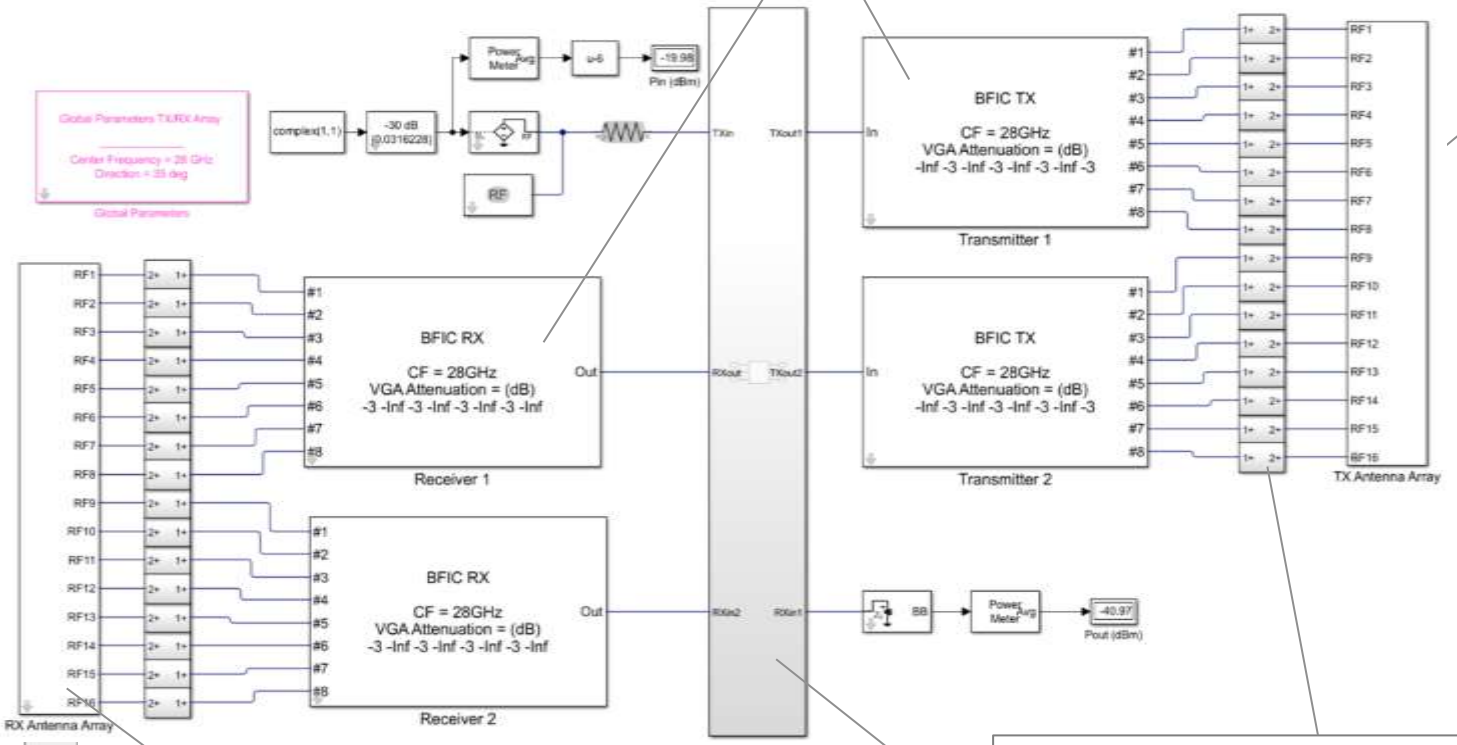
Using the Model to Describe the Antenna in Module (AiM) Card and Scaling up to the PAAM System

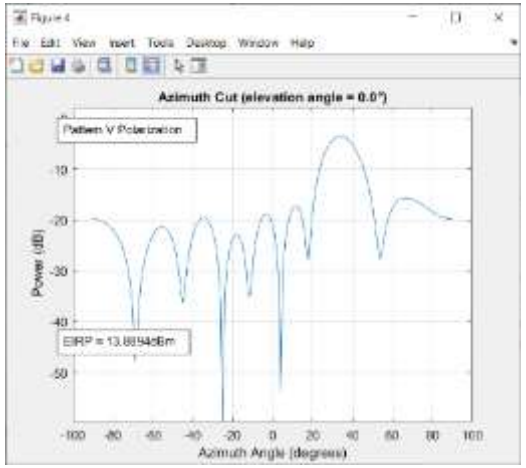
Modeling the AiM Card

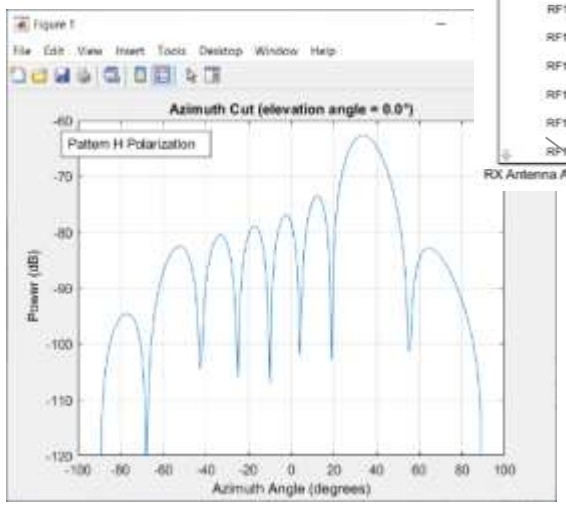


Separately control H/V elements

Antenna model:
- Antenna H/V elements
- Beamsteering
- EIRP





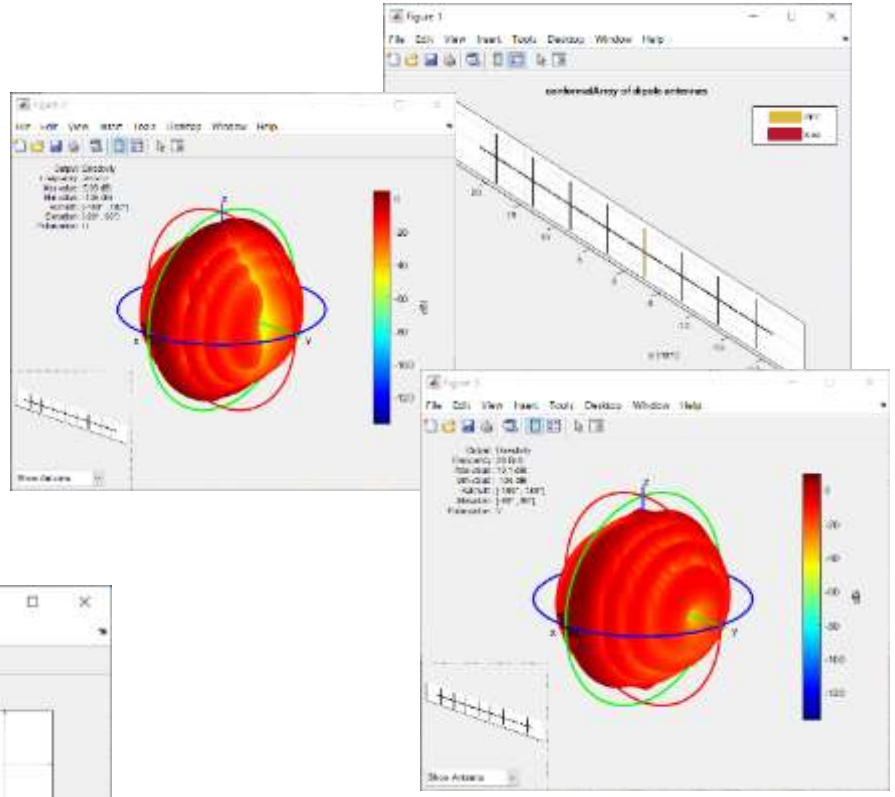


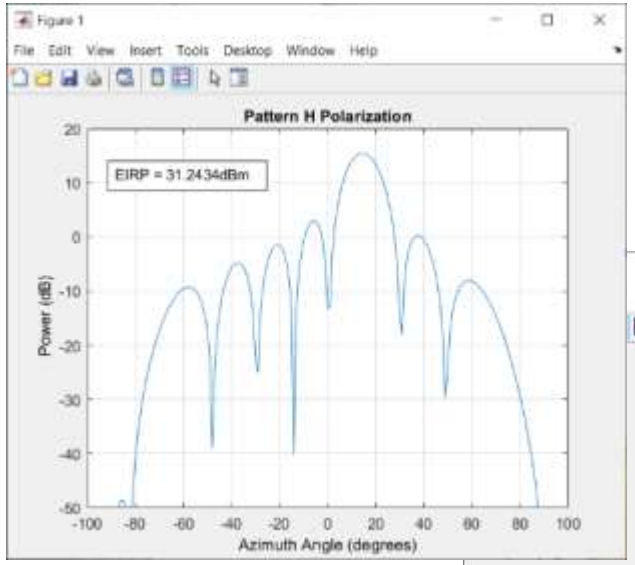
Plane wave excitation:
- Direction of arrival
- Polarization mismatch

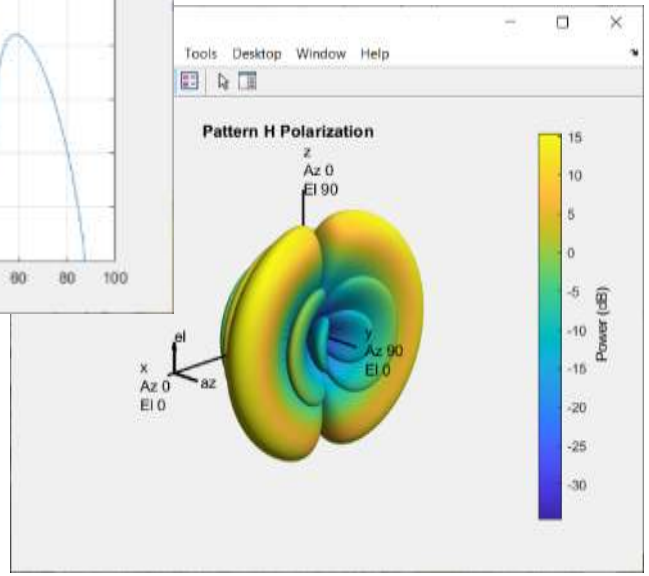
Coupler/Splitter and Switches model:
- Impedance mismatch
- Dispersion
- Losses
- TX/RX Coupling

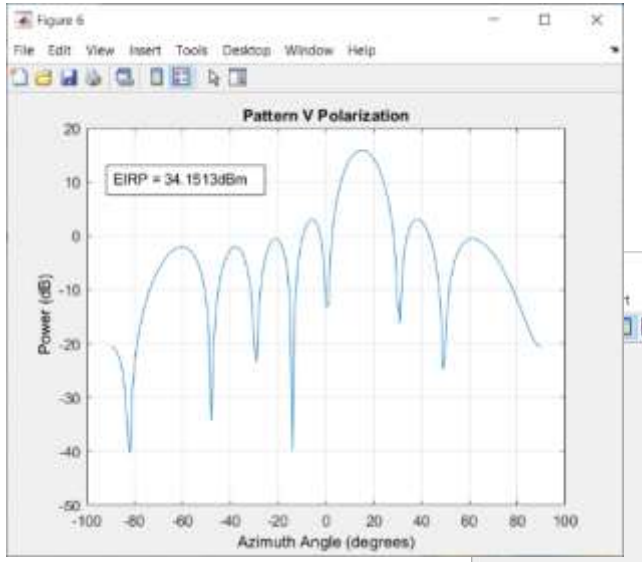
Modeling the AiM Antenna Array 1/2

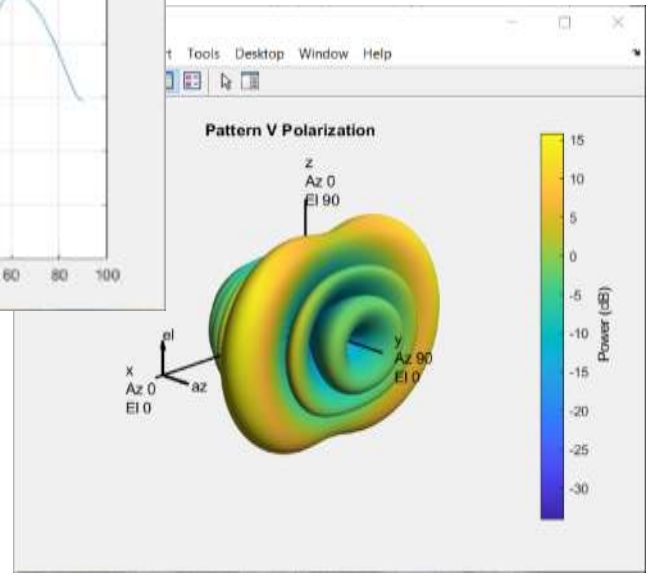
- Design Ideal cross dipole elements (elements in free space)
- Experiment with controlling H/V elements
- Verify patterns and beamsteering
- Extend your design with different type of elements





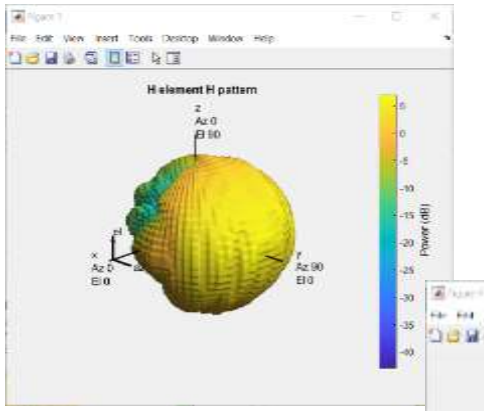


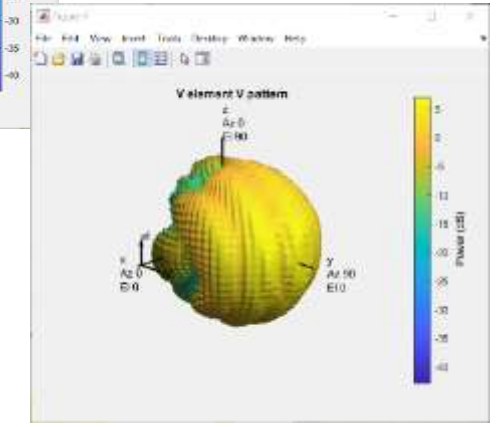


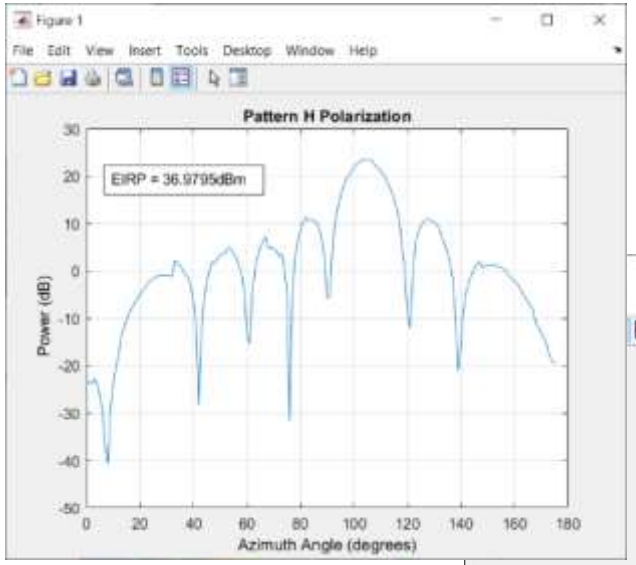


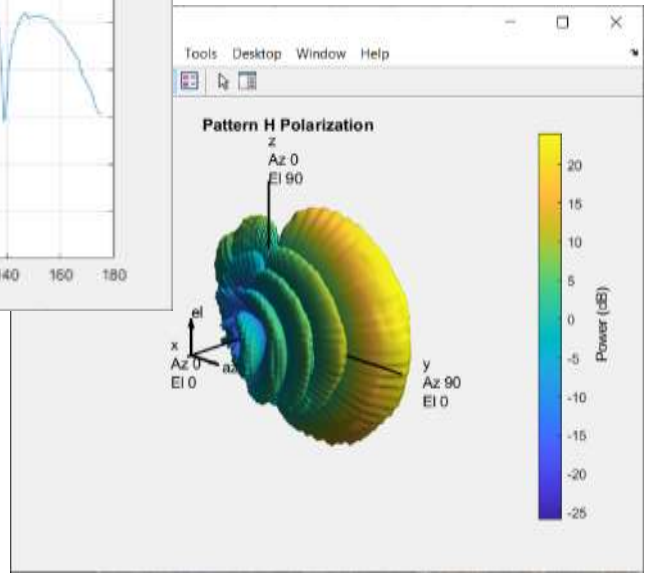
Modeling the AiM Antenna Array 2/2

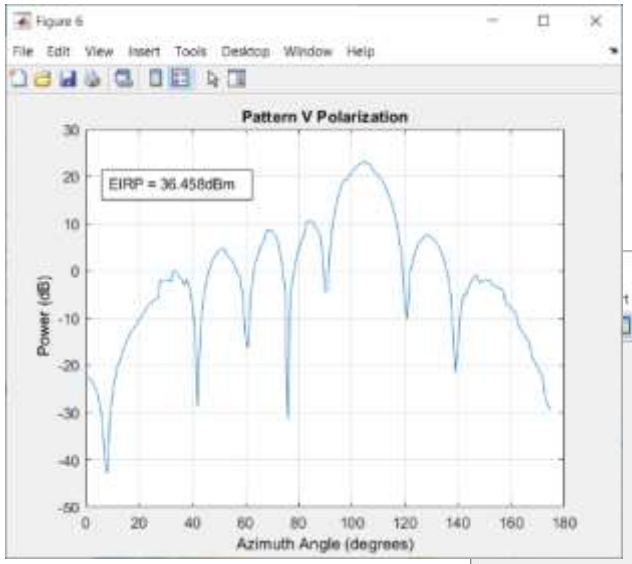
- Import measured antenna patterns
- Integrate into array and experiment with beamforming
- Compare with ideal elements

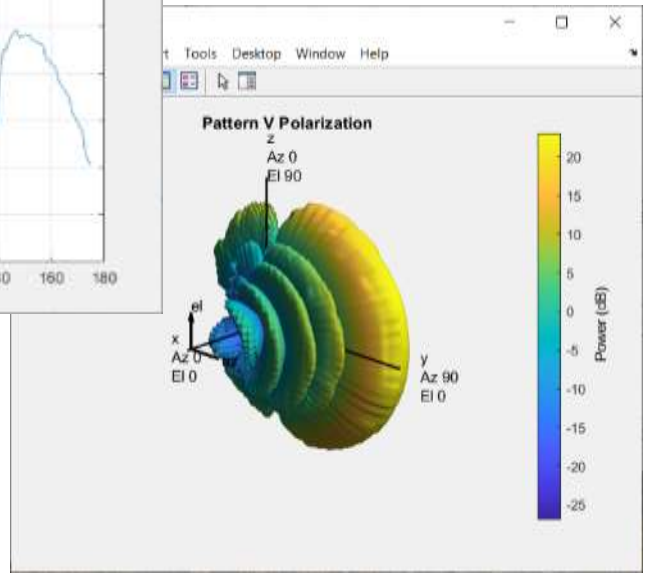




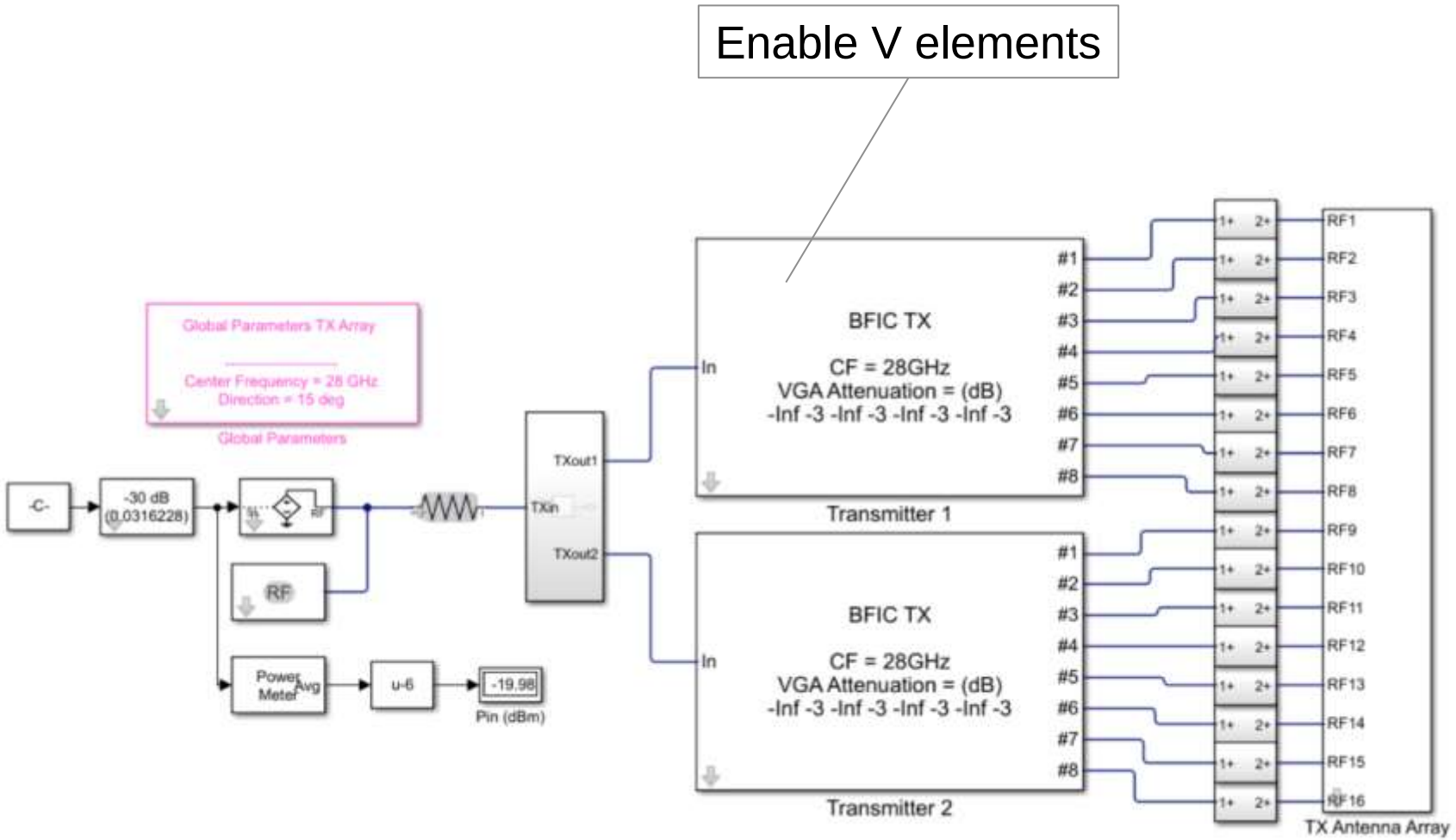


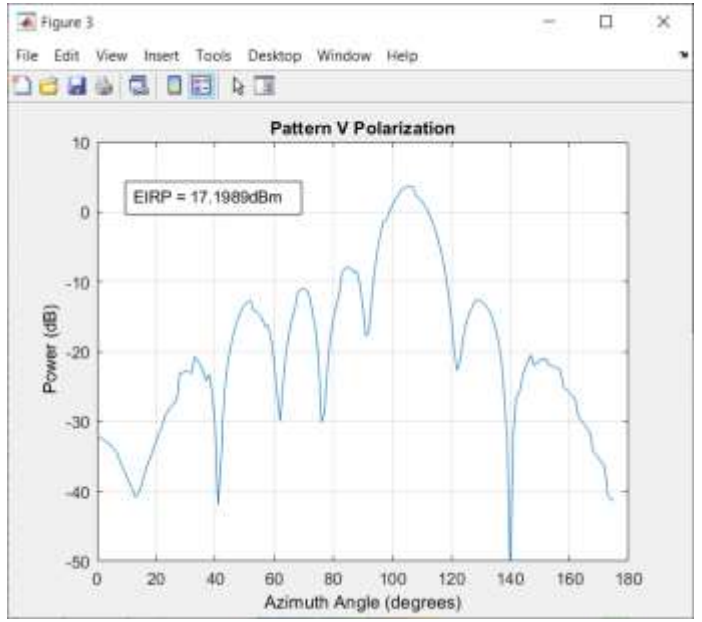


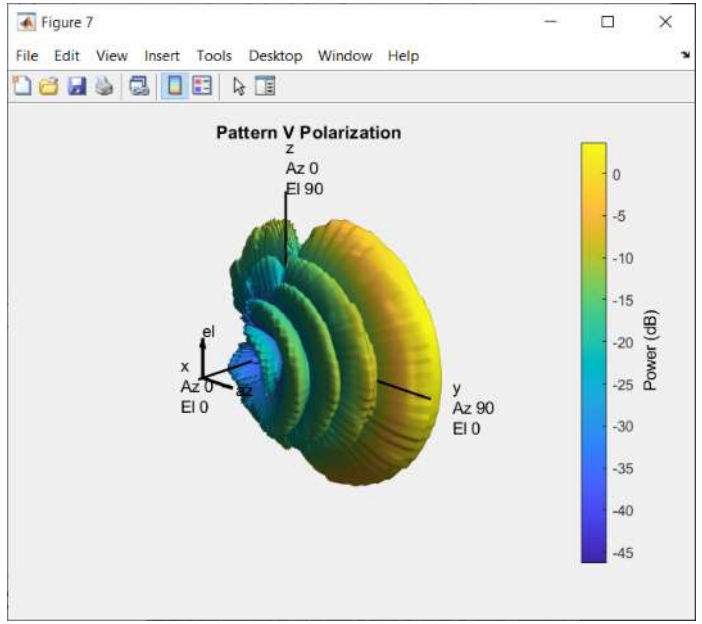




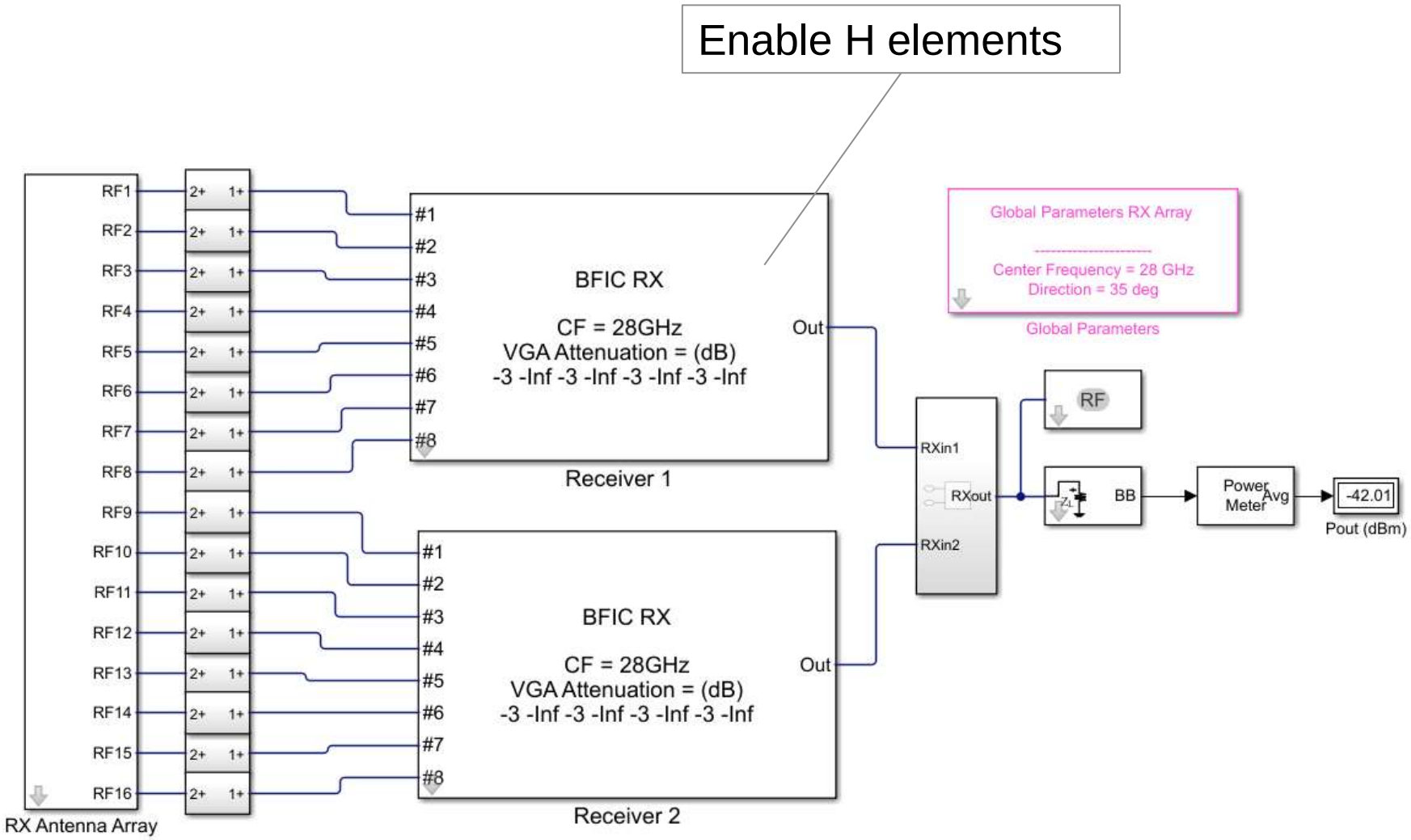
AiM Transmitter

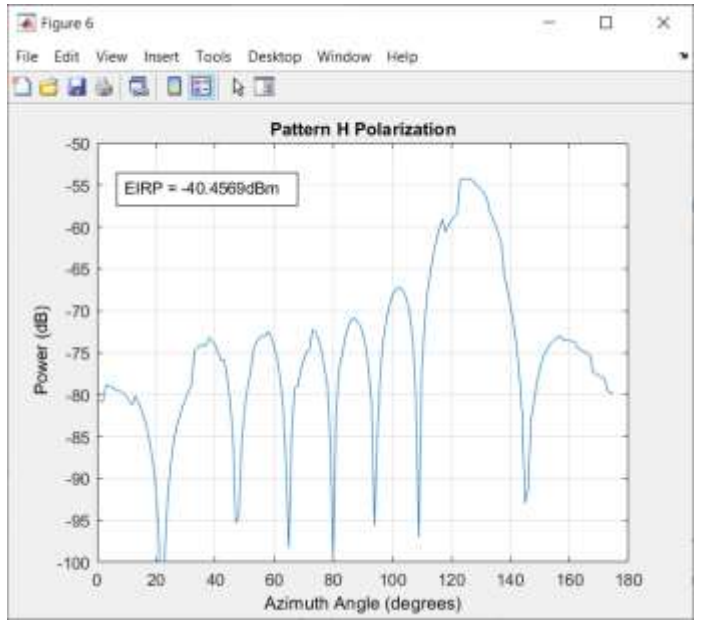


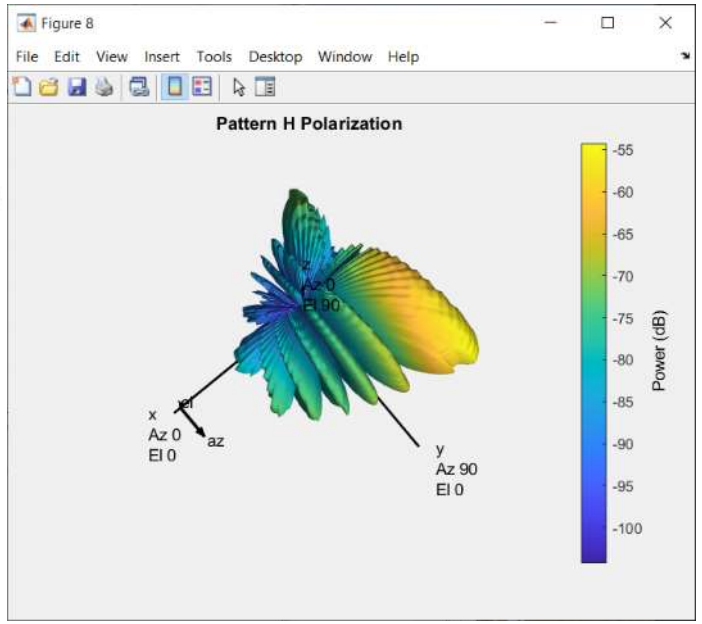




AiM Receiver



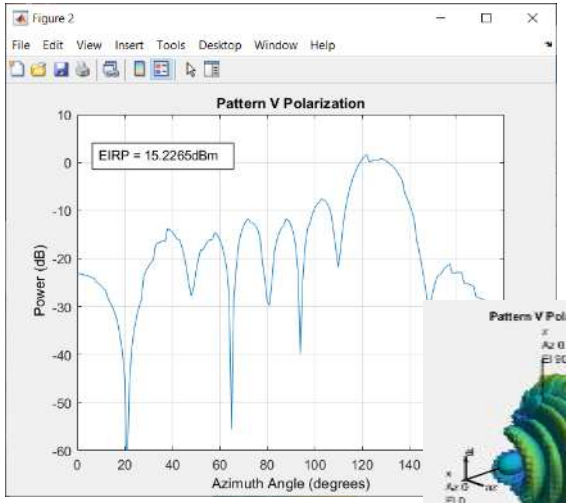


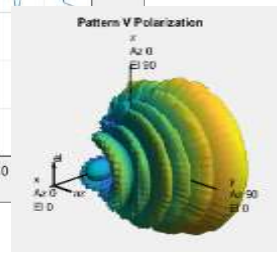


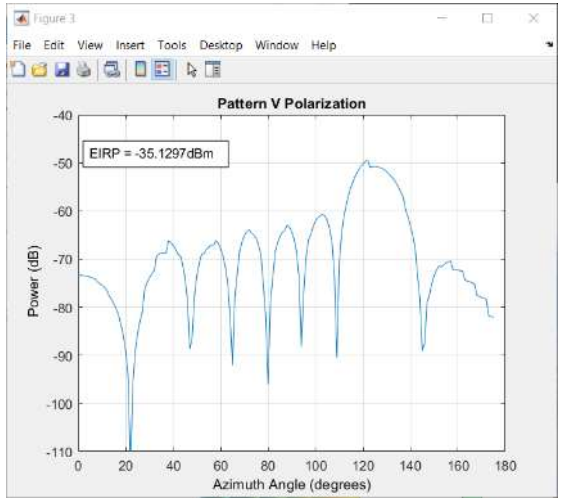
Transmitter + Receiver Chain

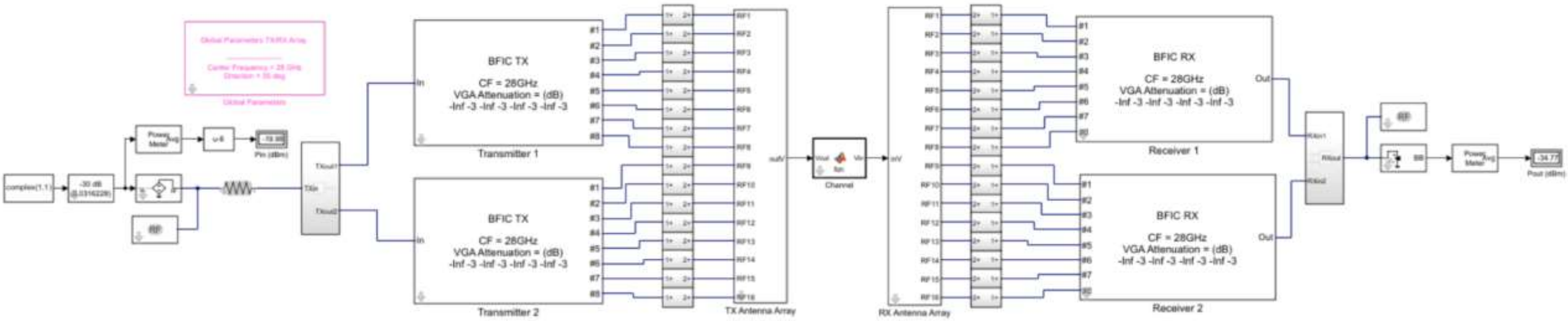
Link budget analysis

- Losses vs frequency
- Direction of arrival/departure
- Channel models
- Polarization mismatches
- Noise
- Non-linearity

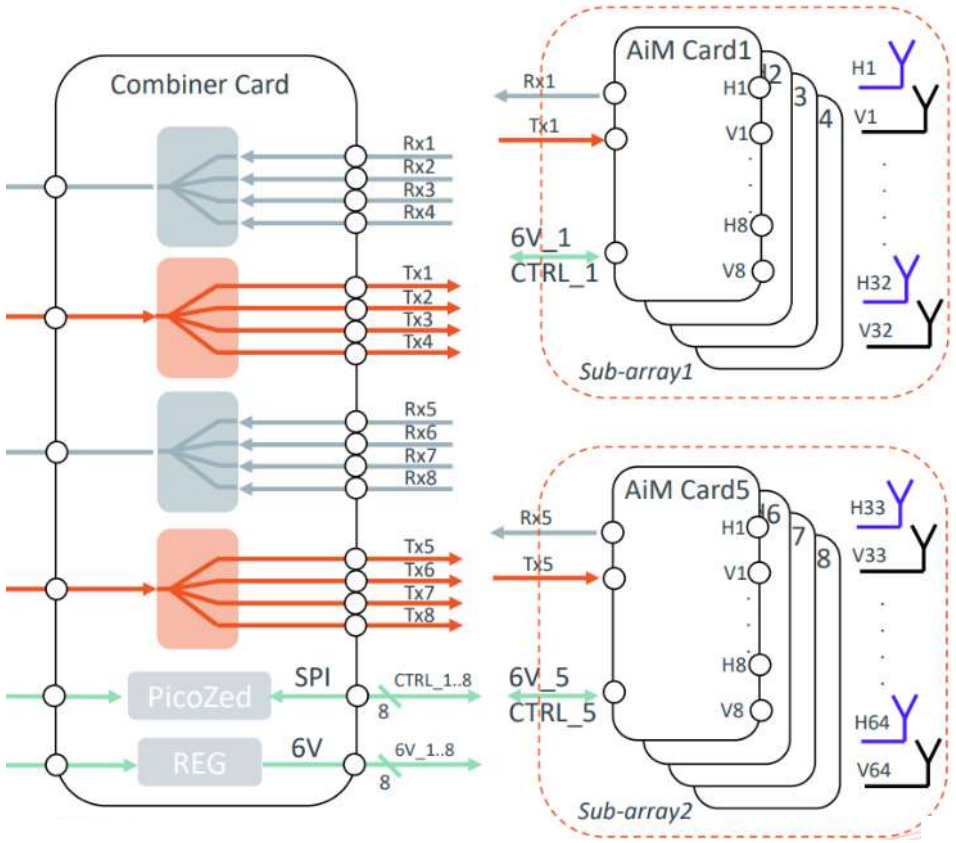


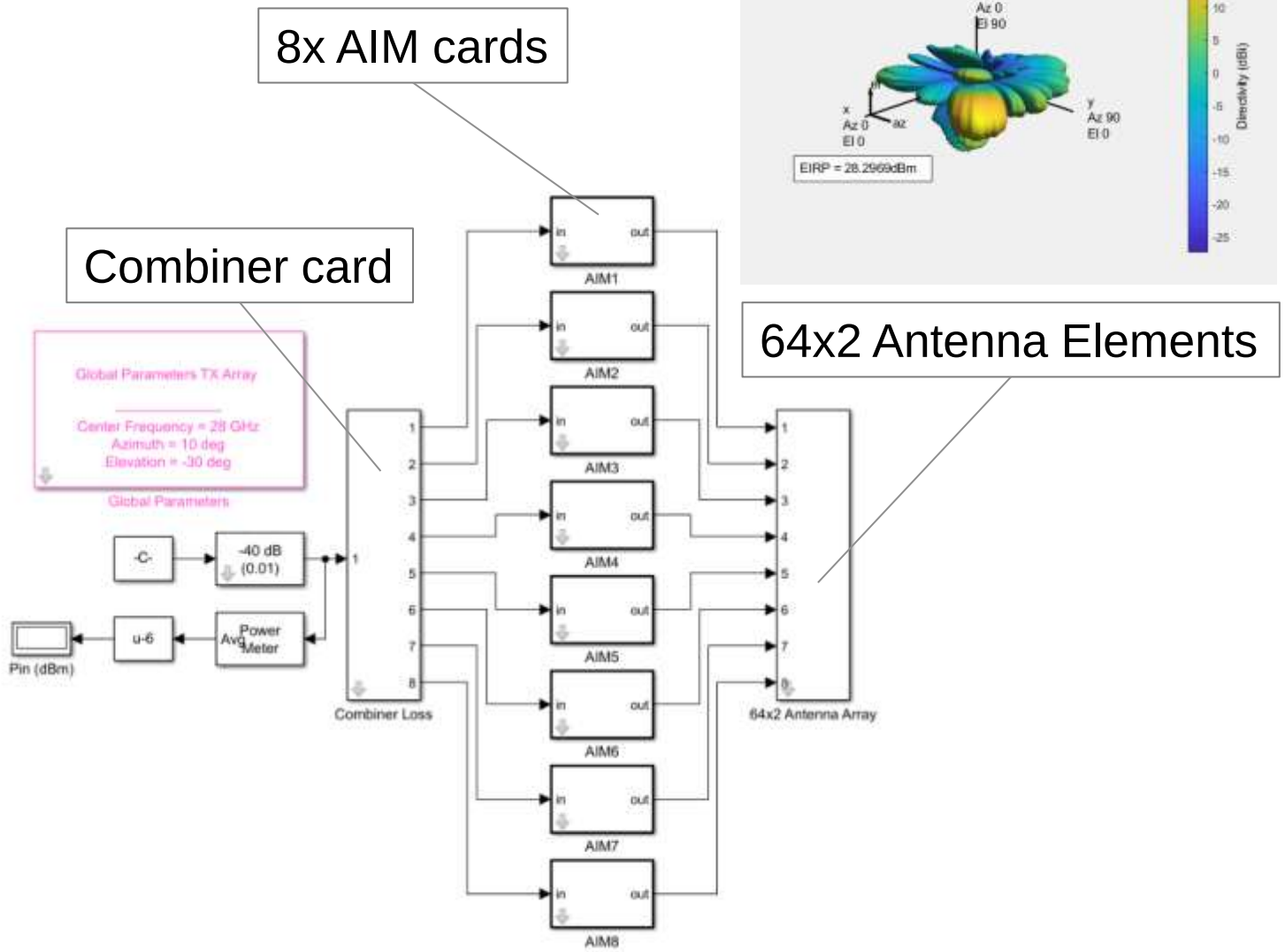




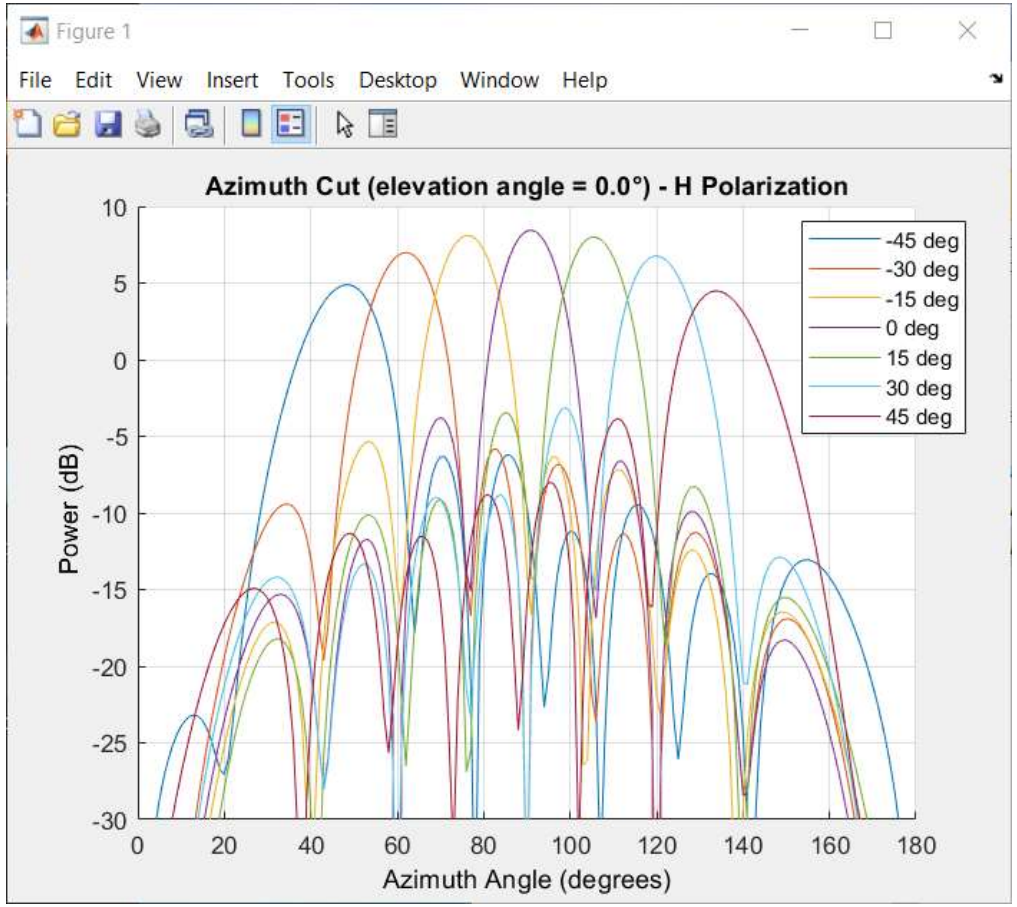


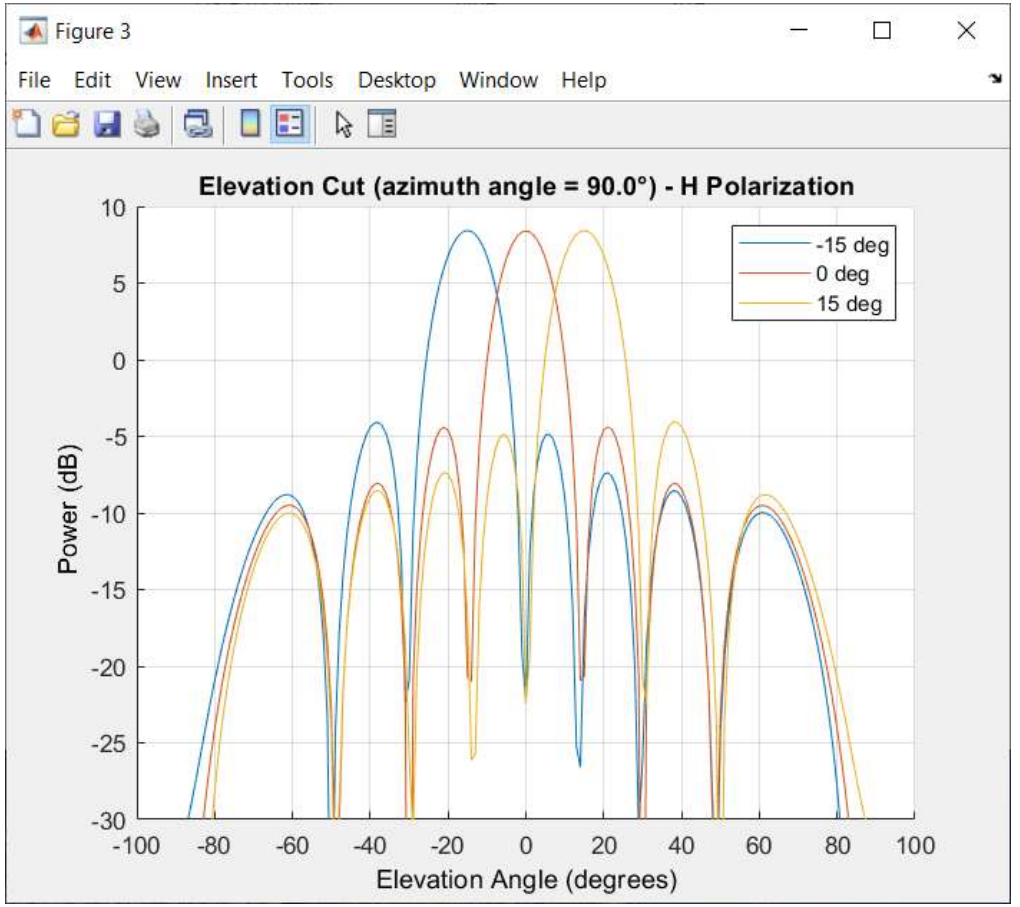
PAAM Module: Enabling Beamforming



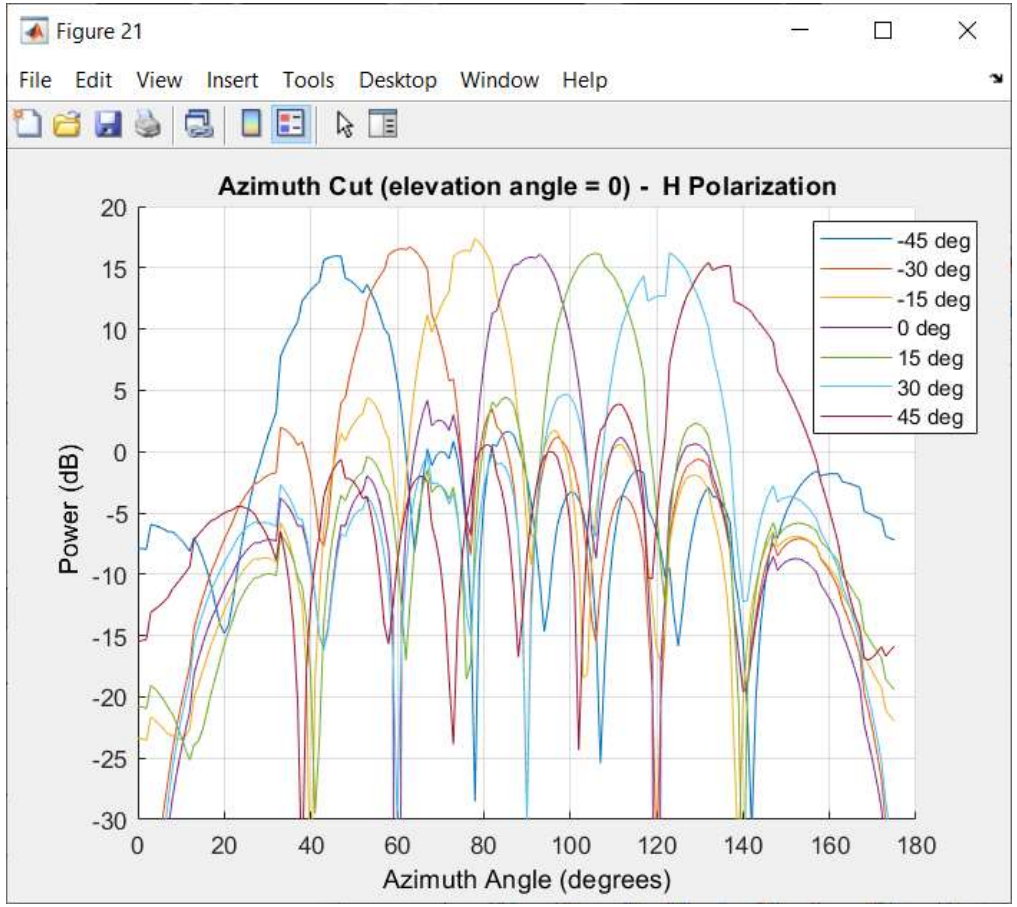


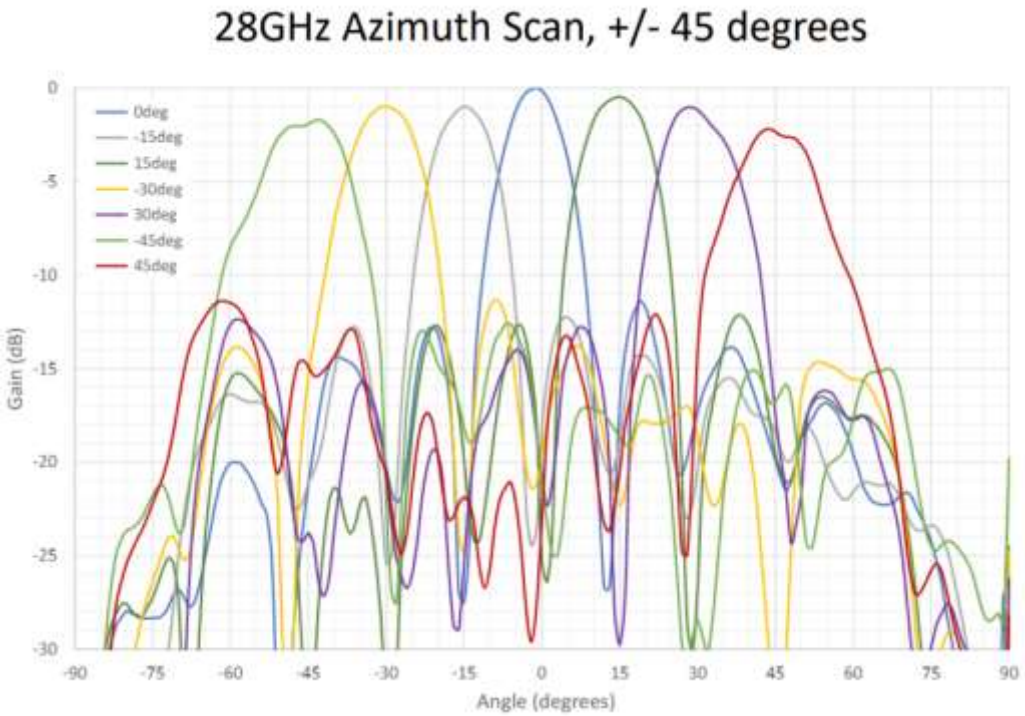
Beam Scanning PAAM Model – H Polarization (Ideal Elements)



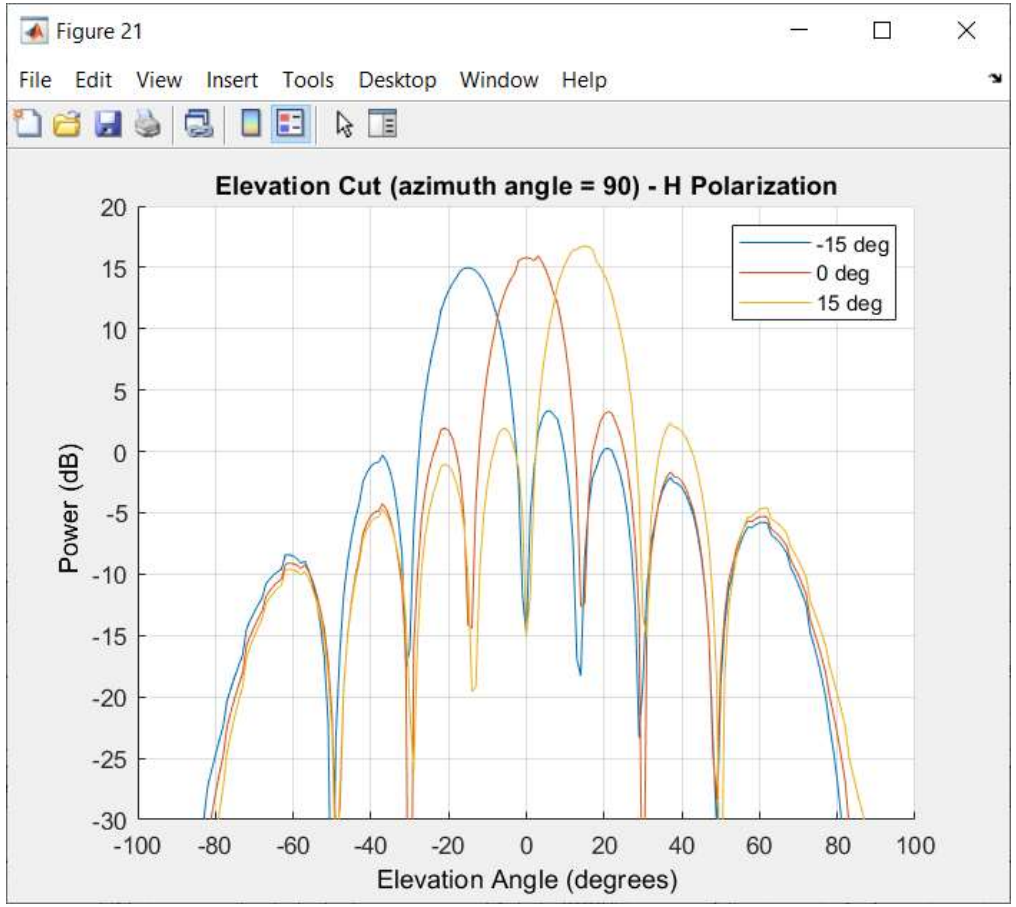


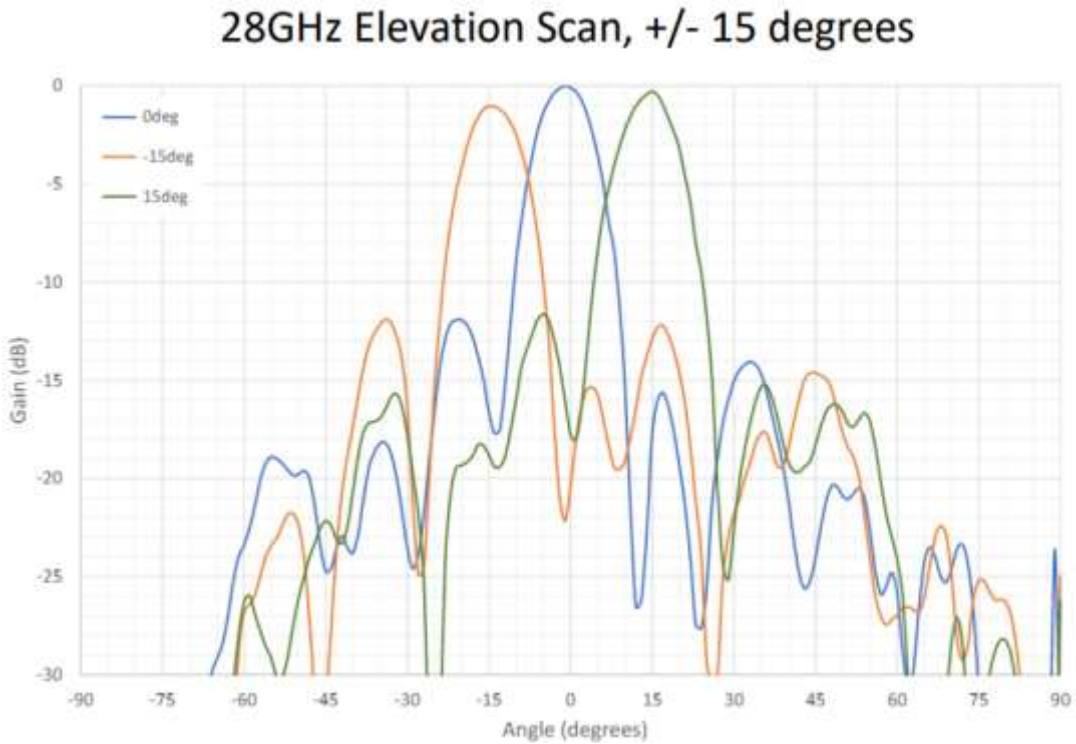
Beam Scanning PAAM Model – H Polarization (Measured Elements)



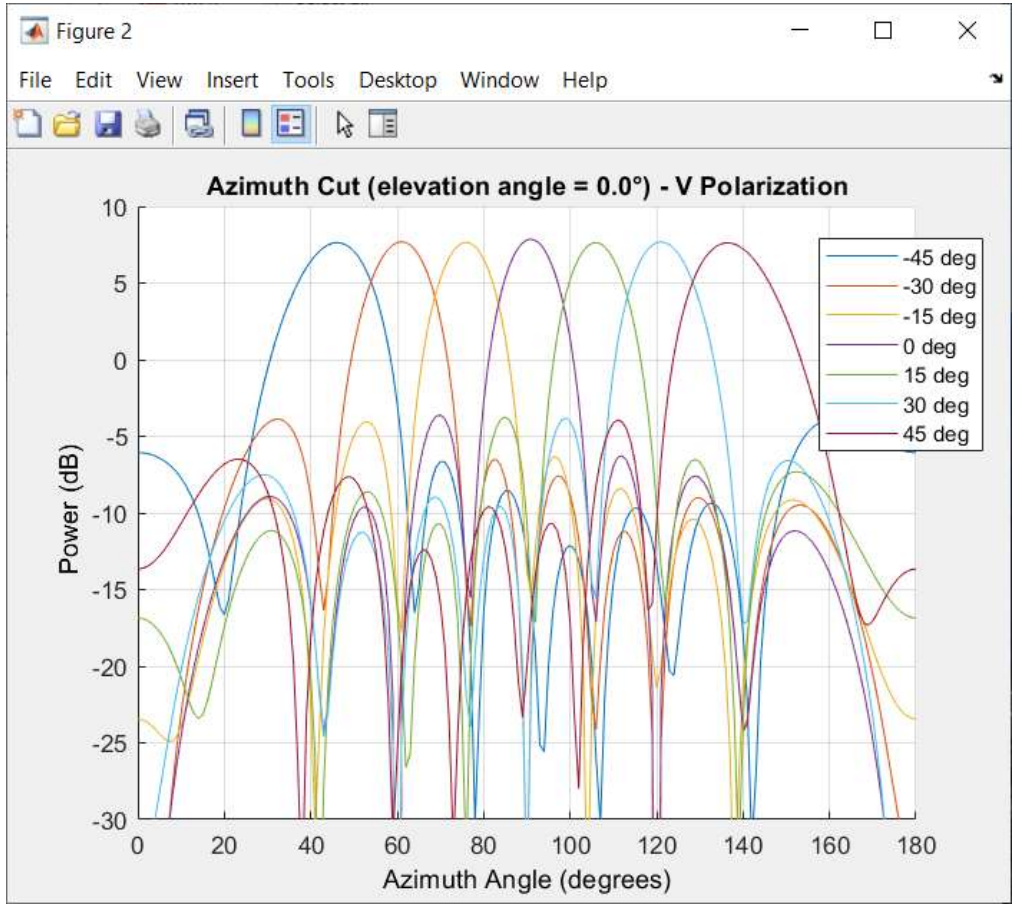


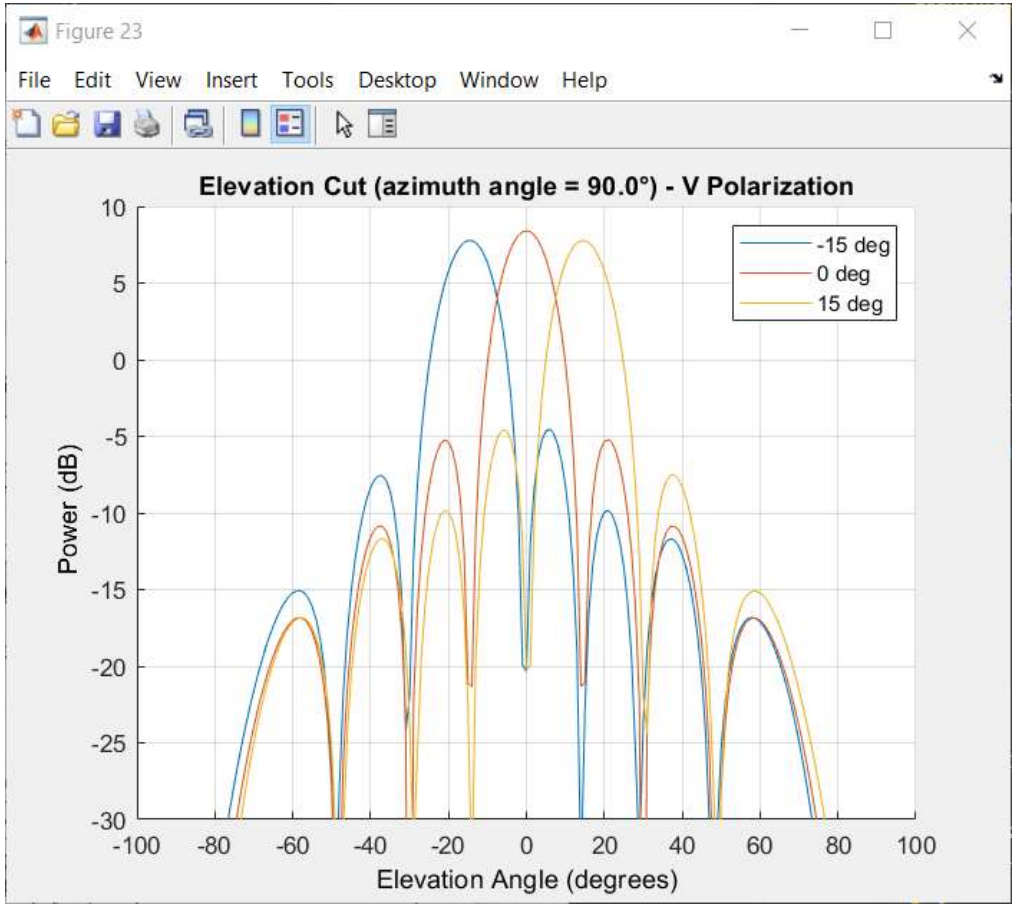
Beam Scanning PAAM Model – H Polarization (Measured Elements)



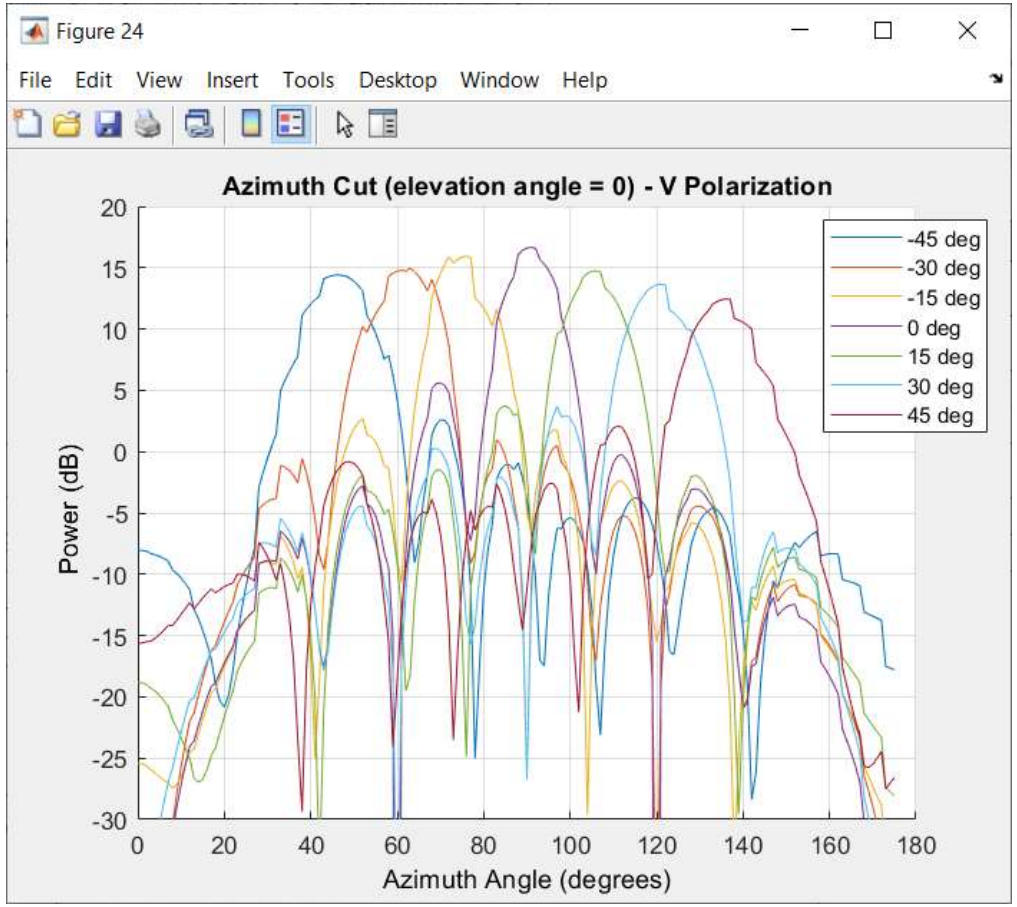


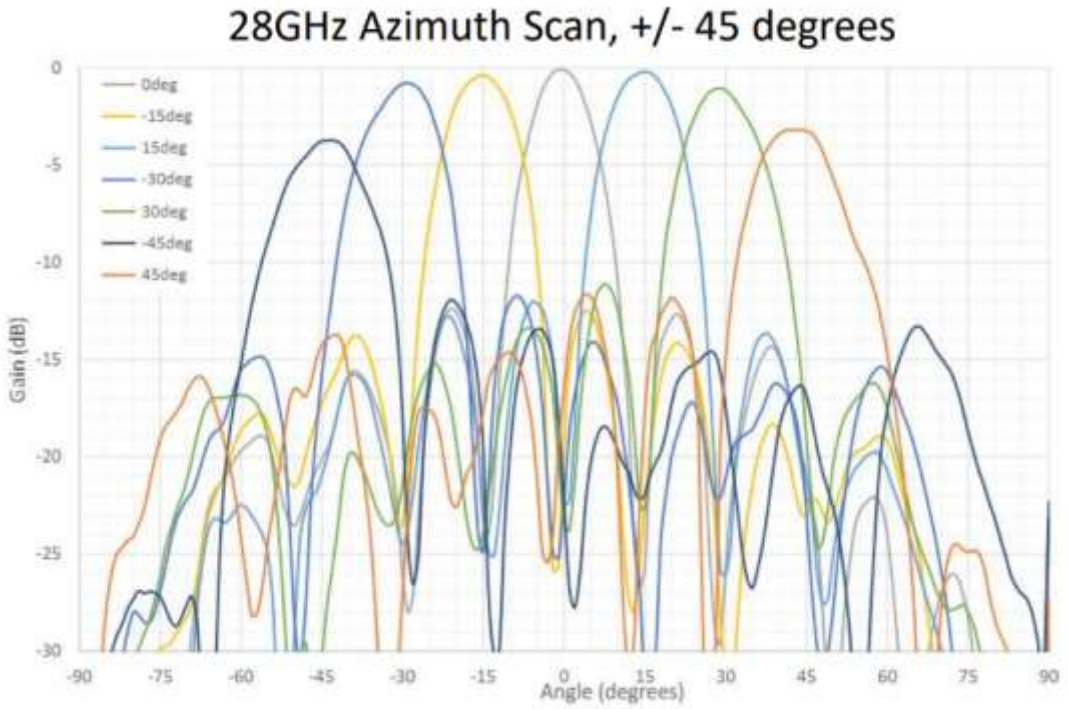
Beam Scanning PAAM Model – V Polarization (Ideal Elements)



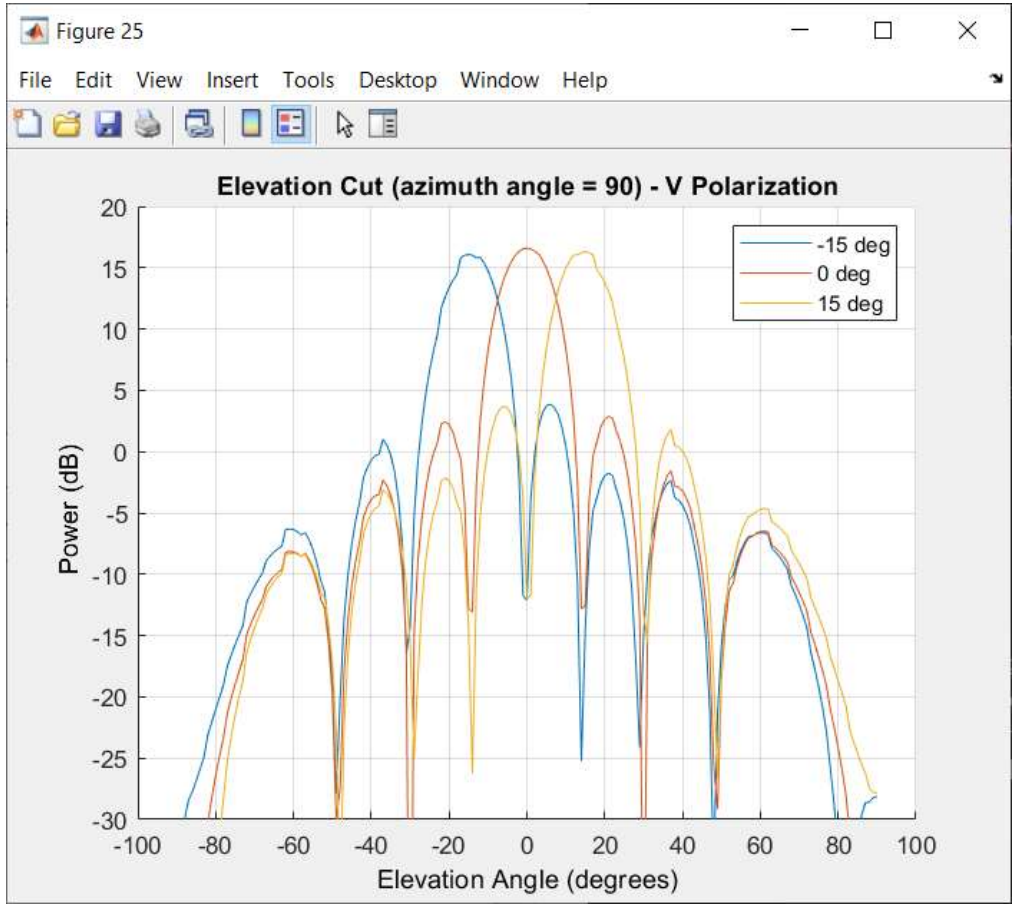


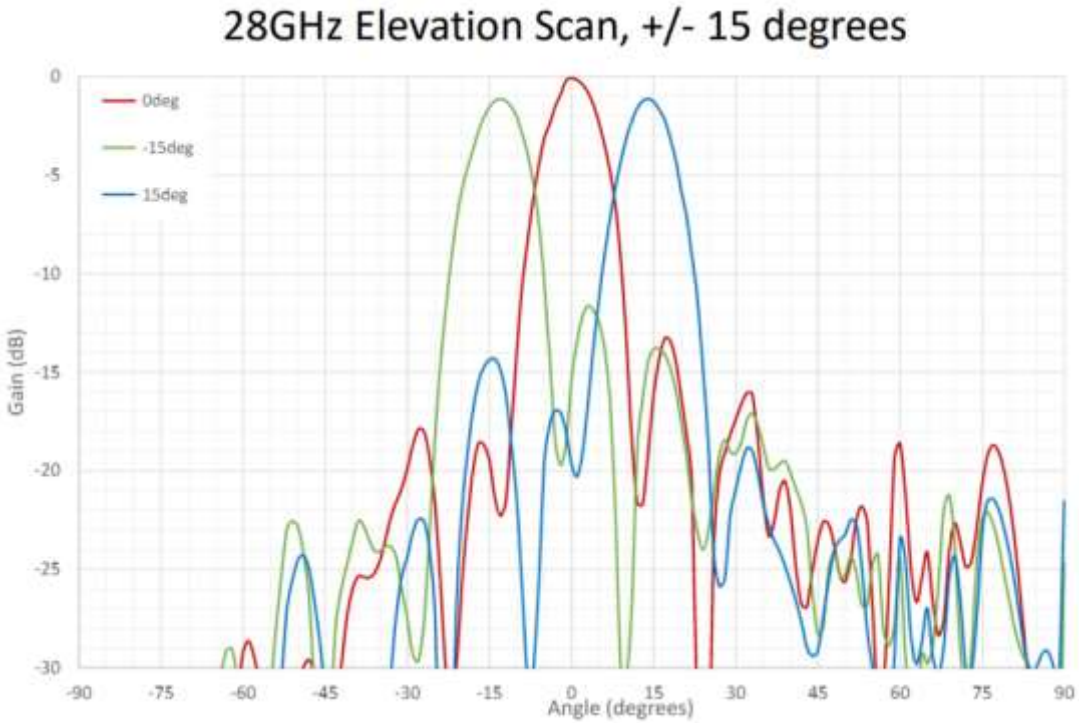
Beam Scanning PAAM Model – V Polarization (Measured Elements)



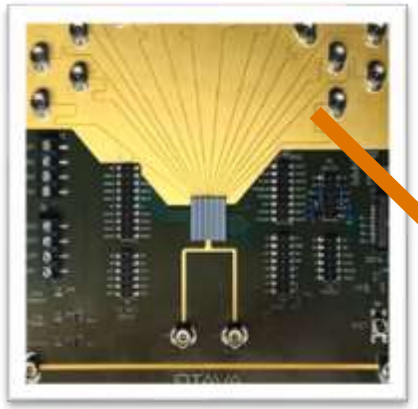


Beam Scanning PAAM Model – V Polarization (Measured Elements)



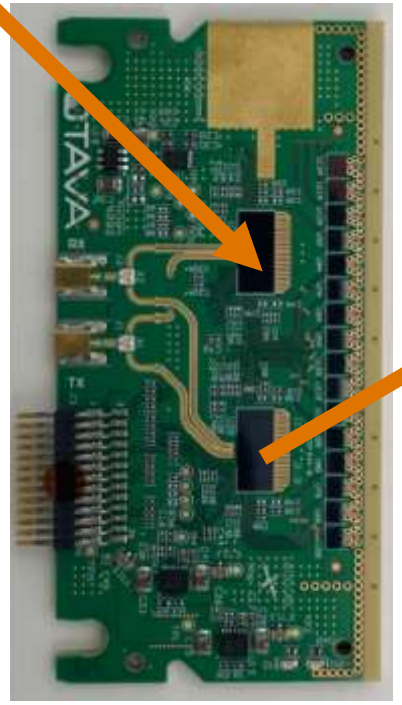


Conclusions: Modeling from IC to Board to Full System

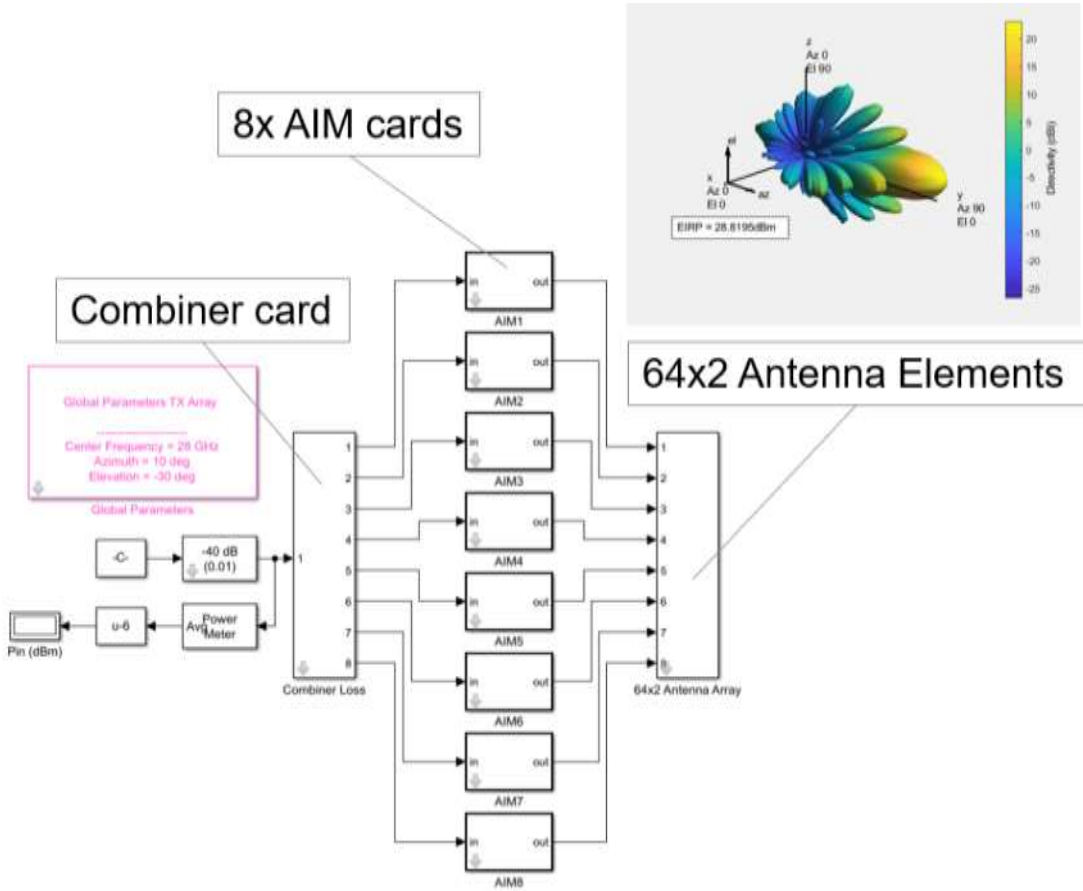


OTBF103

AIM Card

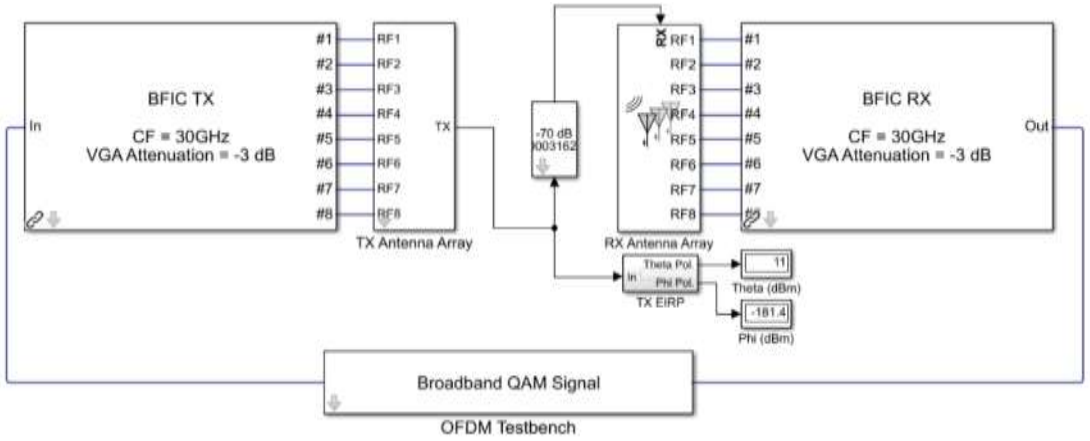


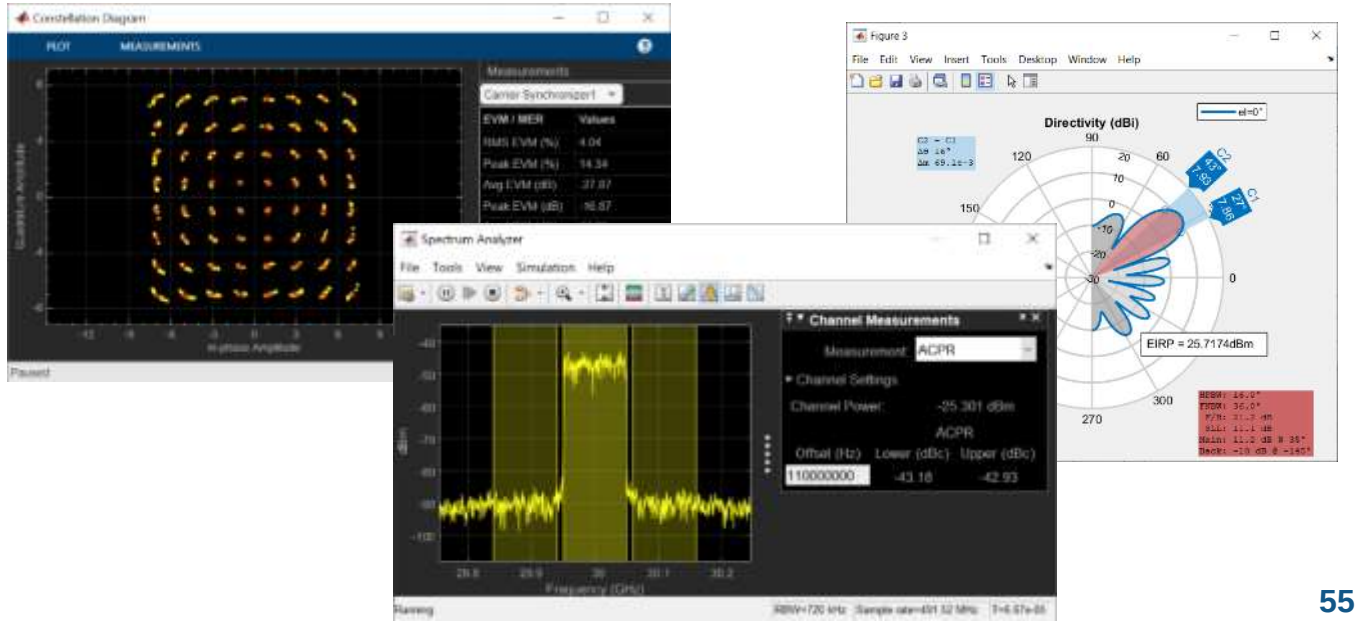
PAAM System



Summary

- BFIC models based on actual measurements and reproducing lab-results
- Testbenches for performance verification: gain, IP3, NF, S-parameters
- Integration with antenna arrays for beamforming applications
  - Full-wave EM analysis to compute impedance, pattern, polarization
- End-to-end simulation for system-level integration
  - Circuit envelope multi-carrier RF simulation for high-frequency and broadband applications





For Follow-Up and Contact Information

- For model inquiries, please email Otava at hello@otavainc.com
- Or fill out a request form at https://www.otavainc.com/products/otbf103

- Learn more about RF Blockset and Antenna Toolbox:
  - https://www.mathworks.com/products/rf-blockset.html
  - https://www.mathworks.com/products/antenna.html

Digital Signal Processing at Baseband

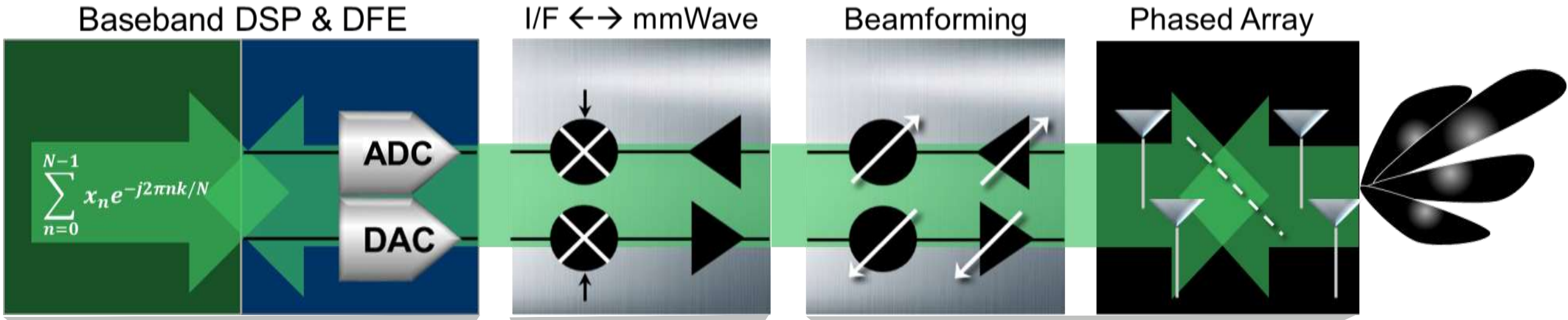
Signal integrity starts in the digital domain

Luc Langlois

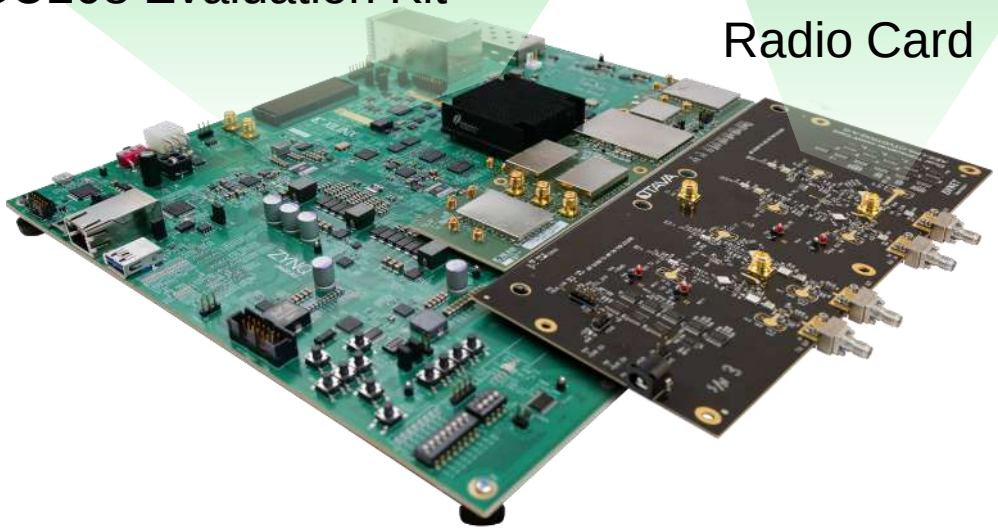
Director, Advanced Applications / 5G

Avnet Embedded

mmWave Phased Array from Digital to RF



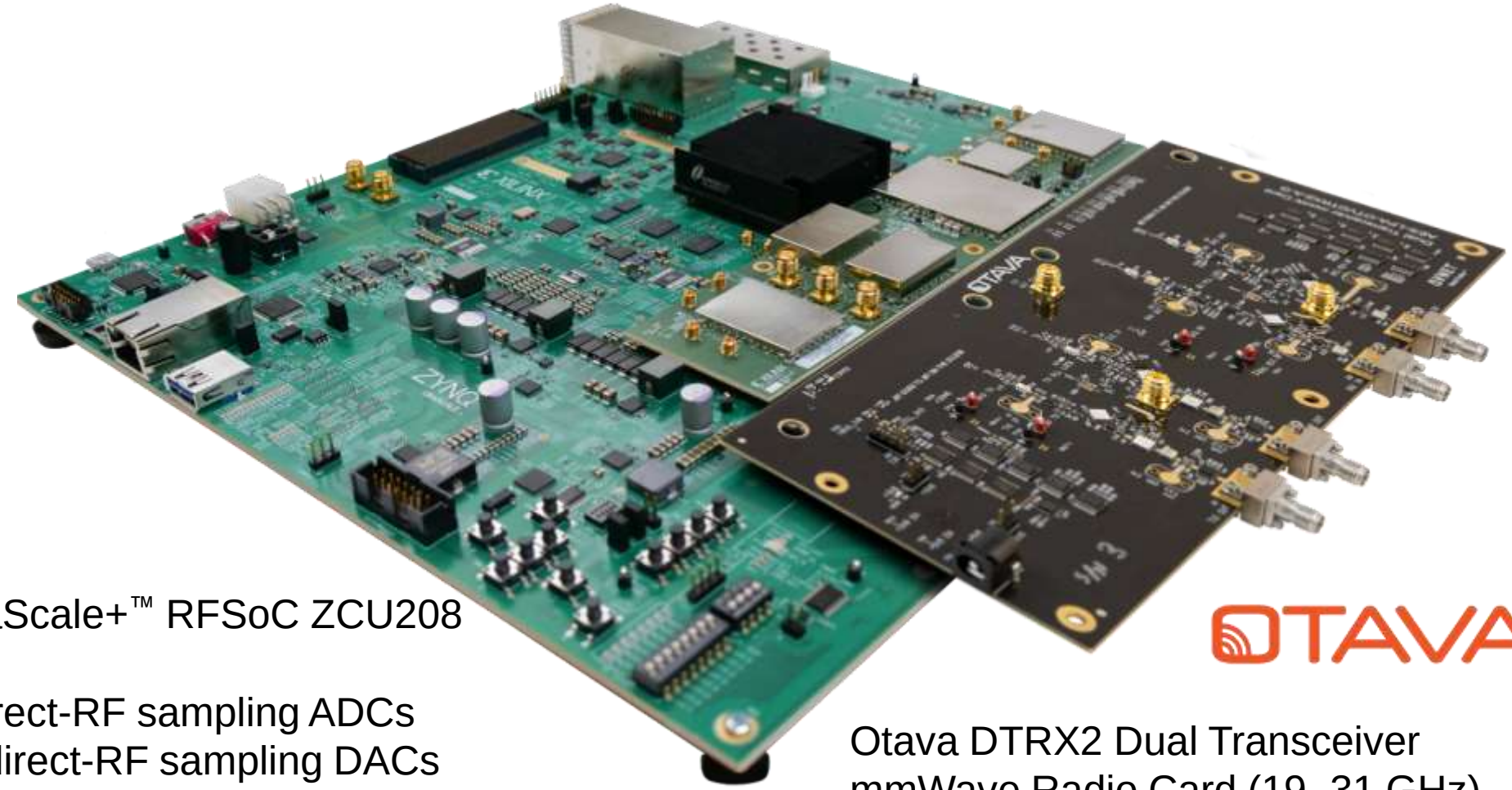
AMD Zynq UltraScale+ RFSoC
ZCU208 Evaluation Kit



Otava
DTRX2 mmWave
Radio Card

Otava Phased Array
Antenna Module (PAAM)

Avnet Wideband mmWave Radio Development Kit for AMD RFSoC Gen-3



AMD/Xilinx Zynq® UltraScale+™ RFSoC ZCU208 Evaluation Kit
8 x 14-bit, 5.0 GSPS direct-RF sampling ADCs
8 x 14-bit, 9.85 GSPS direct-RF sampling DACs
6 GHz analog bandwidth

Otava DTRX2 Dual Transceiver mmWave Radio Card (19–31 GHz)

Zynq UltraScale+ RFSoC with mmWave Up/Down-converter

AMD

ZYNQ RFSoC

Zynq US+ RFSoC Gen-3

Processing System
Quad ARM Cortex-A53
Dual ARM Cortex-R5

Programmable Logic
489K – 930K System Logic Cells
1872 – 4272 DSP Slices

8/16 channels

RF DAC

DUC

RF DAC

Direct RF Sampling

8/16 channels

SD FEC

RF ADC

DDC

RF ADC

GTY
28Gb/s

CPRI, 10GE, 25GE, ..

..10010010101011101010 1…

..10010010101011101010 1…

Digital Baseband

IF out
0 – 6 GHz

RF out
19 – 31 GHz

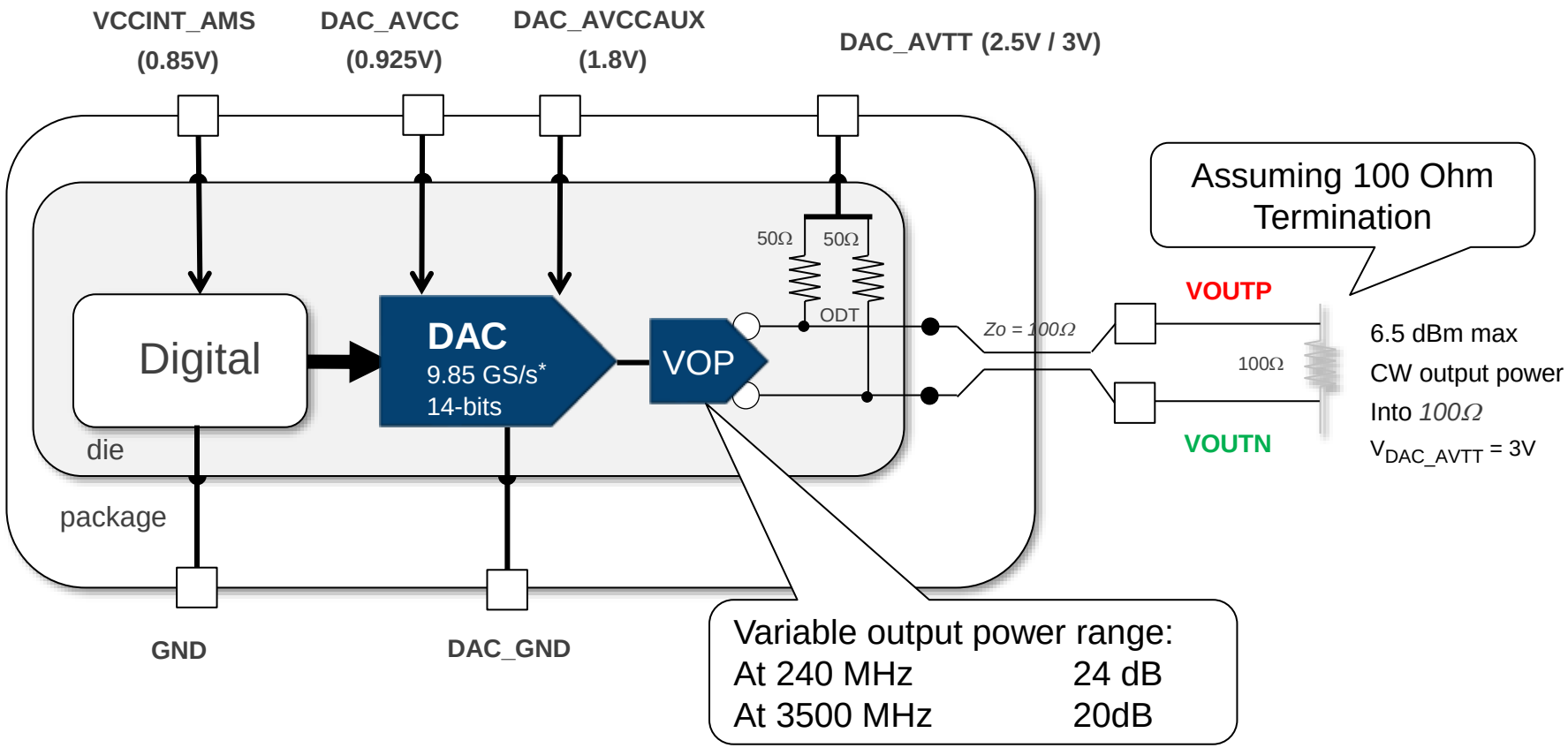
re-construction

anti-alias

IF in
0 – 6 GHz

RF in
19 – 31 GHz

RFSoC Gen-3 DAC with Variable Output Power



Maximize dynamic range in digital domain; adjust output power in analog domain

* **ZU4xDR** -2E, -2I, -2LI speed grade without clock forwarding, datapath modes 2, 3, and 4

Ref: https://docs.xilinx.com/r/en-US/ds926-zynq-ultrascale-plus-rfsoc/RF-DAC-Electrical-Characteristics

RFSoC Gen-3 RF Sub-system with Signal Processing

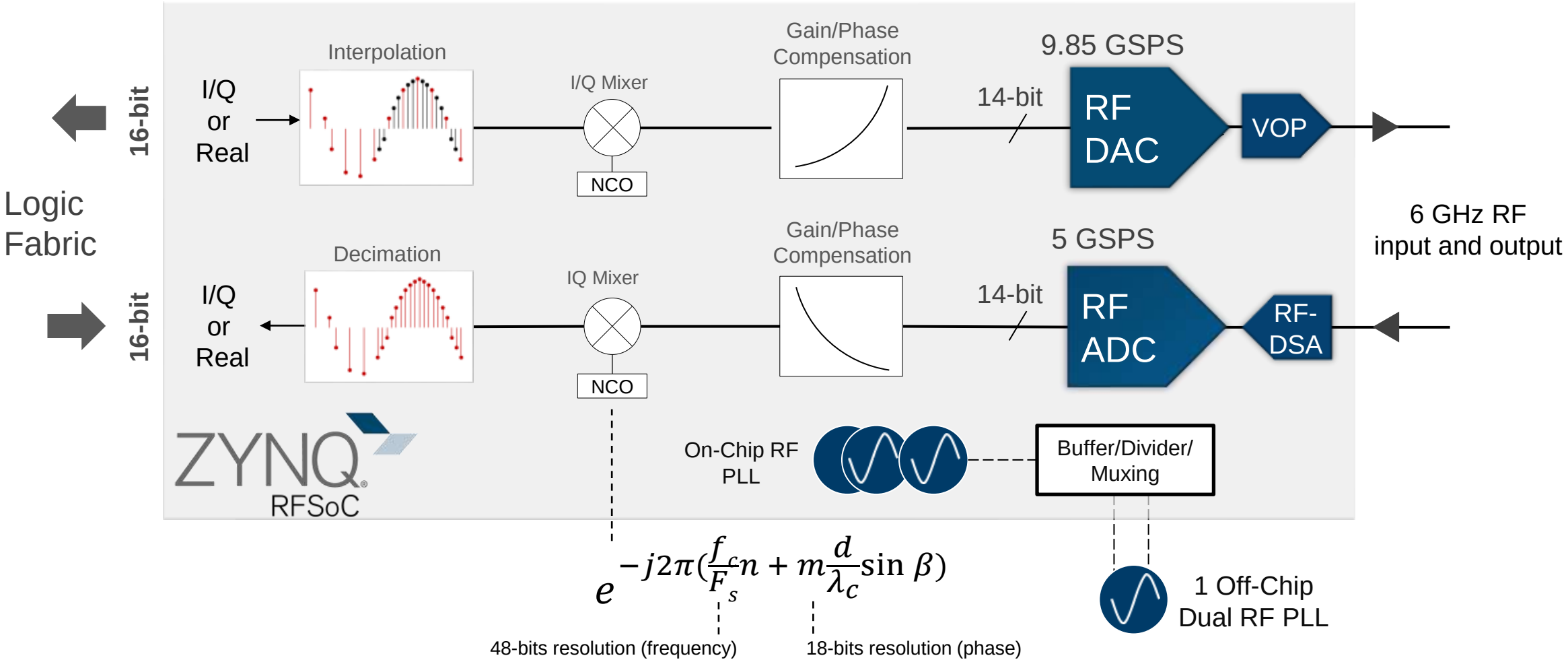
Ref: PG269 (v2.6) April 20, 2022 www.xilinx.com Zynq UltraScale+ RFSoC RF Data Converter Gen 1/2/3/DFE

Digital Mixing and Filtering

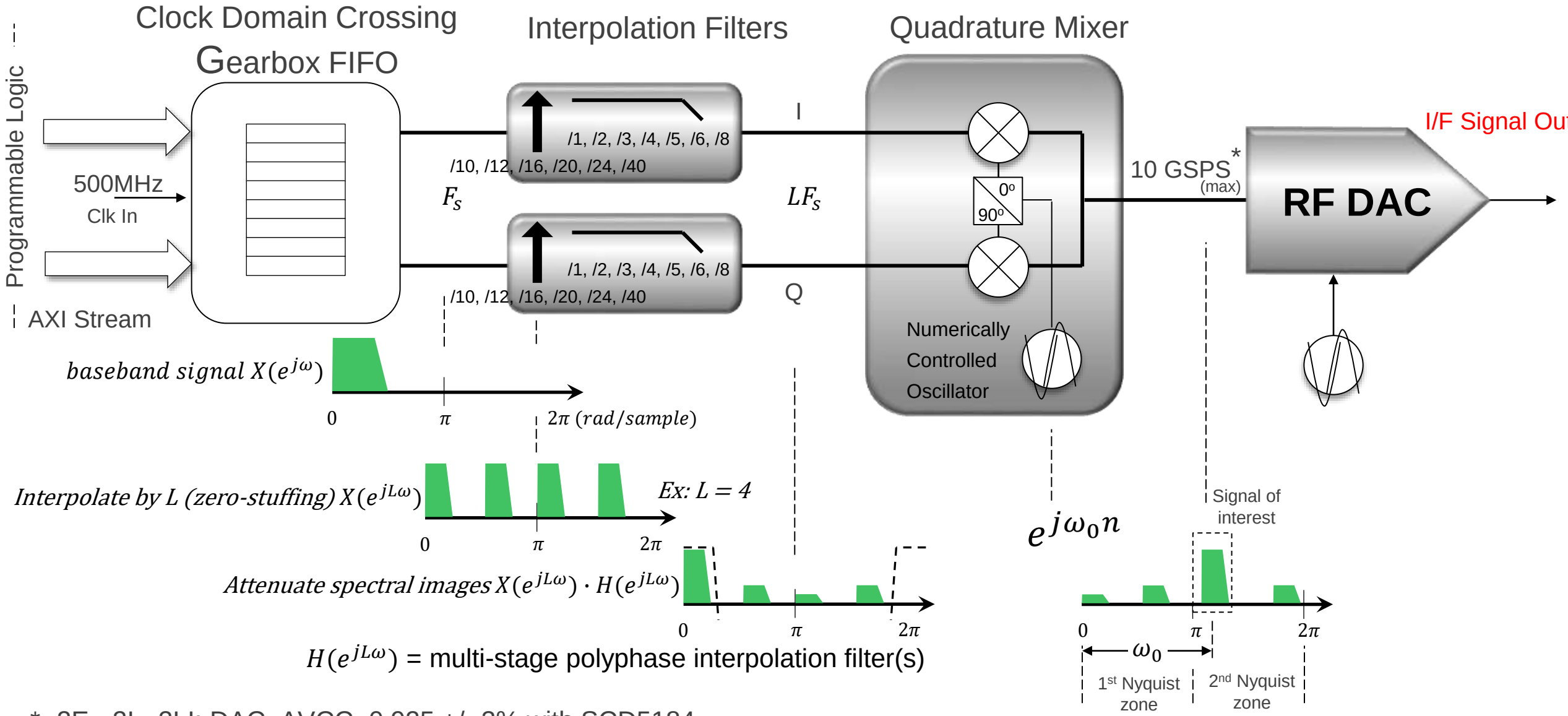
- Digital Up-Conversion and Down-Conversion

Direct-Sampling

- High channel count

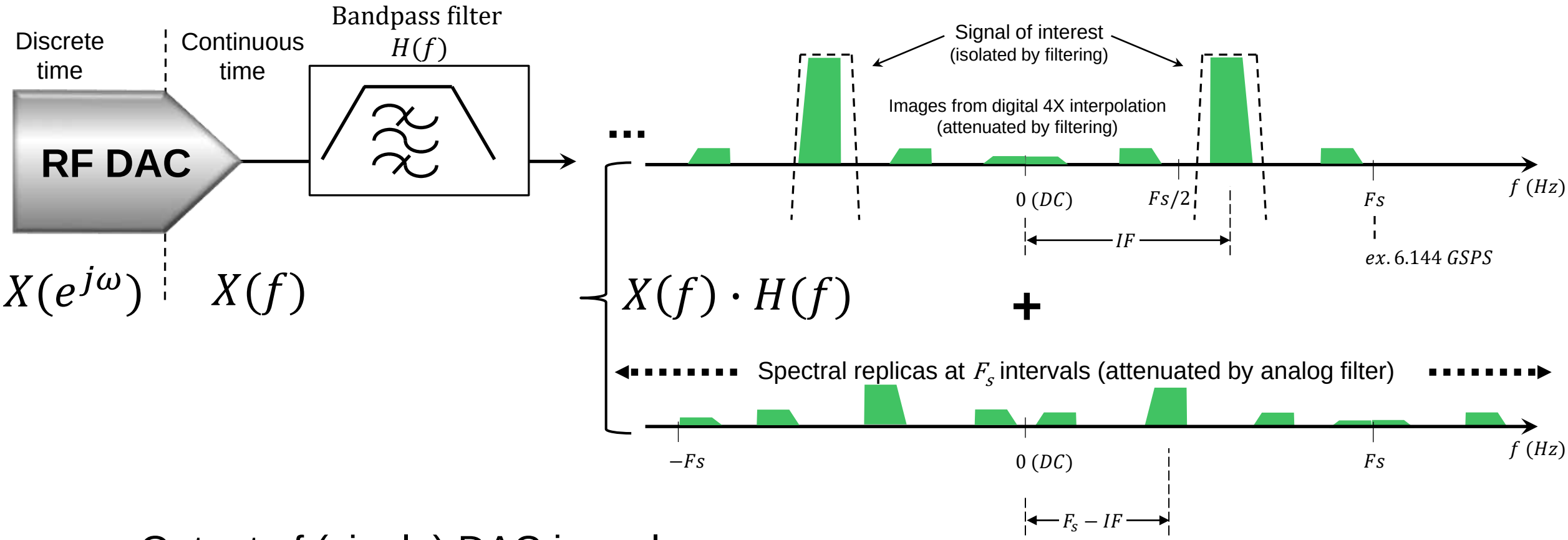


RFSoC Gen-3 Digital Up Converter (DUC)



* -2E, -2I, -2LI: DAC_AVCC=0.925 +/- 3% with SCD5184

RF-DAC Output + Bandpass Re-construction Filter



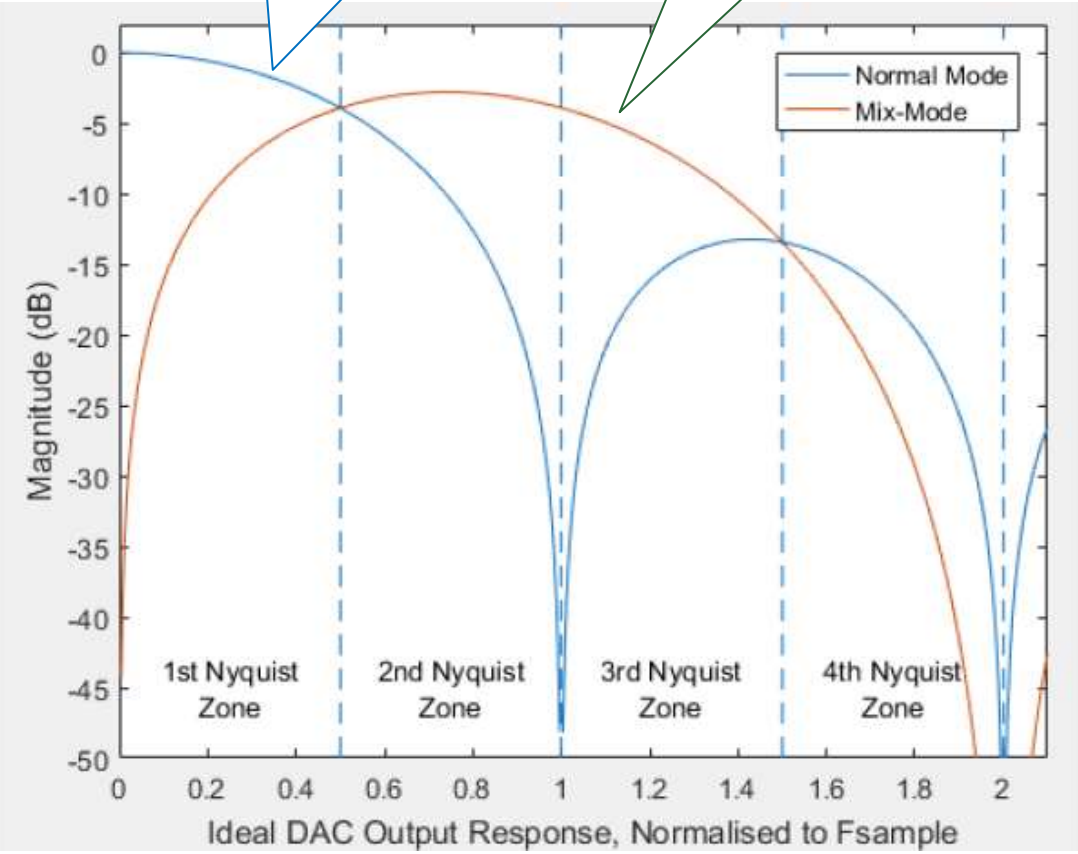
- Output of (single) DAC is real
- Images from digital interpolation below the noise floor with frequency planning
- Beware sampling clock phase noise for signal of interest in higher Nyquist zones

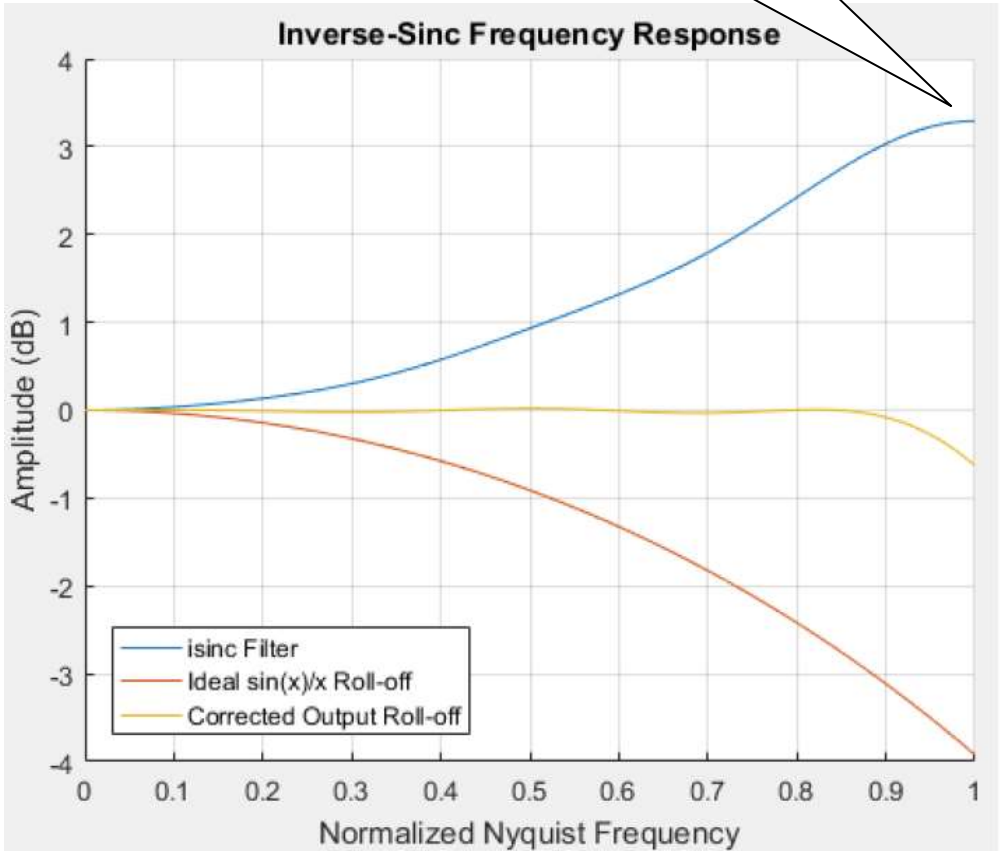
RFSoC Gen-3 DAC Frequency Response

DAC output power rolls off with sinc shape that results in a lot of power loss in 2nd Nyquist zone

Using mixed mode boosts power in 2nd Nyquist Zone at the cost of lower 1st Nyquist

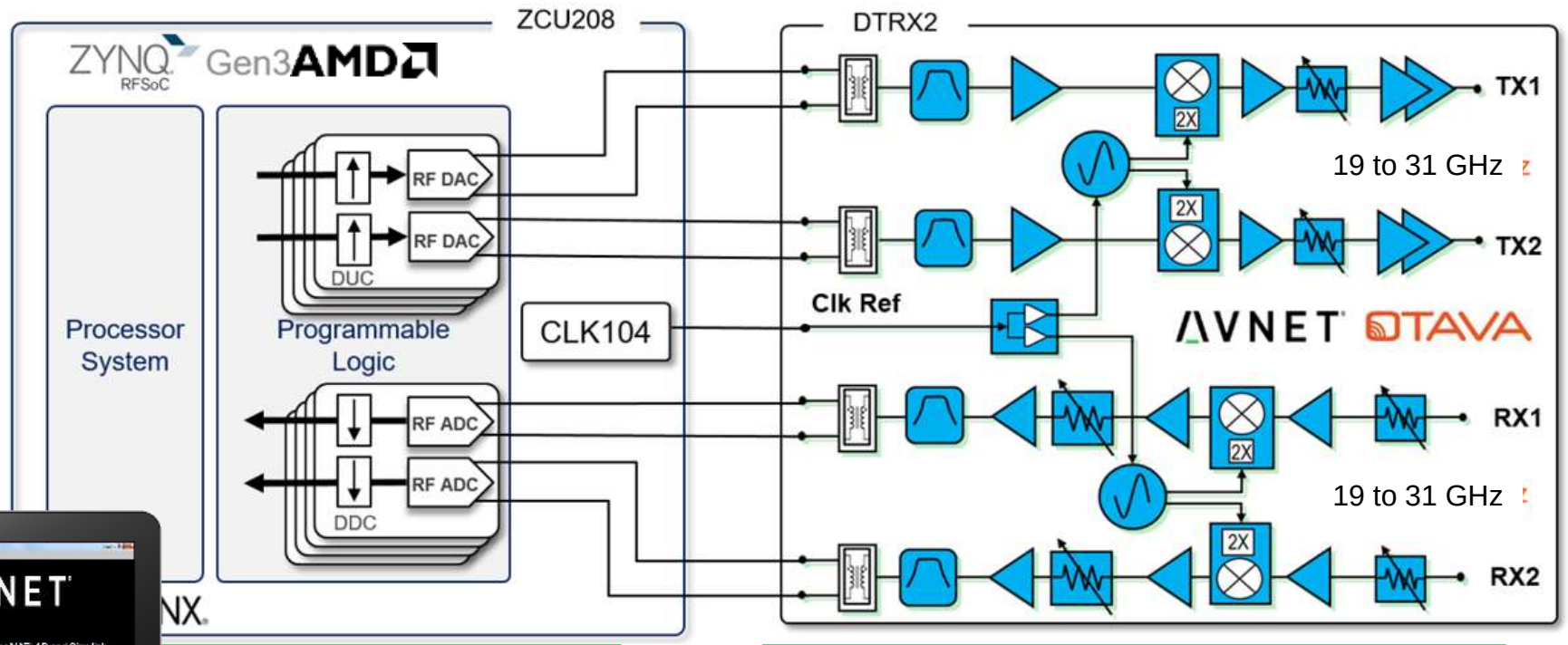
Sinc roll off in the 1st Nyquist zone can be compensated using an inverse sinc response filter





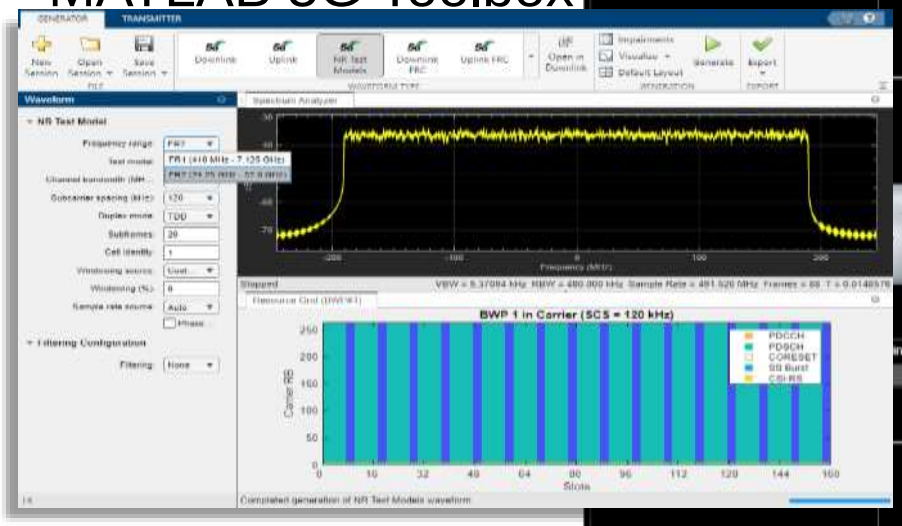
Avnet RFSoC Explorer® MATLAB App supports DTRx2

- Interface AMD RFSoC to MATLAB®
- Programmatic control of RF-ADC and RF-DAC parameters
- Control Otava DTRX2 mmWave Radio Card



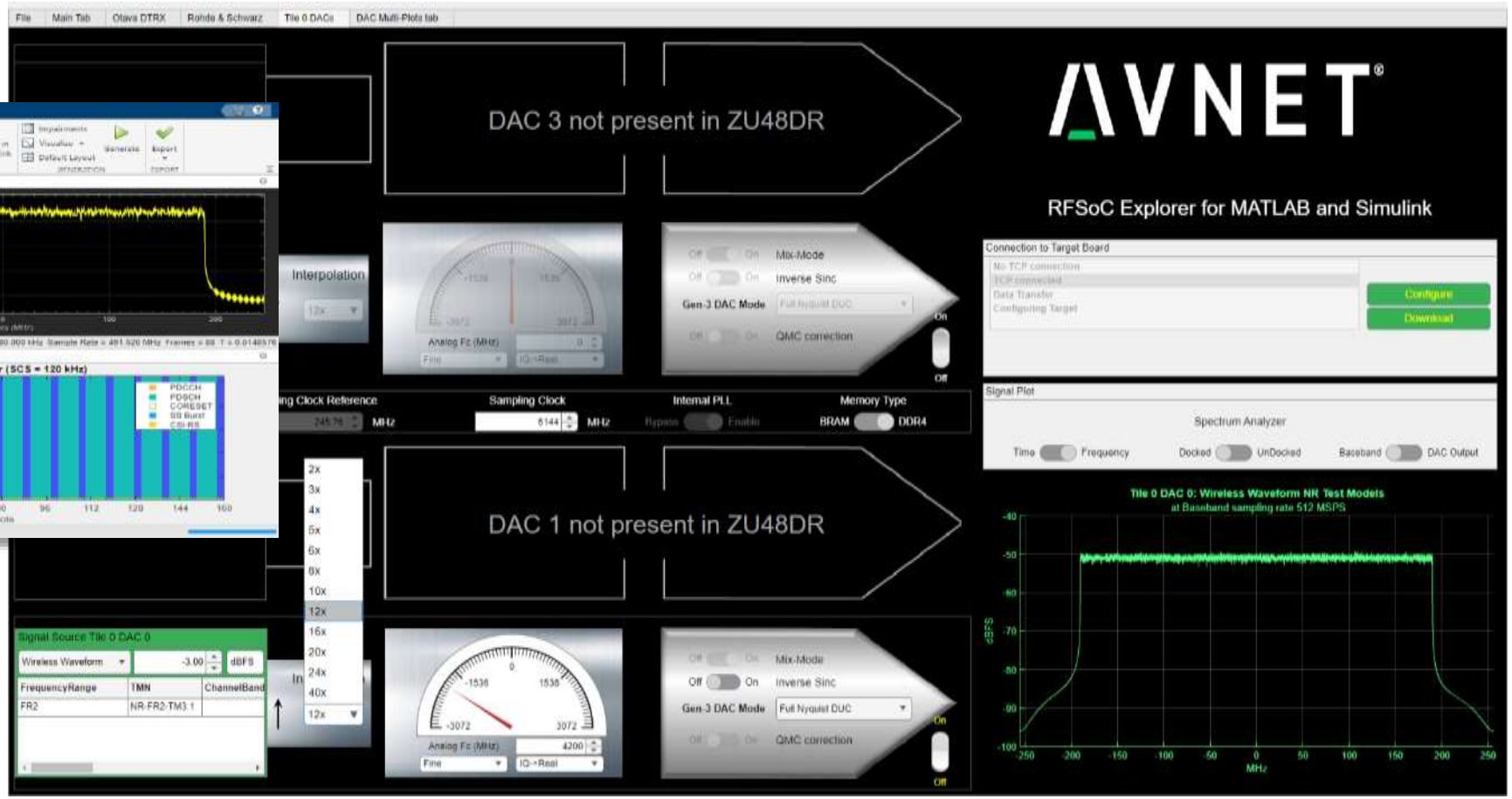
Avnet RFSoC Explorer – Native MATLAB Application

MATLAB 5G Toolbox



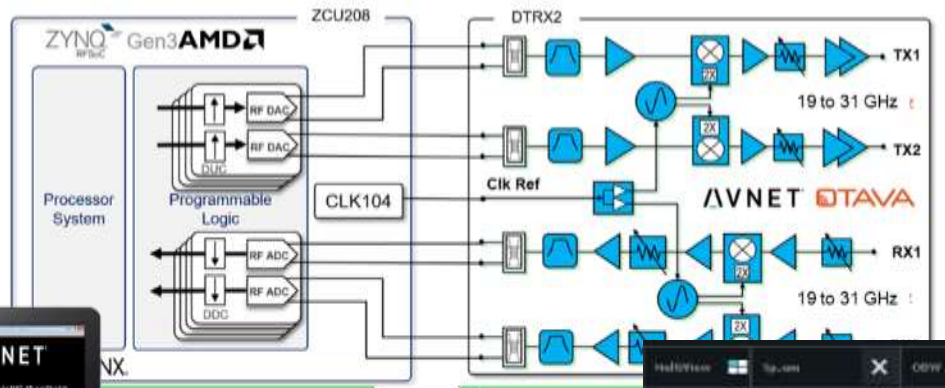
Simulate, analyze, and test the physical layer of 5G

MathWorks®
MATLAB® & SIMULINK®



Create waveforms in MATLAB → Control RFSoC in MATLAB → Capture & analyze in MATLAB

Signal Quality at mmWave / 5G NR TM 400 MHz



FSW 43 GHz

RF out = 27.9GHz
IF = 4.0152GHz
DUC interpolation = 5x
DAC sampling rate = 6.144Gs/s
DAC back off = -2dB
DSA attenuation level = -7.5dB
Pout = 0.5dBm RMS

References

AMD Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics (DS926)

https://docs.xilinx.com/r/en-US/ds926-zynq-ultrascale-plus-rfsoc

AMD Zynq UltraScale+ RFSoC RF Data Converter Gen 1/2/3/DFE LogiCORE IP Product Guide (PG269)

https://docs.xilinx.com/r/en-US/pg269-rf-data-converter

RF Data Converter Interface User Guide (UG1309)

https://docs.xilinx.com/r/en-US/ug1309-rf-data-converter-interface/RF-Analyzer

Avnet Boards Forums → RFSoC Boards

https://community.element14.com/products/devtools/avnetboardscommunity/avnetboard-forums/f/rfsoc-hardware-design

References

CLK104 RF Clock Add-on Card User Guide

https://www.xilinx.com/support/documents/boards_and_kits/zcu216/ug1437-clk104.pdf

Avnet RFSoC Explorer - File Exchange - MATLAB Central (mathworks.com)

https://www.mathworks.com/matlabcentral/fileexchange/73665-avnet-rfsoc-explorer

AMD XILINX

Appendix A

SAMTEC LPAM Host Interface Connector

The CLK104 RF clock add-on card mates with RFSoC evaluation boards using a low profile, 120-pin, high-speed SAMTEC LPA connector. The following figure shows the mezzanine module connector pin-out and the table that follows identifies the pins.

Figure 8: **LPA Connector Pin-out**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
B	G	ADC_REFCLK	G	CLK_SPI_MUX_SEL0/1	G	AMS_REFCLK	G	G	PL_SYSREF	G	PL_CLK	G	DDL_PLY_SYNC	G						
C	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
D	G	G	G	G	3V3	3V3	G	G	G	G	G	5V0	5V0	G	G	G	G	G	G	G
E	G	DAC_REFCLK	G	3V3	3V3	G		SYNC_IN	G	G	5V0	5V0	G	SFP_REC_CLK	G	SCLK	SDA	G		
F	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G

Table 6: **LPA Connector Pin Descriptions**

Pin	Signal Name	Description	LMK04828 Pin
E2	DAC_REFCLK_P	DAC REFCLK, routed to RFSoC DAC on board	DCLKout6*

Balancing Tradeoffs: Taming SI Challenges in mmwave Antenna-to-Bits Implementations

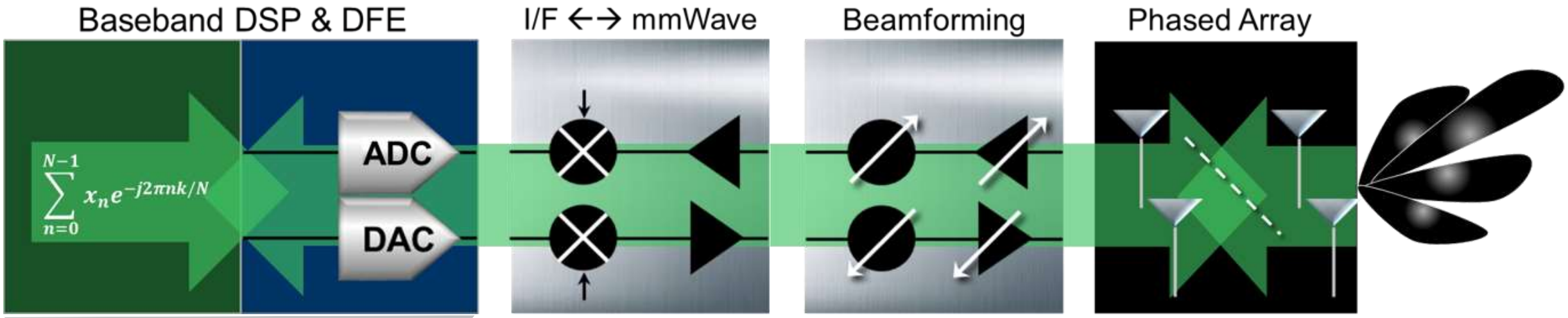
Matthew Burns | Technical Marketing Manager

June 15, 2023

INNOVATIVE TECHNOLOGIES • SUDDEN SERVICE • GLOBAL REACH

Samtec Confidential

Where's the High-Performance Interconnect?



AMD Zynq UltraScale+ RFSoC
ZCU208 Evaluation Kit

Otava
DTRX2 mmWave
Radio Card

Otava
PAAM

AMD ZCU208 + Otava DTRX2 Interconnect Options

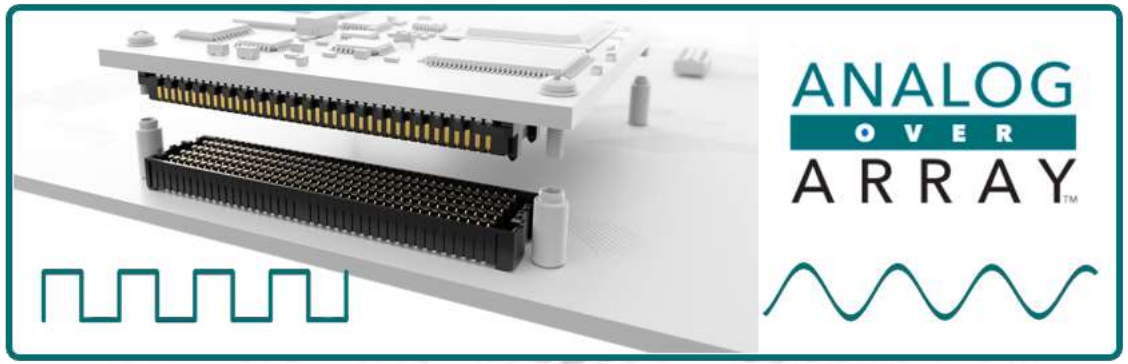
Design Challenge: Density and diversity of signals

- ADCs
- DACs
- Clocking
- Data
- Power

Traditional RF connector challenges:

- Connector misalignment
- Board real estate
- Cost

Design Solution: Samtec Analog over Array technology

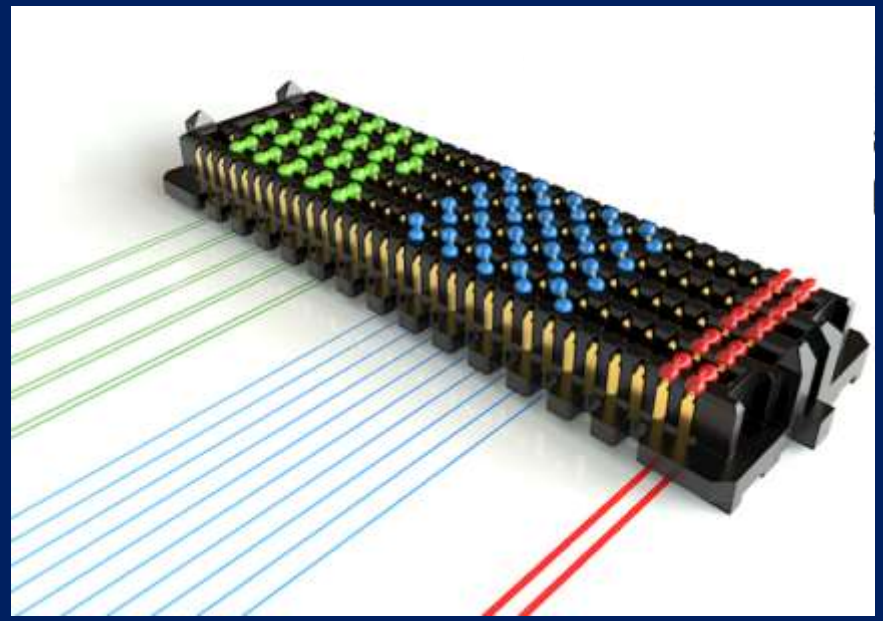


RFMC 2.0 interface provide access to the ADC/DAC, clocking and data path signals

Samtec Confidential

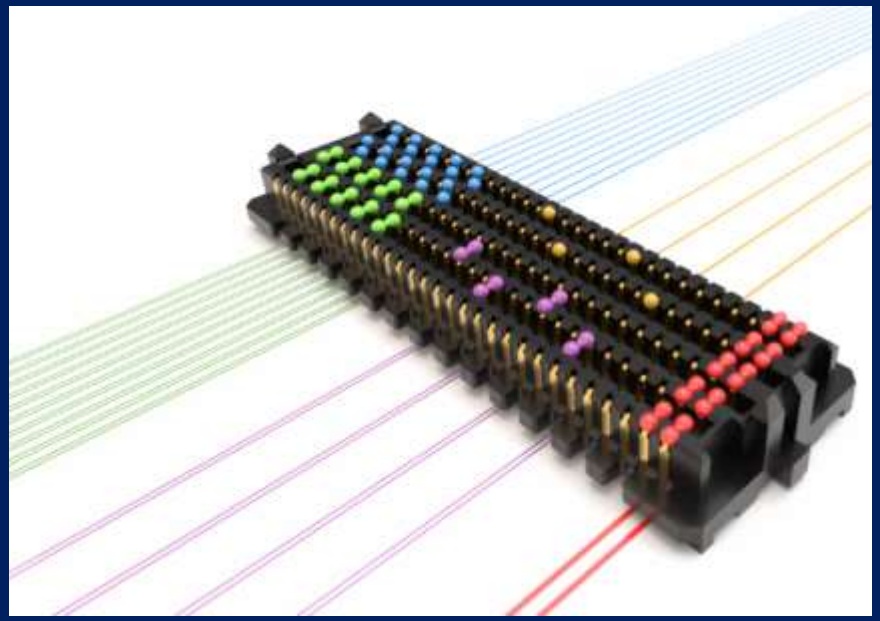
Samtec Analog over Array Technology

Current Open-Pin-Field Arrays



Digital DP
Digital SE
Power
Analog DP
Analog SE

Enhanced Analog over Array Technology



Key AMD Zynq UltraScale+ RFSoC Specs

Key Design Specifications:

Analog Bandwidth: 8.00 GHz

Crosstalk: -63 dBc (F_{IN} <= 8.00 GHz)

Return Loss: -10 dB (F_{IN} <= 8.00 GHz)

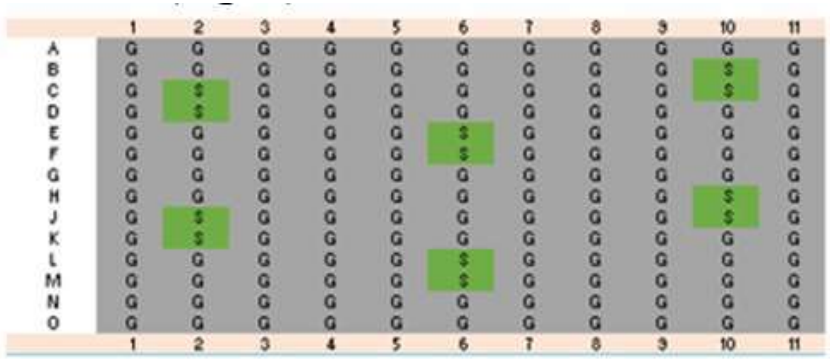
Analog input bandwidth[4]	Full-power bandwidth (–3 dB)	–	7.125	–	GHz
Return loss (R_L)[5]	Up to 4 GHz	–	–12	–	dB
	Up to 7.125 GHz	–	–10	–	dB
Optimized common mode voltage range	Performance optimized range. AC and DC coupling modes[6]	0.68	0.7	0.72	V
Maximum common mode voltage range	Available range before triggering over-voltage protection. AC and DC coupling modes[6]	0.4	0.7	1	V
Crosstalk isolation between channels[7]	F_{IN} = 0–4 GHz	–	–69	–	dBc
	F_{IN} = 0–7.125 GHz	–	–63	–	dBc

RF-ADC Electrical Characteristics for ZU6xDR Devices*

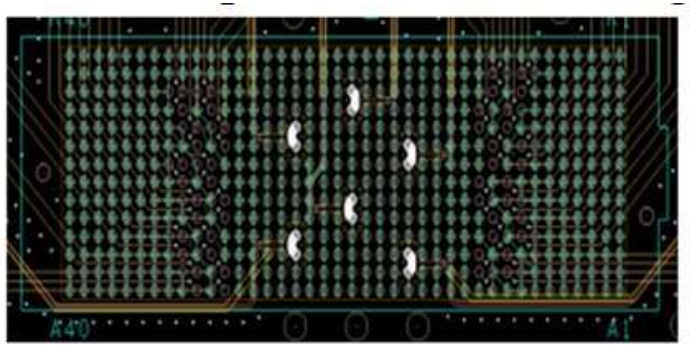
Analog bandwidth	Full power bandwidth (–3 dB)	–	7.125	–	GHz
Return loss (R_L)[5]	Up to 4 GHz	–	–12	–	dB
	Up to 7.125 GHz	–	–10	–	dB
On-die Termination	Single-ended on-die termination to external 3V V_{DAC_AVTT}		50		Ω
Crosstalk isolation between channels[6]	F_{OUT} = 0–4 GHz	–	–69	–	dBc
	F_{OUT} = 0–7.125 GHz	–	–63	–	dBc

RF-DAC Electrical Characteristics for ZU6xDR Devices*

Analog over Array Design Choices

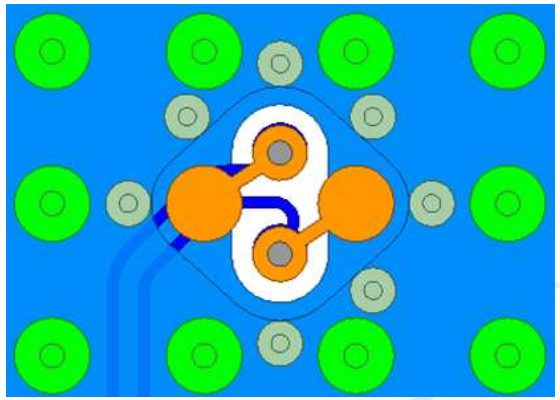


High-Isolation Pin Mapping

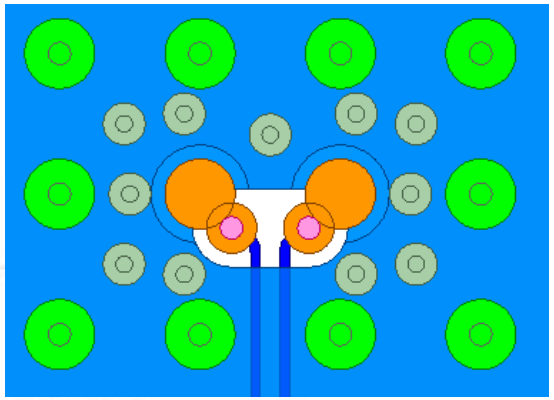


PCB Artwork

Rogers 3003 PCB Laminate

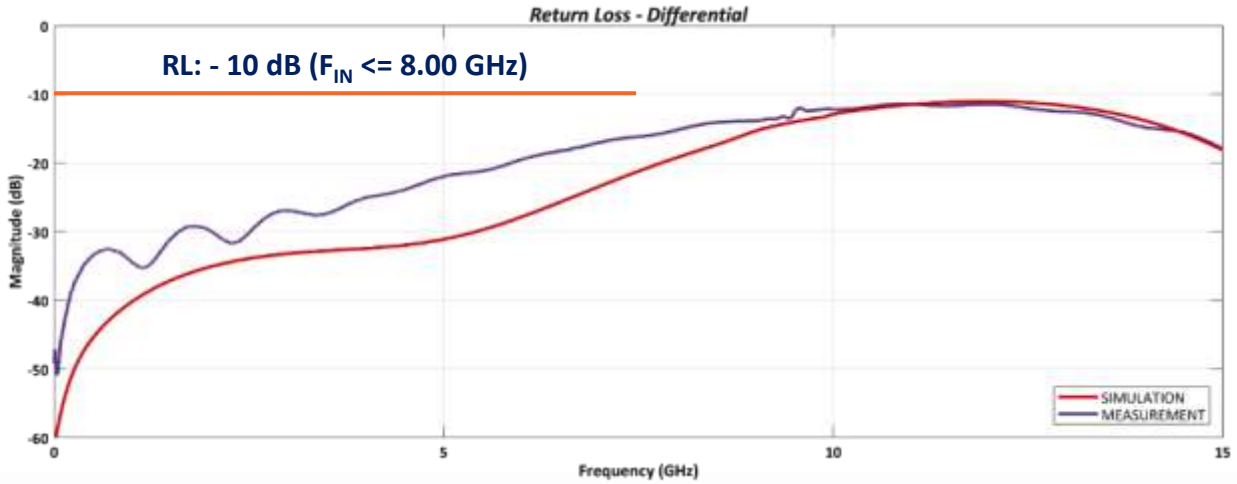


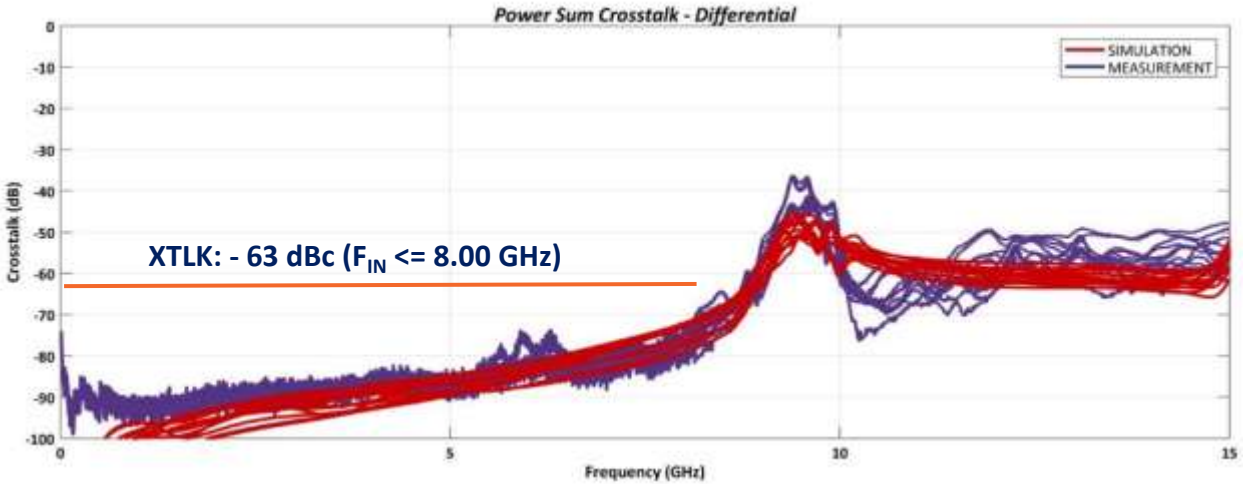
Typical DP Launch Optimization



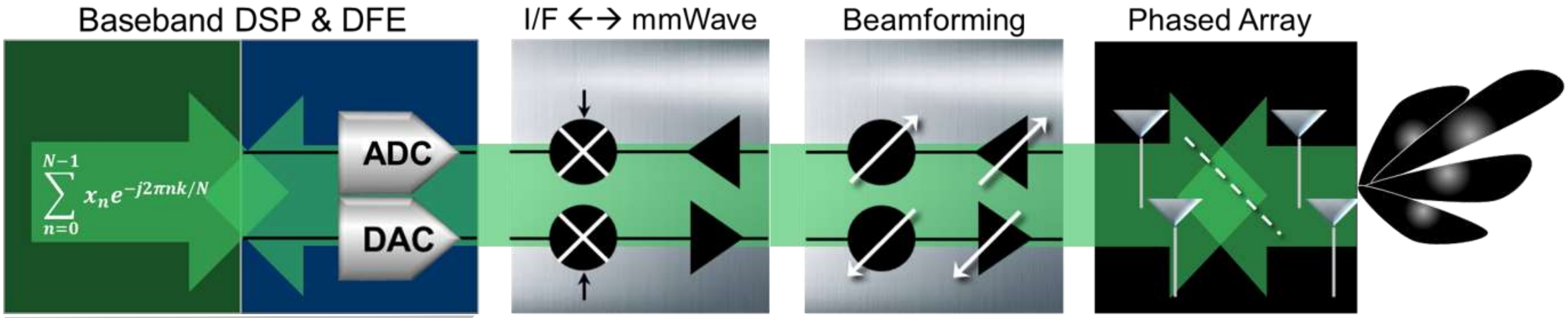
AoA Launch Optimization

Simulation and Measurement Results





Where's the High-Performance Interconnect?

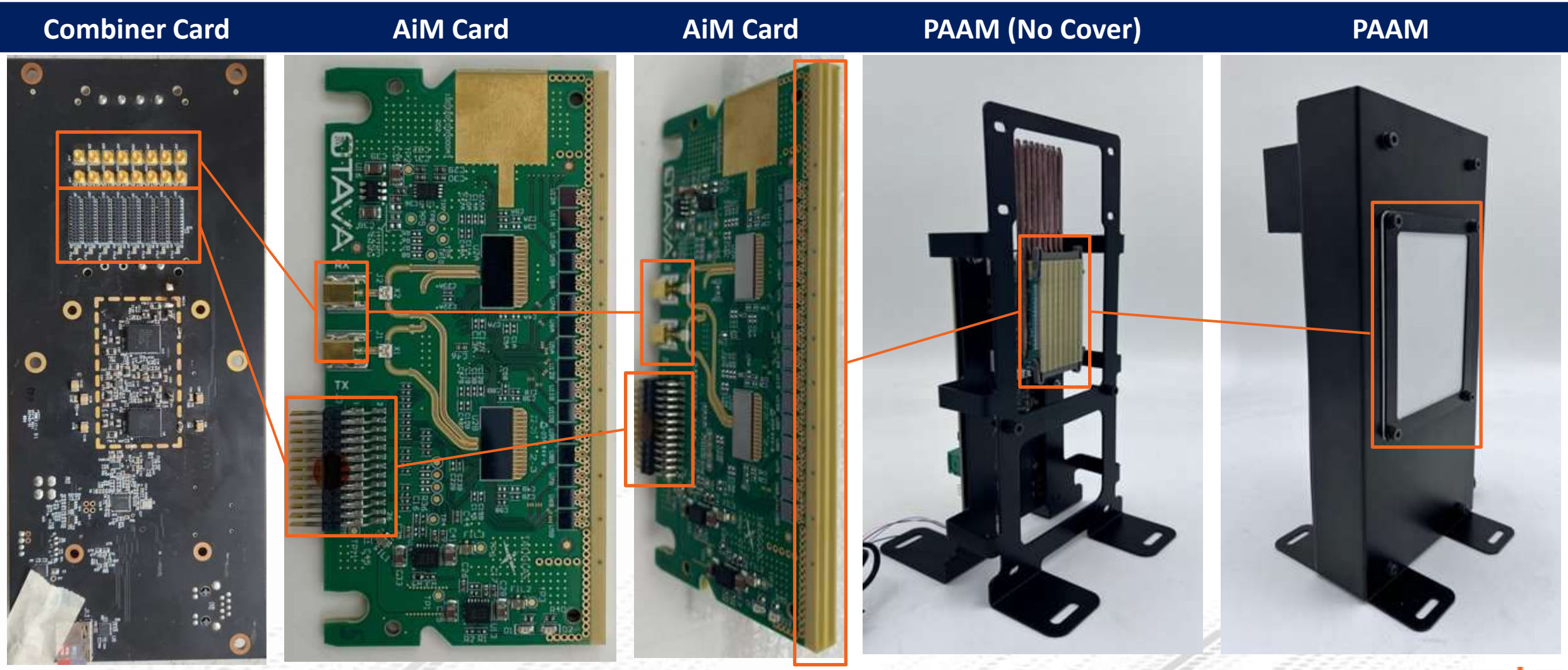


AMD Zynq UltraScale+ RFSoC
ZCU208 Evaluation Kit

Otava
DTRX2 mmWave
Radio Card

Otava
PAAM

Otava PAAM Interconnect Options



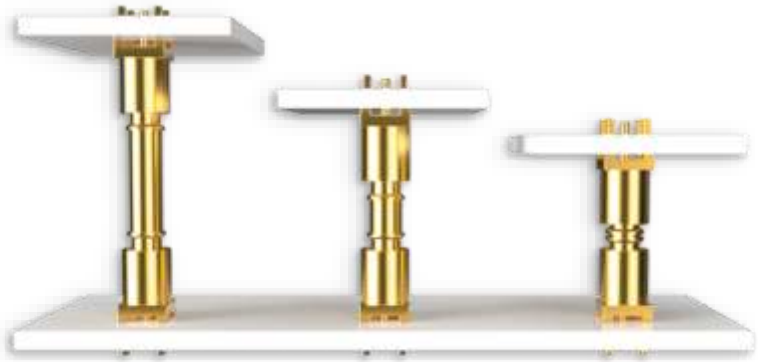
Samtec Confidential

65 GHz Precision RF Interconnect - SMPM/Magnum RF™

SMPM

- Miniature footprint; 30% smaller than SMP
- Push-on design for quick attach and easy mating
- Bullet adaptor for board-to-board blind mate applications
- Edge-Mount (SMPM-EM) – AiM Card
- Bullet Adaptor (PRFIA-SMPM)
- Through-Hole (SMPM-TH) – Combiner Card

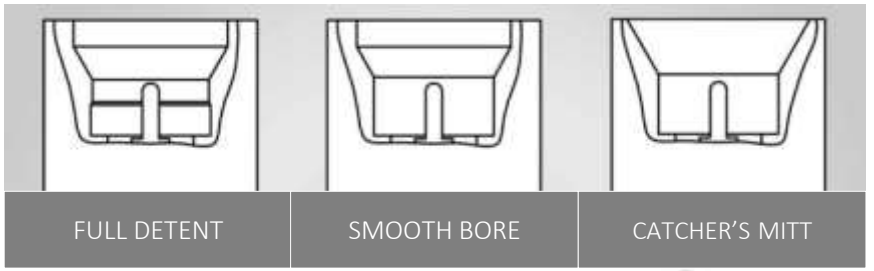
PRFIA-SMPM Options



SMPM Connectors with Bullets

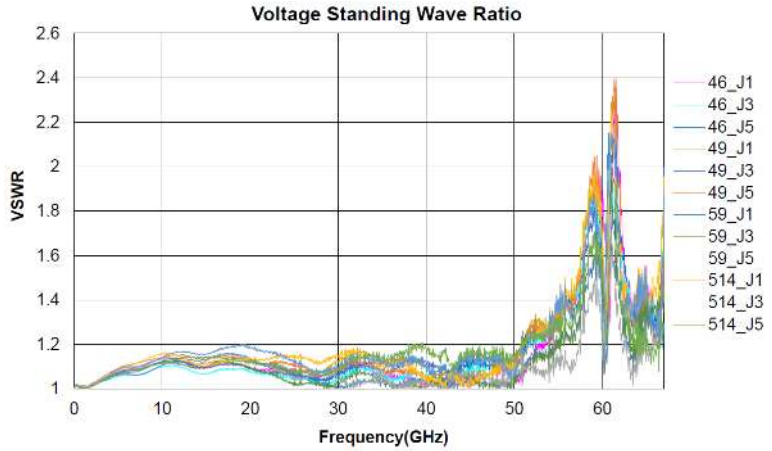
SMPM Interface

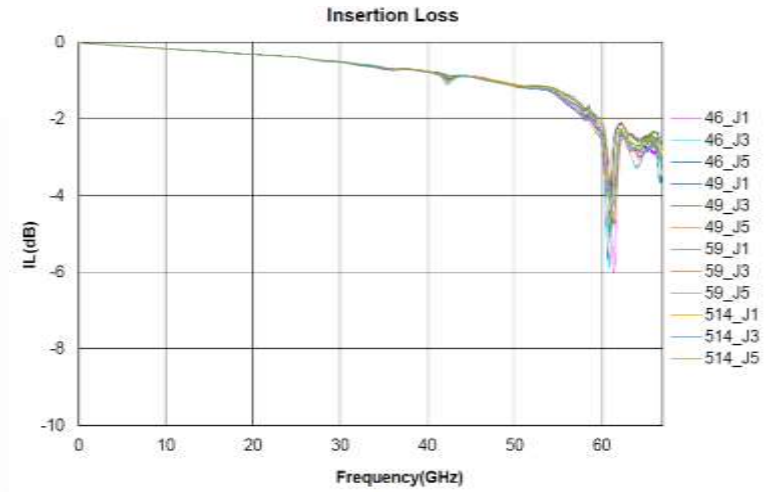
- Full detent, smooth bore or catcher's mitt
- Accommodates axial and radial misalignment when used with bullet adaptors



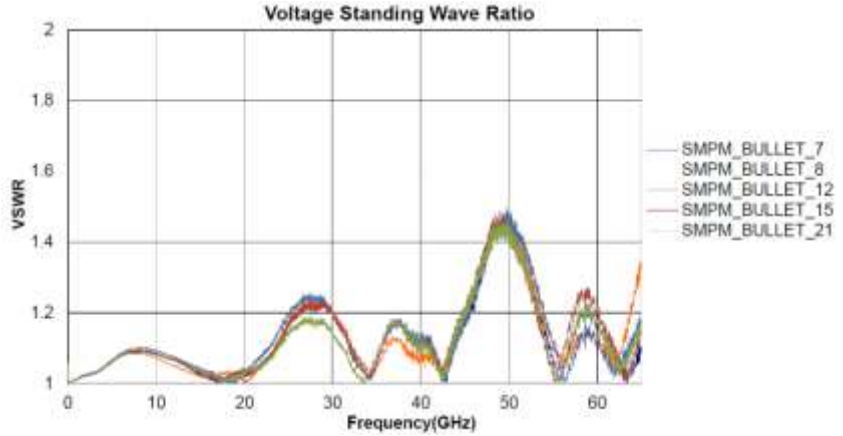
Samtec SMPM Interconnect Performance

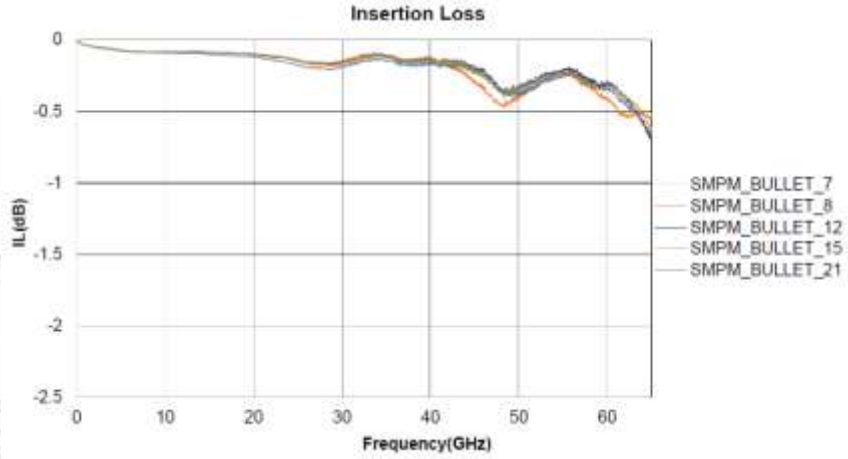
SMPM-SM Series



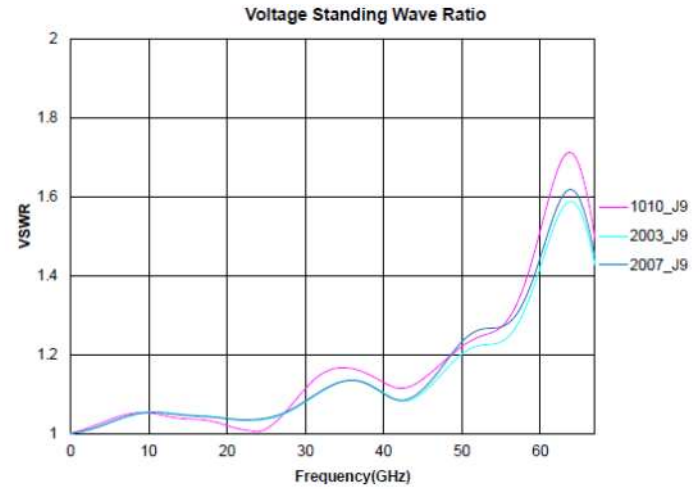


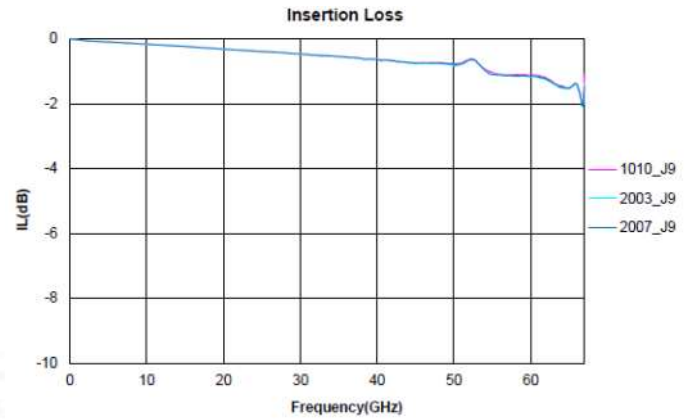
PRFIA Series





SMPM-EM Series

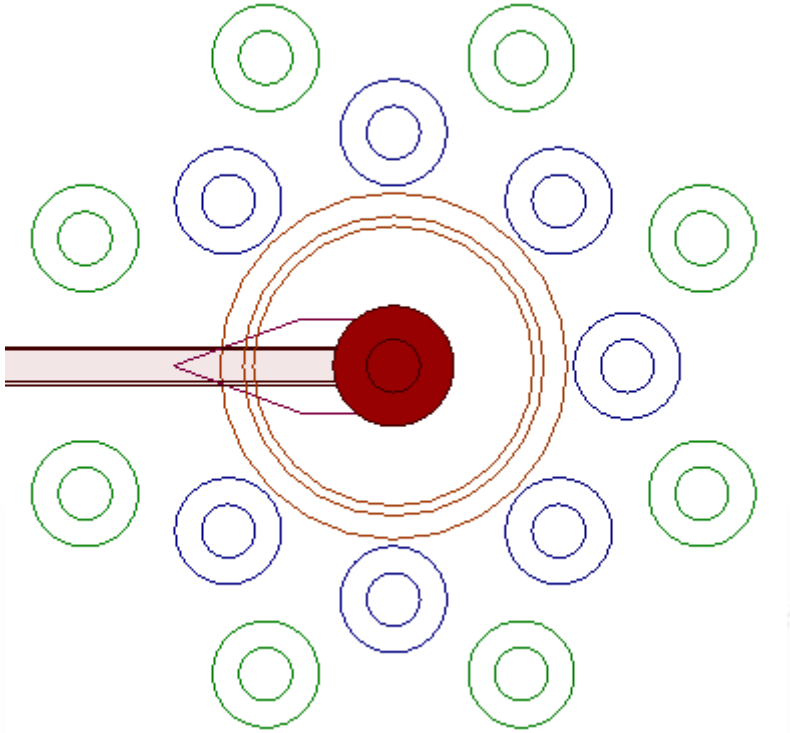




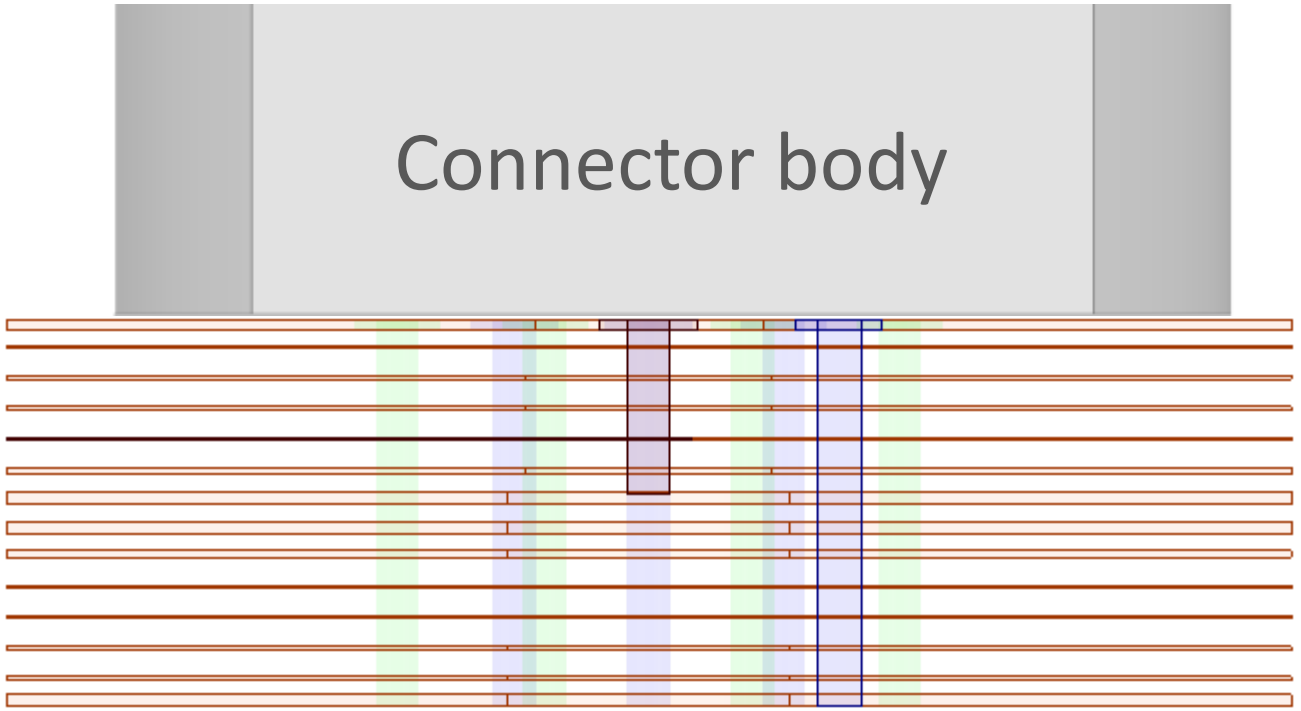
Samtec Confidential

PCB Connector Optimized Launch

Top View



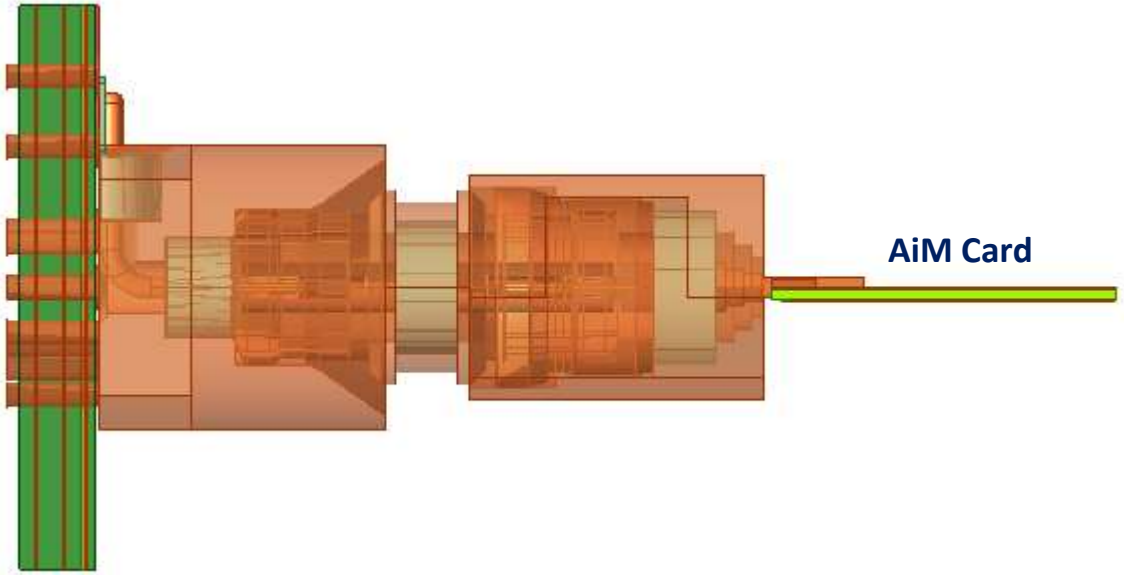
Side View

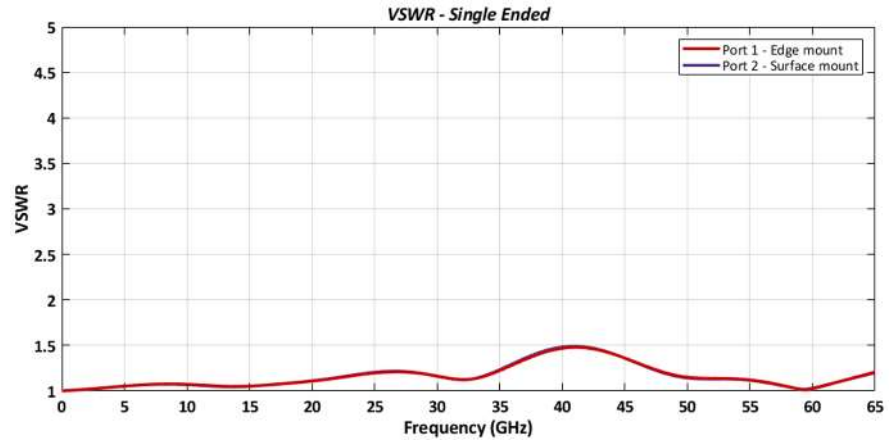


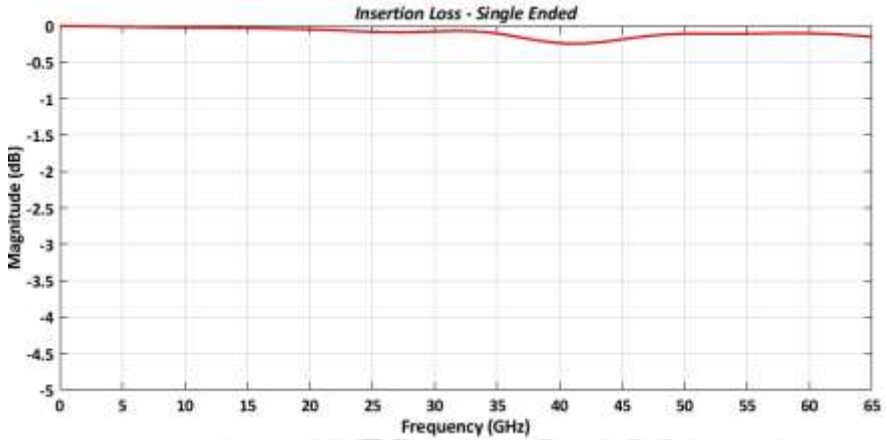
Otava AiM/Combiner Card Performance

Optimized Signal Channel Performance

Combiner Card







Signal Integrity and RF Design Experience

Launch optimization, design services

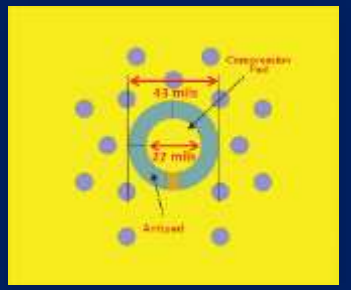
Simulations

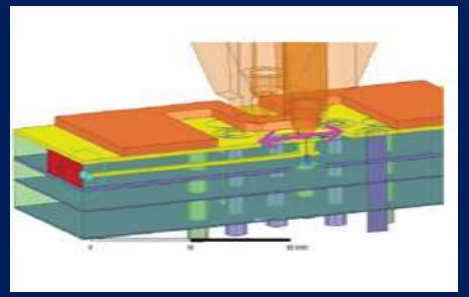
Physical test and measurement verification

Full channel analysis, system support

Specific design and development application assistance

Samtec's Signal Integrity Group (SIG) provides in-house signal integrity expertise for complex applications, with live EE support available 24/7 worldwide





Key Takeaways

Analog over Array technology optimizes the outing of analog/RF signals via the RFMC interface on the AMD ZCU208 + Otava DTRX2

Samtec's holistic design of RF signal channels optimizes performance in complex application like Otava PAAM

For more information:

- www.samtec.com

Our next speaker . . .

- Markus Lörner
- Market Segment Manager RF Components
- Rohde & Schwarz

Array Connectors for Mixed-Signal Multi-Channel RF SOCs up to 8GHz

Chris Koeble[1], Kiana Montes[2], Juan Aguirre, Jeane Love[3]
Samtec, New Albany, IN, USA
[1]Chris.Koeble@samtec.com, [2]Kiana.Montes@samtec.com, [3]Jeane.Love@samtec.com

Abstract — System on chip (SoC) implementations with integrated data converters and RF front-end subsystems are being deployed in 5G/6G, phased array radar, SATCOM, FPGA cards, and test and measurement architectures. This paper describes the research, development, simulation, and measurements performed in a project to design the optimal breakout region (BOR) for the use of array connectors that simultaneously carry analog, digital, and/or power signals in an RF environment, as a replacement for traditional compression mount and threaded PCB connectors for RF signals.

Keywords — MIMO communications, interconnect, satellite communications, connectors, analog, RFSoC, high solutions.

I. INTRODUCTION

Single-chip broadband systems on chip (SoC) products with integrated data converters and RF front-end subsystems are being deployed in 5G/6G, phased array radar, SATCOM, FPGA cards, and test and measurement instrument-to-bit architectures. The development of these RFSoC devices challenges the traditional approach of using compression mount and threaded PCB connectors and cable assemblies to handle the RF signals. A simple alternative, using multiple gauged connectors, will ease many on form factor, weight, and financial budget, especially as high-frequency RF channel count increases in these SoC-based systems.

One approach is to take existing technology that was originally designed for high-performance, high-speed digital signaling and adapt it: array connectors. These connectors make it possible to route high-frequency, high-isolation RF signals as well as digital and power signals through a single connector. While these connectors are already proven in high-speed digital systems, using them for RF applications required the development of specific PCB stack ups, and launch optimizations in order to achieve the differential crosstalk and return loss performance required for frequencies up to 8GHz and beyond. This paper describes the research, development, simulation, and measurements performed in a project to design the optimal breakout region (BOR) for the successful use of array connectors in an RF environment.

II. BACKGROUND

In pursuit of the latest applications, mixed-signal designers have taken FPGA technology to the next level, adding RF sampling data converter functionality on chip. Traditionally, RF design is a discrete approach, including, for instance, a baseband processor, ADC, DAC, and IF/RF signal chain devices. An RFSoC brings the ADC/DAC and some of the RF signal chain processing into the same package as the FPGA. Examples of these types of devices are the AMD Xilinx Zynq® and Intel® Agilex™ Direct RF-Series, with frequencies up to nearly 8GHz.

One of the fundamental differences of these new SoC designs is that instead of one or two coaxial cables into a processor, a single chip is now supporting dozens of RF signal chains. This enables new technologies such as 5G MIMO, which also requires beamforming, as well as phased array systems, with a typical phased array having 64 to 128 antenna paths with discrete antennas.

Each of these antennas needs a signal path, which could include an RF attenuator, a switching function (which determines Tx or Rx), up/down converters, IF circuitry, beamforming, etc. Traditionally, designs use simple compression RF connectors which offer excellent performance but do not scale well. They take up valuable PCB space, add cost, and are prone to misalignment in an array form factor. A solution for some simpler designs is gauged RF connectors, offering, for example, a 1x8 or 1x9 configuration. While this is proving to be a very good solution in many applications, it is still too bulky to support RFSoC designs. For instance, a 5G MIMO or phased radar array design could require dozens or hundreds of RF connectors. As a result, the industry requires smaller, denser, high-frequency connectors. Ideally these connectors handle RF, digital, and power simultaneously, linking the motherboard to daughter cards and beyond.

Fortunately, the latest RFSoCs can handle differential RF signals, so this paper will focus on a connector BOR design using differential RF signals. (Single-ended signals were also part of the overall project, and they are mentioned in the future work section.) The industry is moving towards differential RF signaling to achieve the necessary noise performance at higher frequencies. Since differential signals are out of phase with each other, they have a natural noise rejection that single-ended designs do not have, essentially canceling each other's unwanted EM fields [1].

As compared to single compression-mount RF SMA connectors or gauged ones, an array connector offers a better solution in terms of performance, cost, and real estate for designs using RFSoCs, as long as its pinouts and BOR are optimized for use with RF signals. To date, our work on this array project has supported 4GHz, 6GHz, and now 8GHz mixed-signal FPGA designs. In addition, designers using these

International Microwave Symposium

11-16 June 2023, San Diego, CA

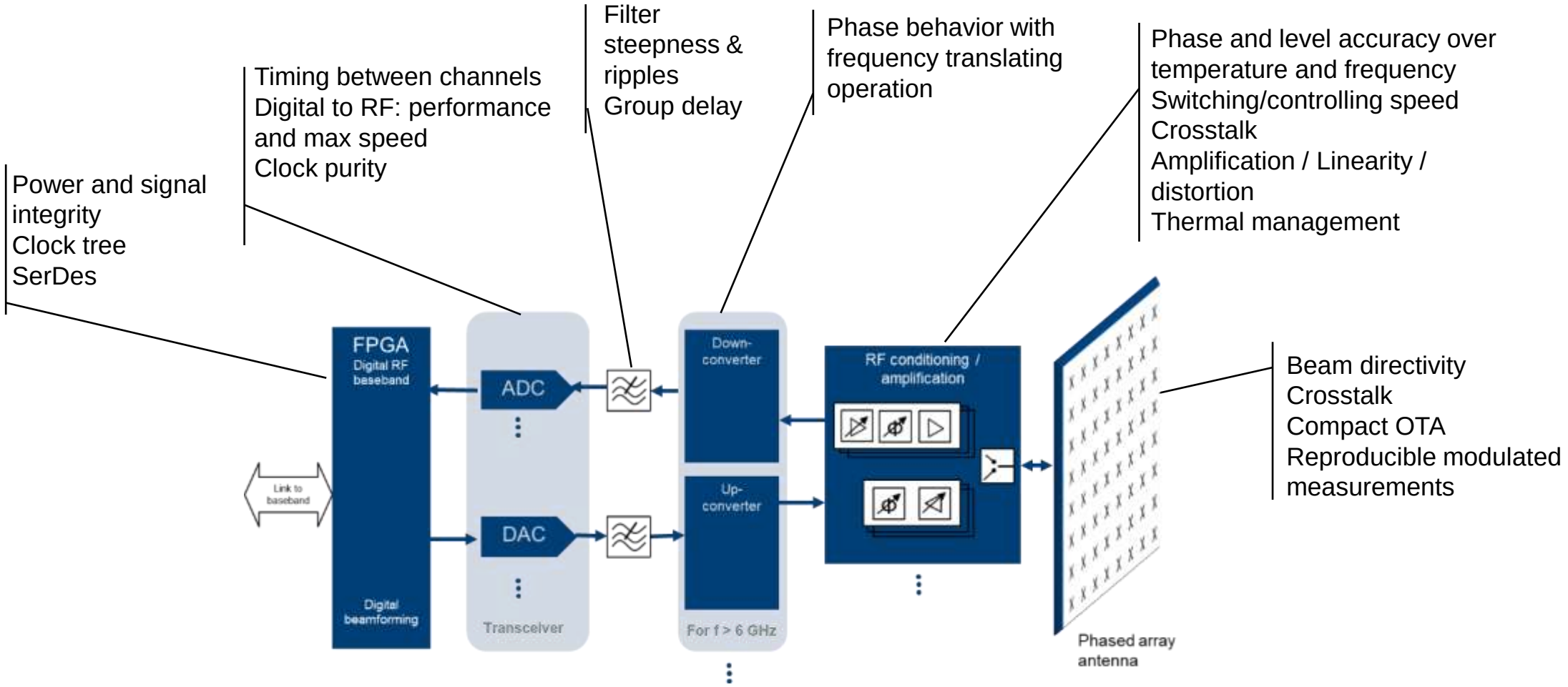
TAMING SIGNAL INTEGRITY CHALLENGES IN MMWAVE ANTENNA-TO-BITS IMPLEMENTATIONS

Markus Lörner, Market Segment Manager RF Components

ROHDE&SCHWARZ

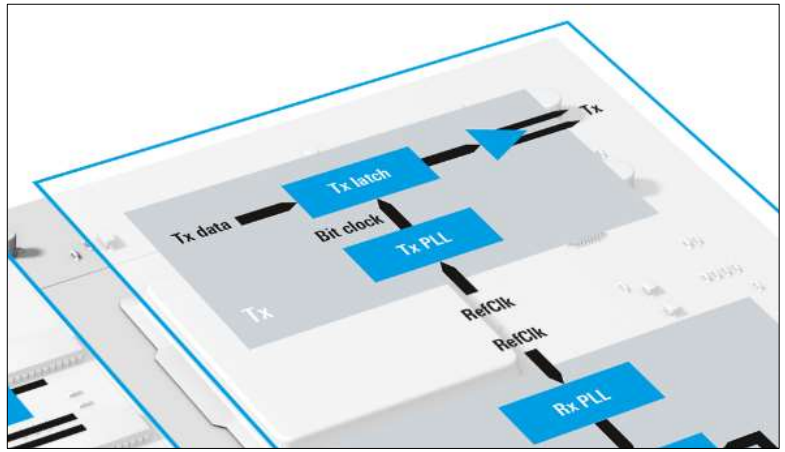
Make ideas real

DESIGN PAIN POINTS



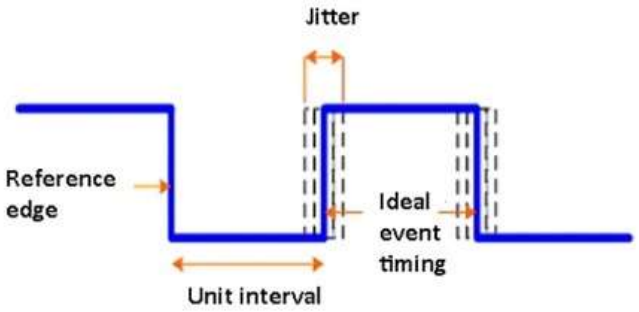
DIGITAL INTERFACE TEST

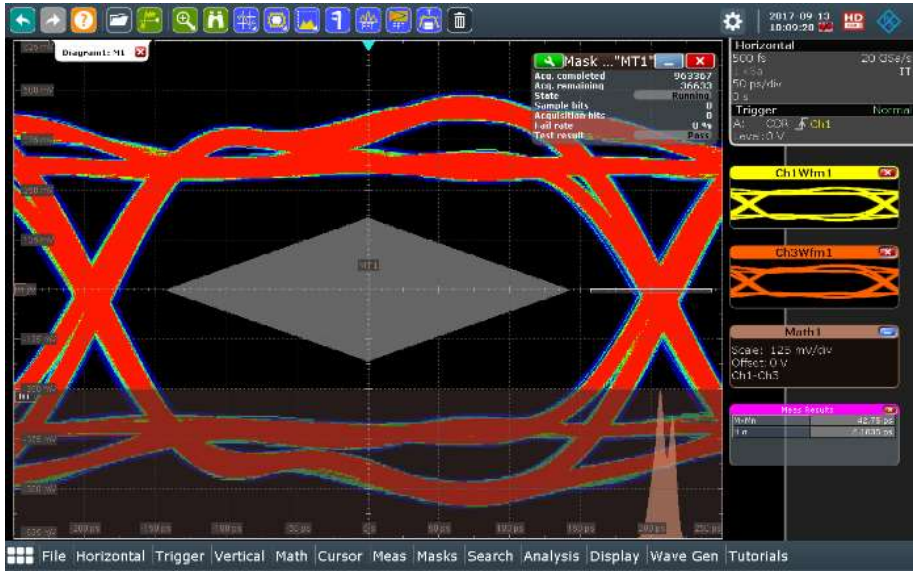
Building Blocks



Typical Design Challenges

- Jitter: e.g. Time Interval Error (TIE)
  - track graph
  - histogram
  - spectrum
- Eye diagram and mask test (Compliance)
- Rise / fall time, timing measurements, …





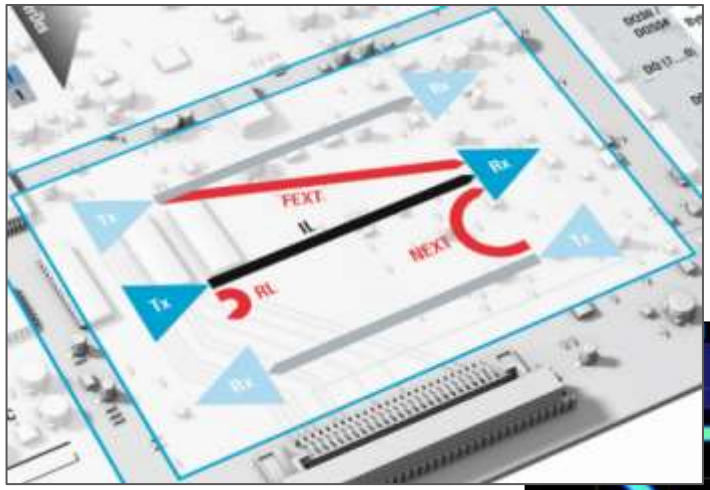
R&S®RTP

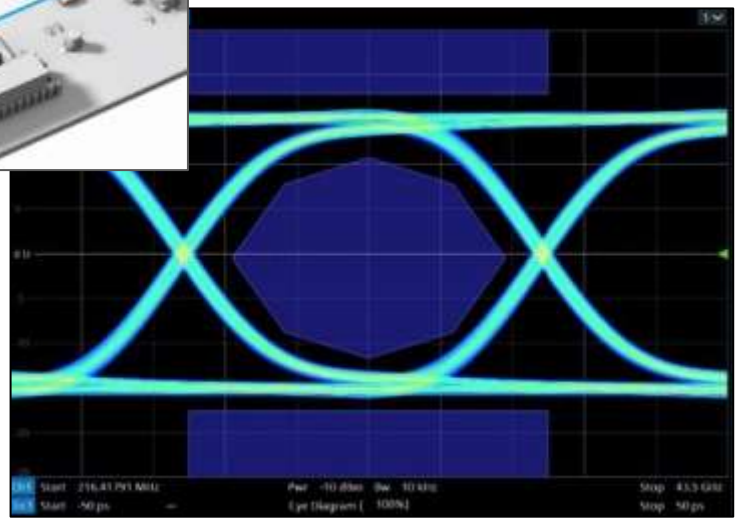
VNA AND SIGNAL INTEGRITY TESTING

Q : When do I need a VNA?

A : When you have to measure:

- PCBs
- Cables
- Connectors





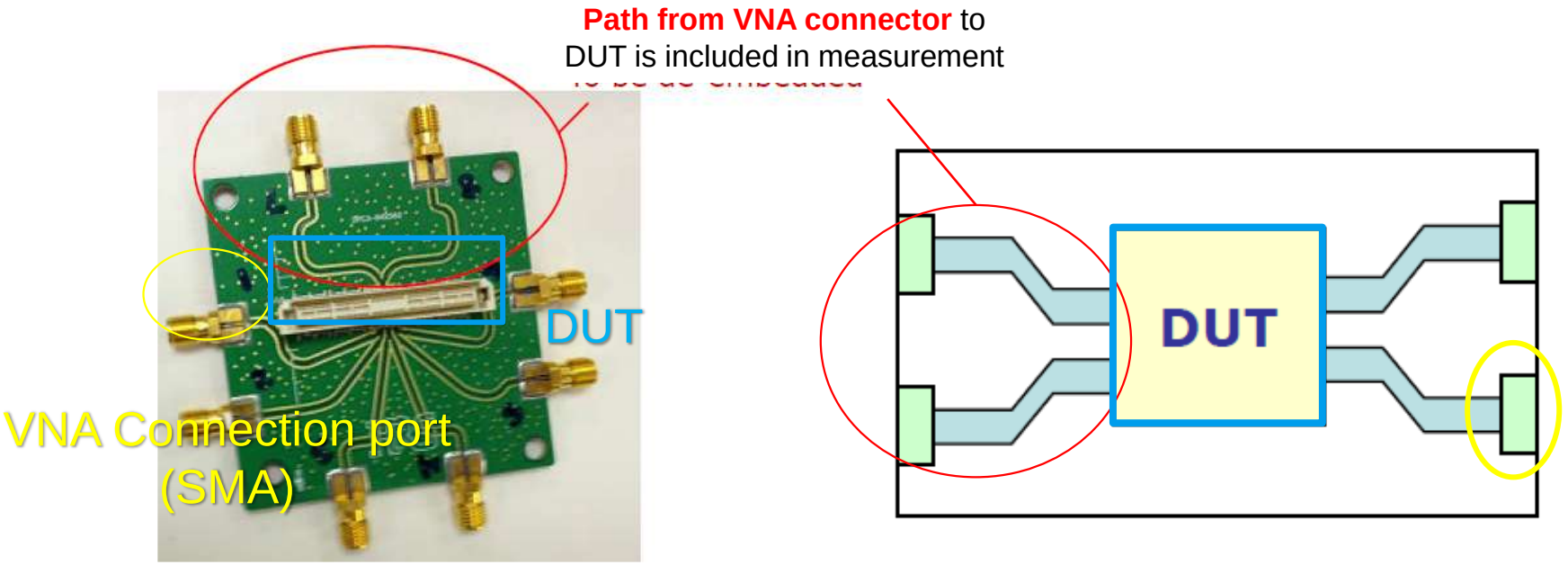
Q : What can I measure?

A : Parameters such as:

- Insertion/Return loss
- Impedance
- Crosstalk
- Eye diagram-related measurements (skew, rise-time, etc.)

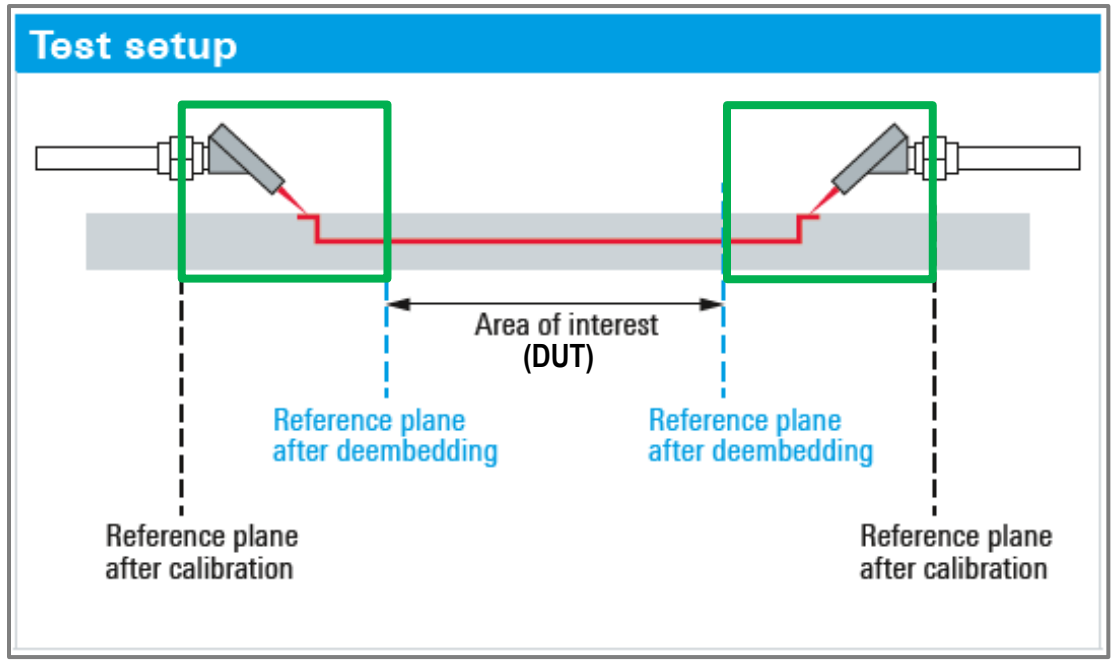
THE CALIBRATION ISSUE

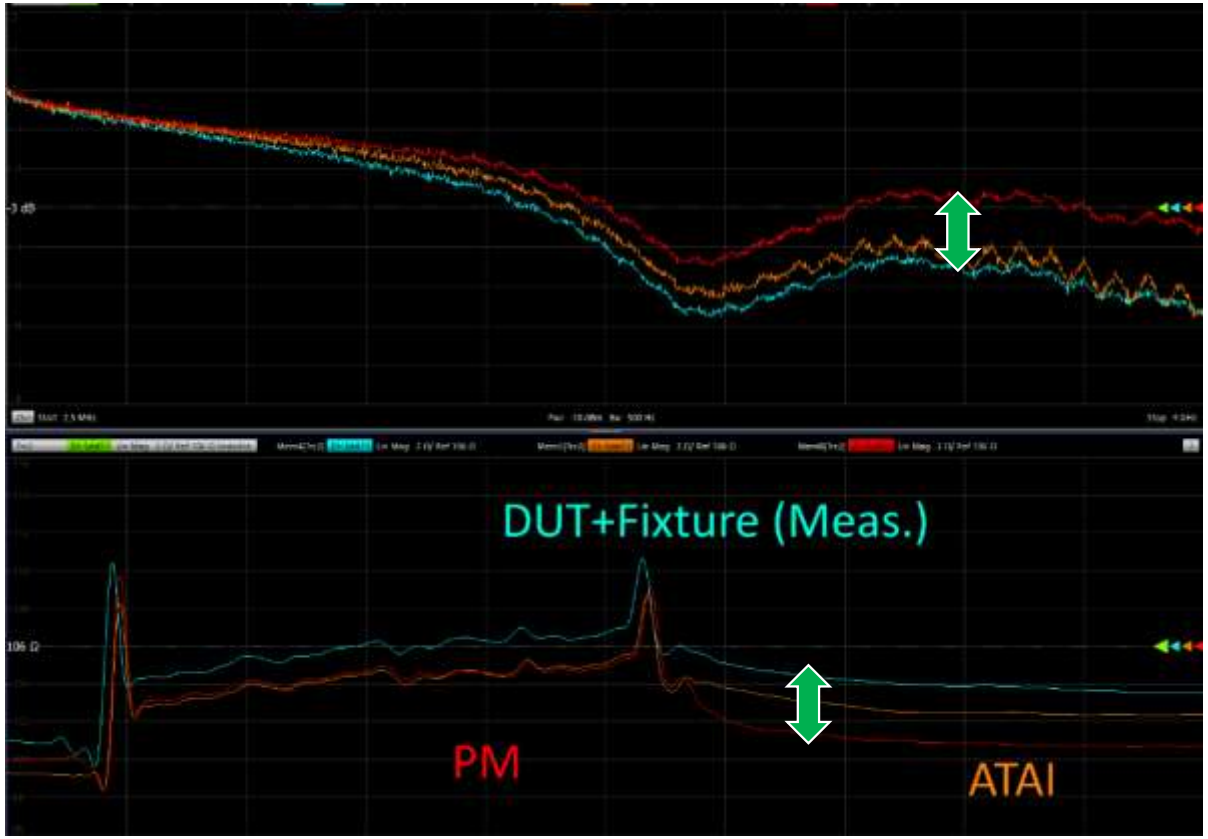
- VNA precise measurements → calibration
- Even if you calibrate and have a coaxial interface…



…a **fixture** could become “a DUT part”,
which has to be removed **(de-embedded)** from the measurement

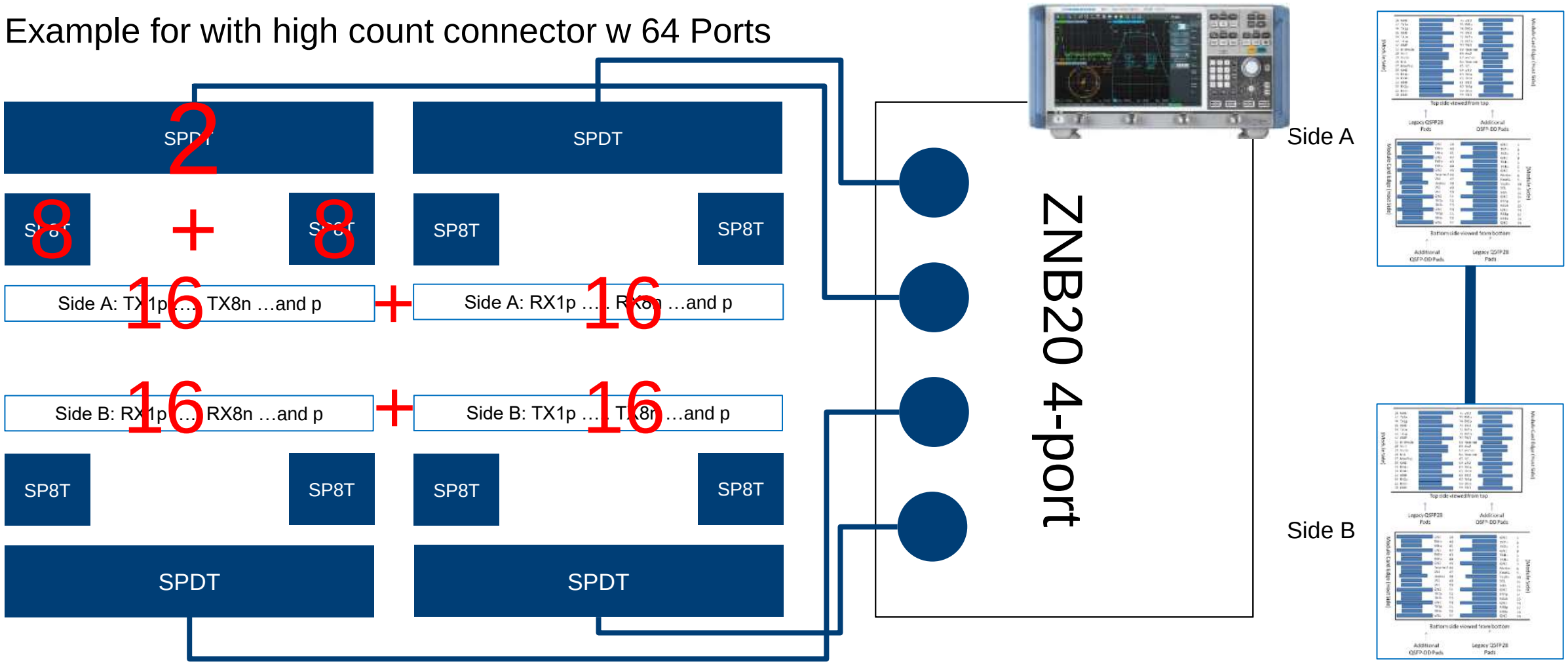
THE IMPORTANCE OF DE-EMBEDDING





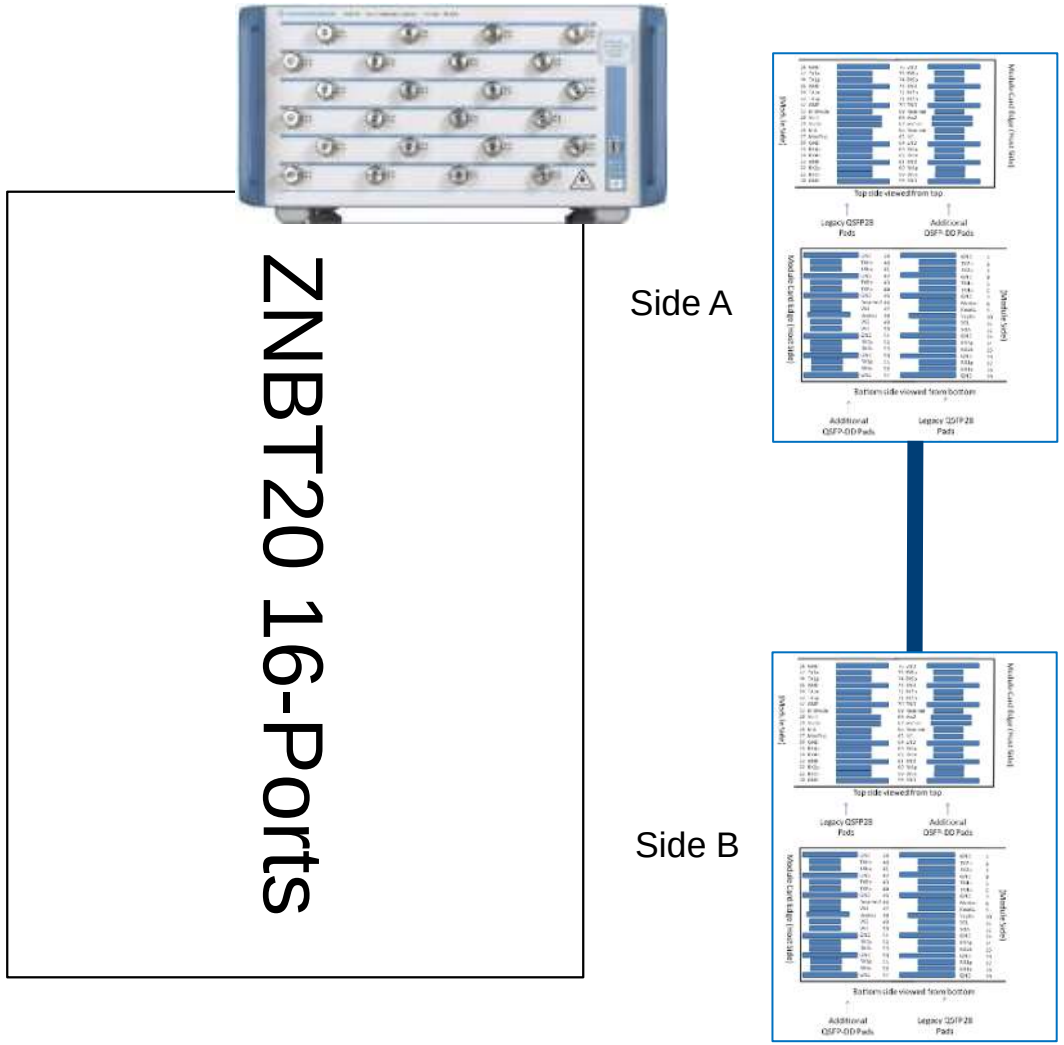
CHEAT-SHEET – THE POWER OF MULTI-PORT

Example for with high count connector w 64 Ports



CHEAT-SHEET – THE POWER OF MULTI-PORT

Example for with high count connector w 64 Ports



MODULATION PERFORMANCE TEST

Goals
- Check compliance with design targets
- Optimize design
- Shorten design cycle

Test considerations
- No compromises
- Maximum flexibility
- Right tools
- Speed

Excellent performance out of the box for modulated tests during R&D and design validation

Selected instruments for modulated measurements

R&S®SMW200A

- Single & dual RF up to 2x 44 GHz / 1x 67 GHz
- 2/4 GHz RF BW
- DPD, ET, Doherty suites

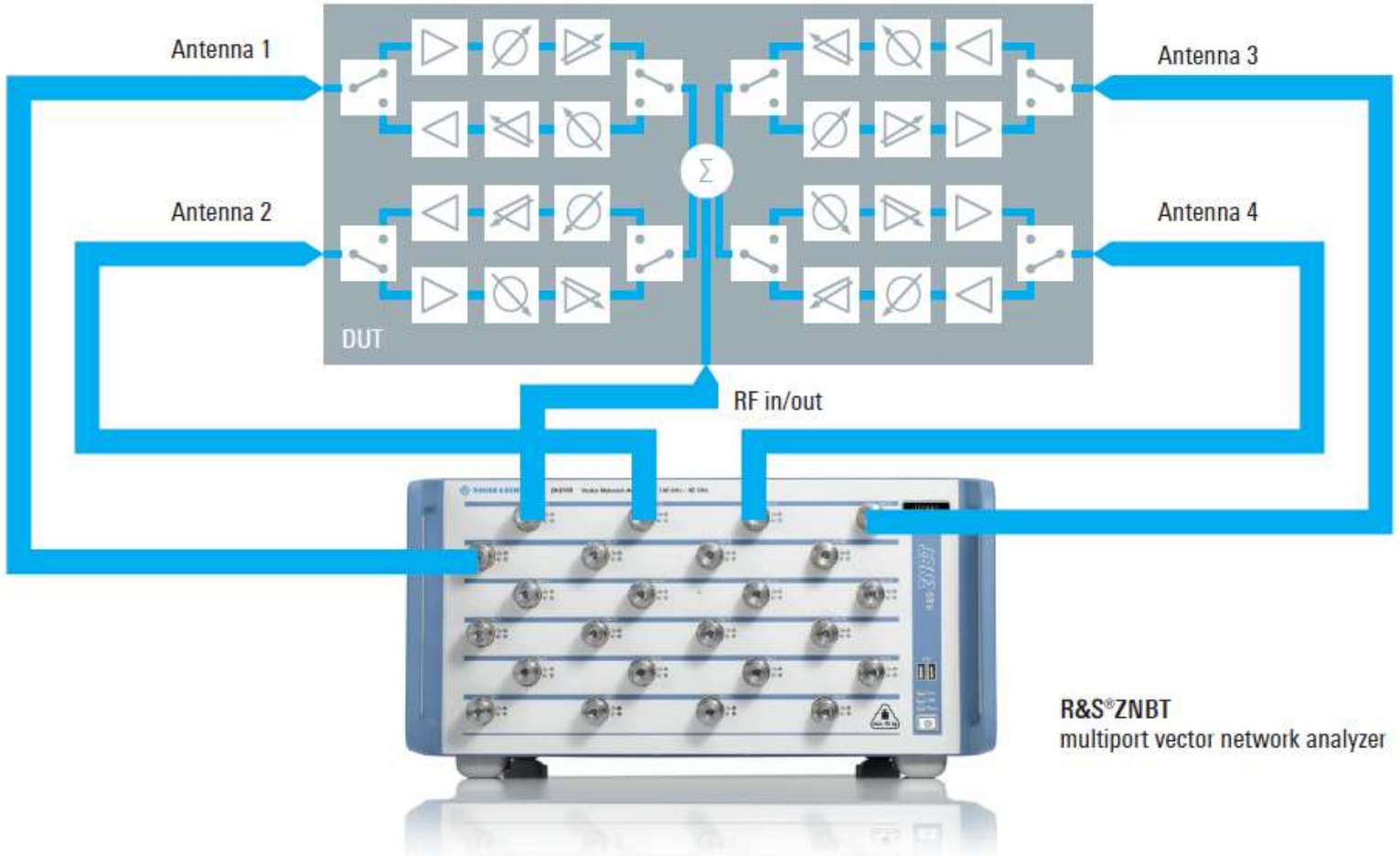
R&S®FSW

- Up to 85 (90) GHz
- 8 GHz internal analysis BW
- 60 dBc SF dynamic range
- PA measurement suites

R&S®NGP800

- 4 channels, 800 W total
- Up to 32V/20A or 64V/10A per channel
- DUT protection

BEAMFORMER VERIFICATION: MULTIPORT SOLUTIONS



R&S®ZNBT
multiport vector network analyzer

R&S®ZNA

Accuracy and dynamic range

Test speed and simultaneous measurements

ANTENNA MEASUREMENTS USING CONTINUOUS WAVE OR MODULATED SIGNALS

Measuring with Continous Wave

- Done during early stages of R&D
- Useful as fast check of parameters
- System components: OTA chamber, ZNA, AMS32
- Measurements: directivity, gain, realized gain, efficiency, beamwidth, EIRP, TRP, 2D/3D patterns, phase measurements

Measuring with Modulated Signals

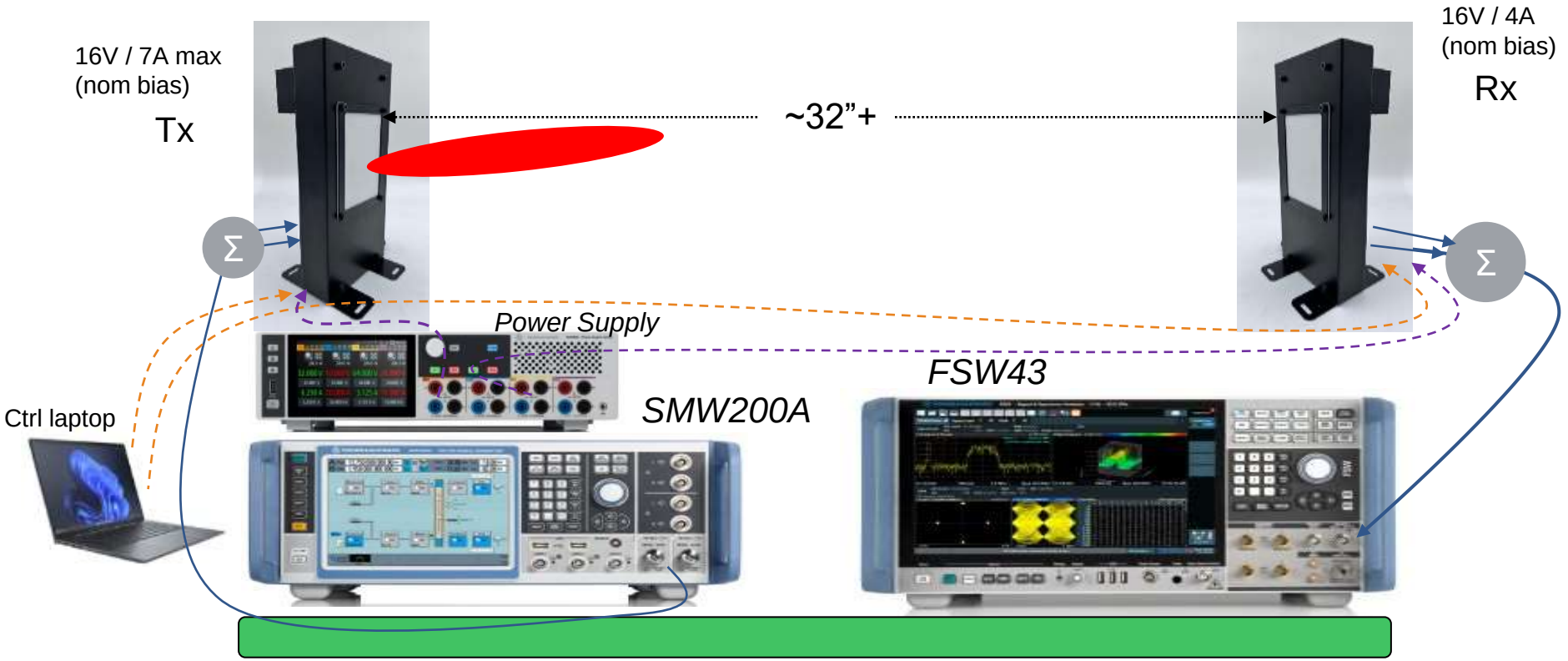
- Done during advanced stages of development, especially useful for debugging devices
- Improves final type approval rate
- System components: OTA chamber, FSW, SMW, AMS32
- Measurements: EVM, ACLR, SEM, directivity, gain, realized gain, efficiency, beamwidth, EIRP, TRP, channel power, 2D/3D beamforming patterns

OTA SOLUTION OVERVIEW FOR FR2 AND ALIKE

	ATS1000	ATS800B	ATS800R	ATS1800C
Dim. (WxDxH)	1 x 1.5 x 2.1	1.2 x 0.6 x 0.8	0.8 x 1 x 2.1	0.9 x 1.5 x 2
Application	R&D, antenna measurements	Benchtop R&D, academia, research institutes	R&D, pre-conformance (RF, LBS, Netop, PCT, PQA)	R&D, Conformance & pre-conformance (RF, LBS, Netop, PCT, PQA)
Type	White box DFF/NF	Black box CATR	Black box CATR	Black box CATR
Freq. Range	18 - 87 GHz	18 - 50 GHz	18 - 50 GHz	(6) 18 - 90 GHz
Supported freq. Range	Full range	Full range	Full range	23 - 44 GHz (Feed antenna)
Quiet zone	Ø 4 cm @ 40GHz	Ø 20 cm	Ø 20 cm	Ø 30 cm
Positioner	3D conical cut	2D positioner (opt.)	3D Az over El (opt.)	3D Az over El
Shielding Eff.	>50 dB	-	>40 dB	100 dB
Extreme Temp.	3D	-	1D	3D

“If you want to go fast, go alone.
If you want to go far, go together!”
African proverb

PAAM Demo – Samtec Booth #2627



AVNET
Booth #2514

samtec
Booth #2627

OTAVA
Booth #2514

MathWorks
Booth #2541

Booth #735

Balancing Tradeoffs

Taming Signal Integrity Challenges in Millimeter Wave Antenna-to-Bits Implementations

Questions?

samtec

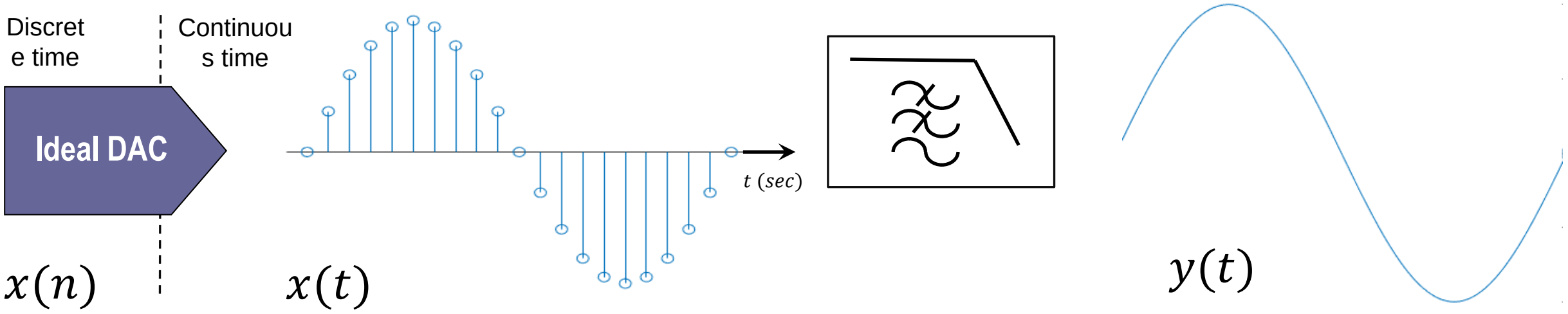
MathWorks®

AVNET®

OTAVA

Appendix

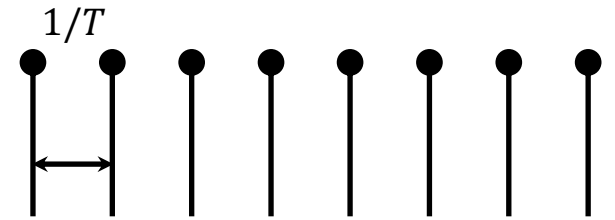
Fundamental DAC DSP Theory (Time Domain)



$$x(t) = y(t) \cdot \sum_{k=-\infty}^{+\infty} \delta\,(t - kT)$$

Fourier Series

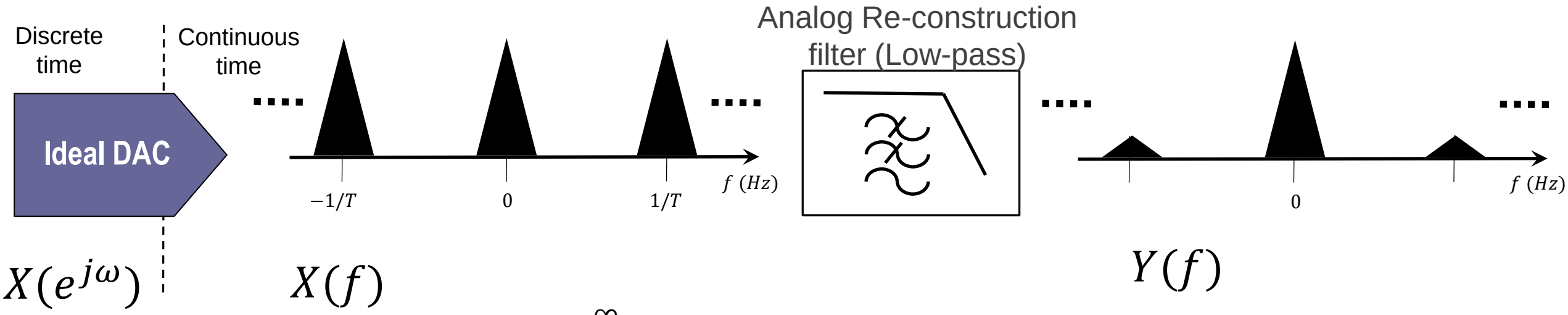
$$= y(t) \cdot {}^{1}/_{T} \sum_{k=-\infty}^{+\infty} e^{{}^{j2\pi kt}/_{T}}$$



$\text{Ш}_T(t)$ Dirac comb function

AVNET

DAC DSP Theory (Frequency Domain)



$$= {}^{1}/_{T} \cdot \sum_{k=-\infty}^{\infty} \int y(t) \cdot e^{{}^{j2\pi kt}/_{T}} \cdot e^{-j2\pi ft}\, dt$$

→ Fourier transform

$$= {}^{1}/_{T} \cdot \sum_{k=-\infty}^{\infty} \int y(t) \cdot e^{-j2\pi t(f - k/T)} dt$$

$$X(f) = 1/T \cdot \sum_{k=-\infty}^{\infty} Y(f - k/T)$$

Repeating Spectral Replicas at sampling frequency $1/T$ (Hz)

AVNET