KYOCERA AVX

ACCELERATING INNOVATION

Reducing Board Space and Improving RF Performance by Embedding MOS Capacitors

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Embeddable MOS Capacitors

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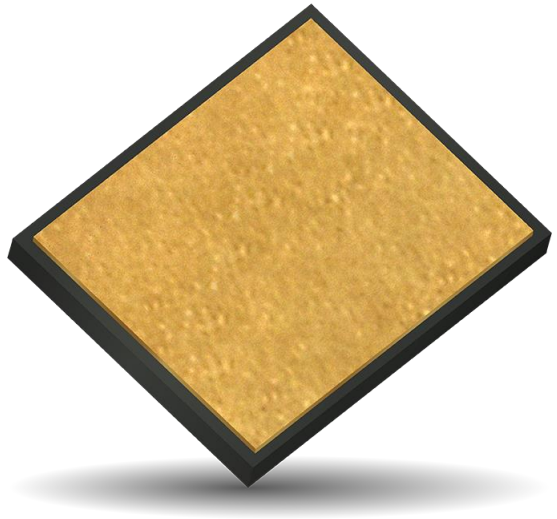

Embeddable MOS Capacitors

Introduction – About Me

- **Cory Nelson**
- **Principal Design Engineer**
  - Thin Film Components
  - Multi-Layer Organic (MLO) Products
- **KYOCERA AVX for 7 years**
  - Previously at Collins Aerospace and Honeywell
- **Masters of Science from Iowa State University**
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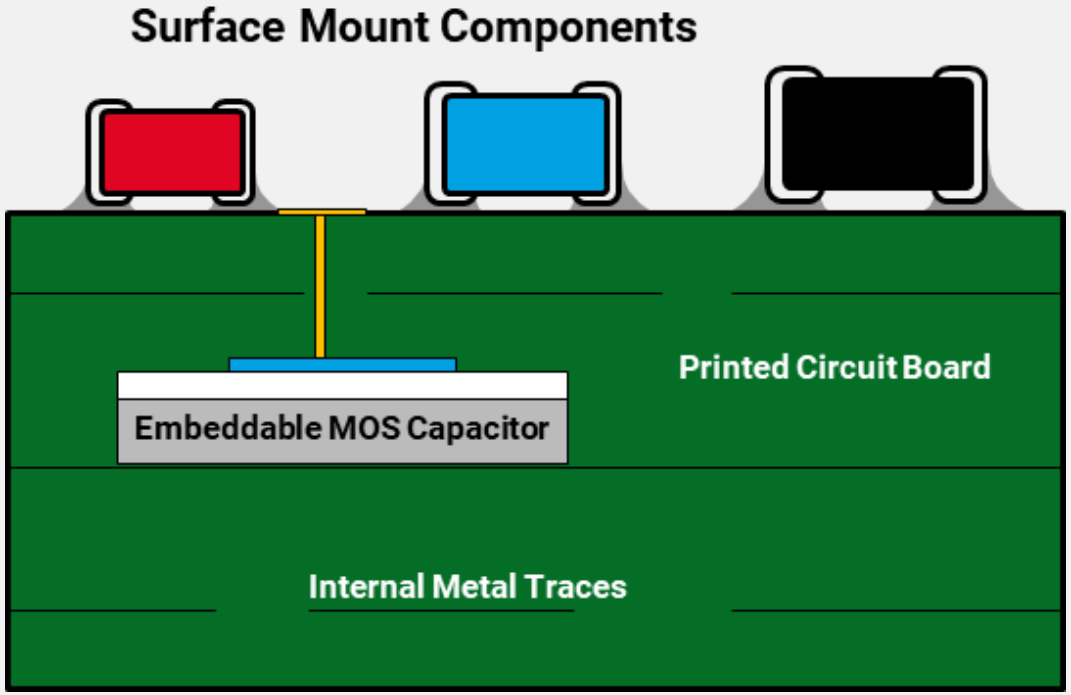
Embeddable MOS Capacitors

Introduction

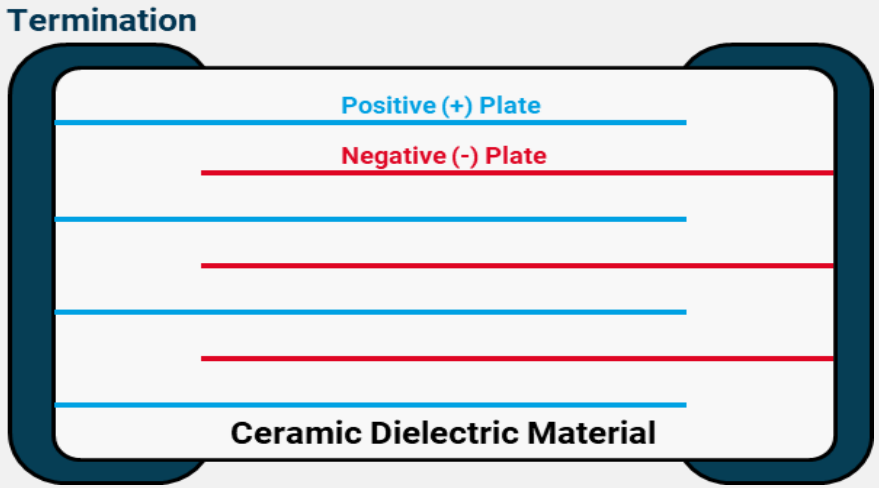
- Embedding circuits into the printed circuit board saves space
- Certain components are better suited for embedding
- RF performance can be improved through proper embedding



Embeddable MOS Capacitors

Capacitor Background - MLCC

- **Multi-Layer Ceramic Capacitor (MLCC)**
  - Stacks multiple plates to increase capacitance range
  - Surface mount components
  - Small sizes down beyond 01005
- $C = \frac{\varepsilon_r * A}{d} * (N - 1)$
- **Embeddable Limitations**
  - Chip thickness based on capacitance and number of layers required
    - 01005 size components could be embedded with 5mil thickness
  - Termination limits connections
    - Would prefer to be uniform and copper for embedding
    - Can't place on a ground plane without rotating

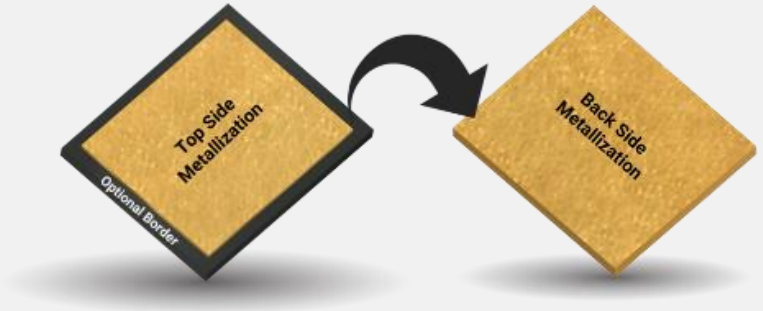


Cross section of a traditional surface mount capacitor with multiple plates with 1 terminal shown with blue plates and the other with red plates

Embeddable MOS Capacitors

Capacitor Background – SLC

- **Single Layer Capacitor (SLC)**
  - Two plate design
    - Allows backside to be on ground plane
  - Ceramic material changed to change capacitance value
  - Can get high capacitance values in small package
  - Offers ultra-thin thicknesses
- **Embeddable Limitations**
  - Capacitance dependent on thickness/material
  - Materials vary in temperature stability
  - Materials vary in structural match with PCB

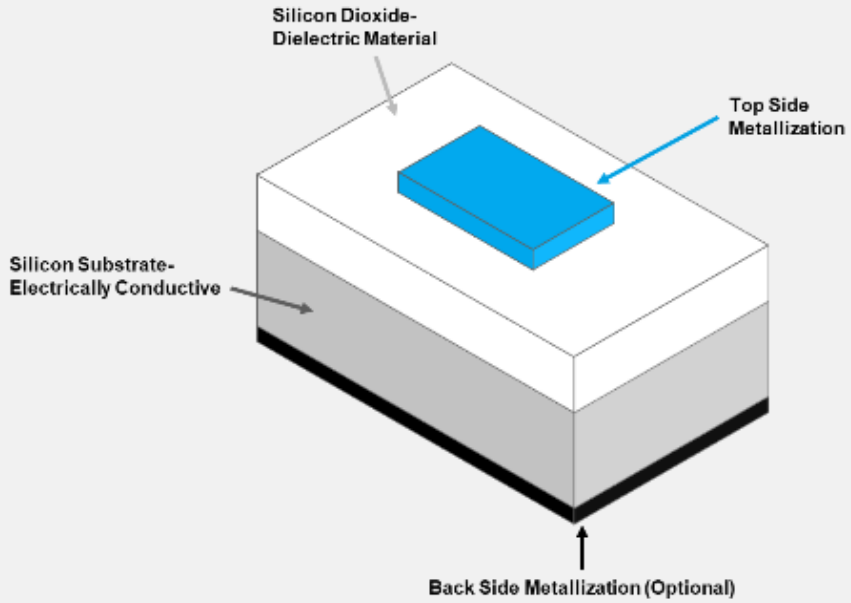


Top Cross section of a single layer capacitor the top metallization is represented with a blue line and the backside metallization is represented with a red line. **Bottom** Render of SLC frontside (with border) and backside

Embeddable MOS Capacitors

Capacitor Background – MOS Capacitor

- **Metal Oxide Silicon (MOS) Capacitor**
  - Two plate design
    - Subset of the SLC capacitors
  - Silicon substrate
    - Improves temperature performance and board match
    - Ultra-thin design below 5 mil
  - Oxide layer for dielectric
    - Can vary thickness without affecting chip thickness
  - Ideal for copper termination plating
- **Embeddable Limitations**
  - Cap values limited vs same size SLC



Cross section of metal oxide silicon capacitor with blue line for top side metallization and black line for backside metallization

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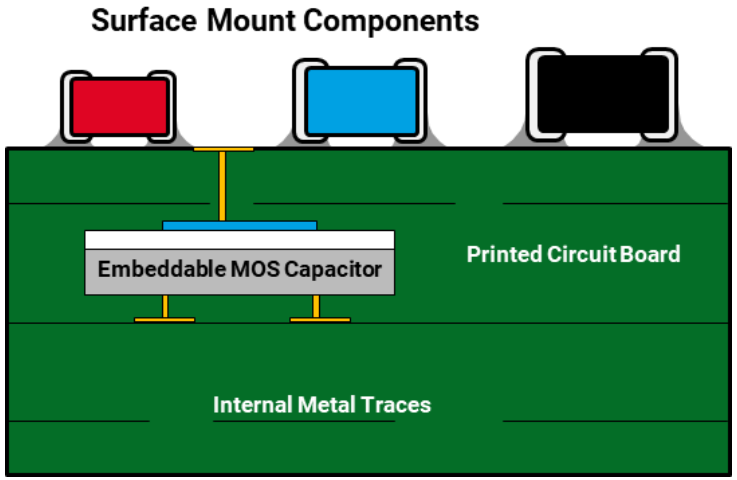
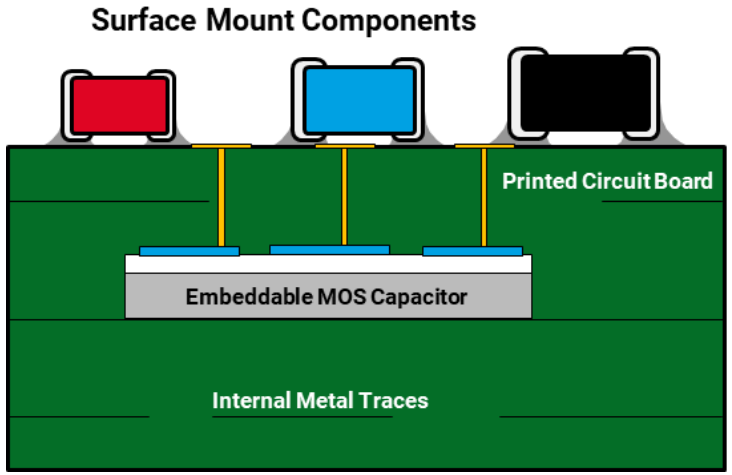
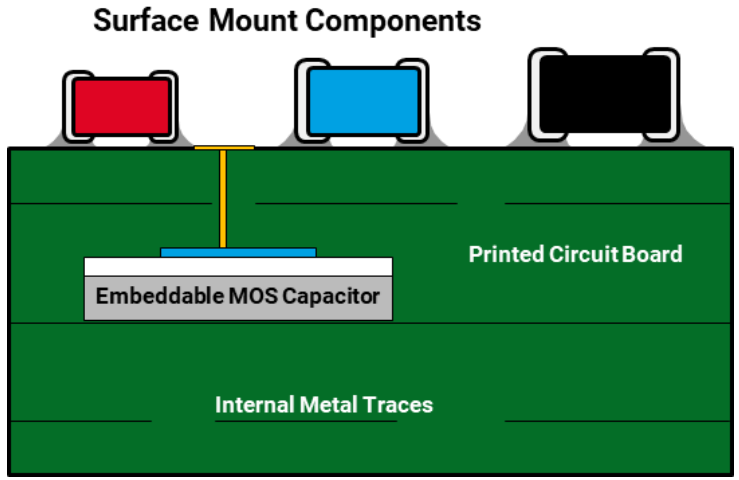
Embeddable Connection Options



Connection vias from top side and backside of board to connect to internal traces and mounted components



Multiple vias connecting the top side of board with components. Either through the single capacitor to ground or MOS cap array.



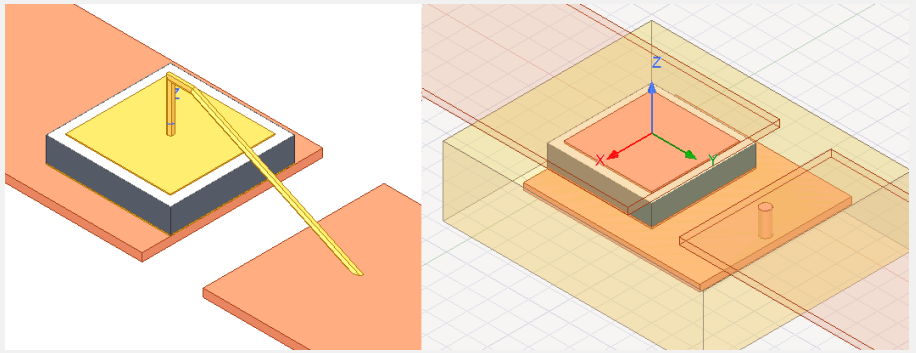
Chip mounted on internal (or external) ground plane with vias connecting top side to traces or components.

Embeddable MOS Capacitor

Modeled Performance

– Wirebond vs Embedded

- **Modeled performance in Ansys HFSS**
- **Wirebond model**
  - MOS Capacitor with wirebond connection bridging gap between transmission lines
- **Embedded model**
  - MOS Capacitor with via from transmission line to capacitor
  - Internal trace beyond the capacitor size connecting backside
  - Via from internal trace to top side transmission line
  - Epoxy used for the material where the embedding happened
- **Transmission lines and board remained same other than noted changes**
  - Rogers 4350, 50 ohm lines

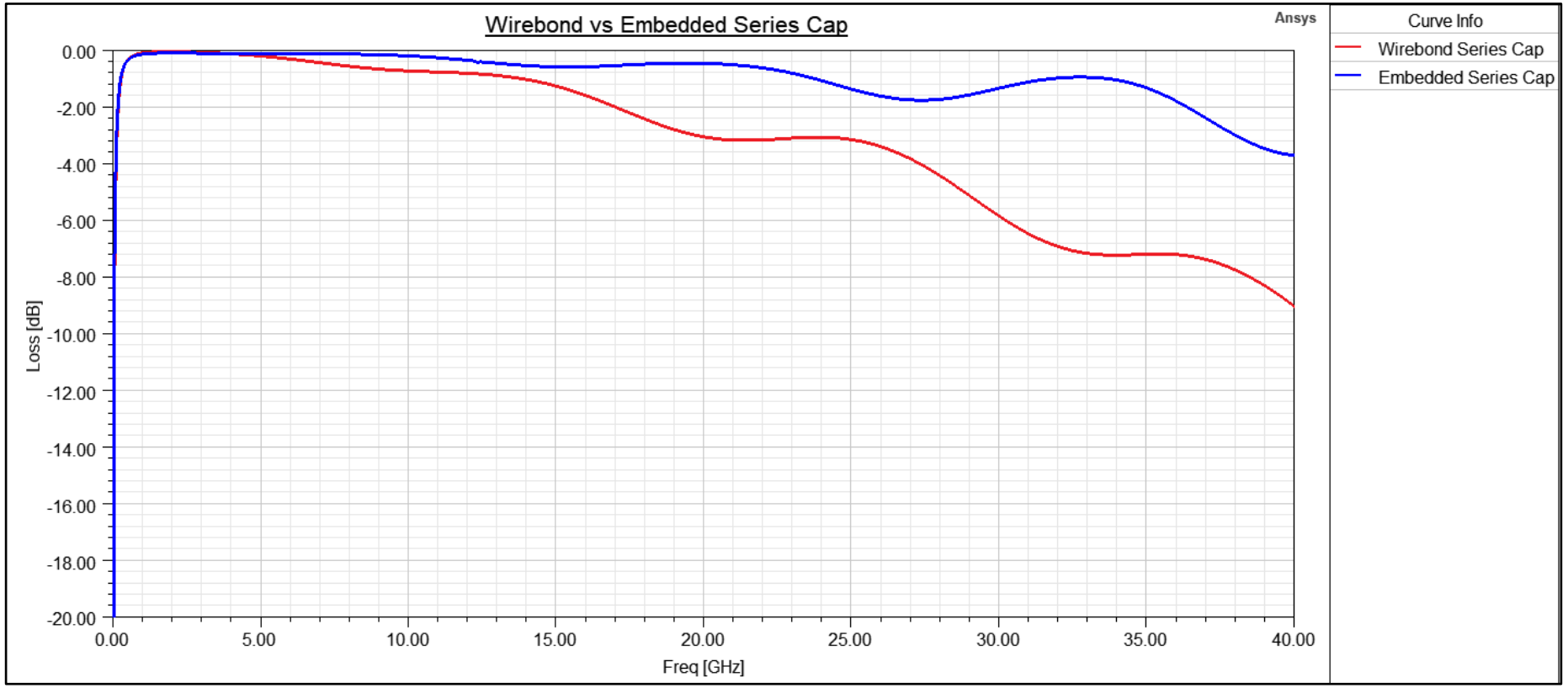


Left 10pF MOS capacitor on Rogers 4350 test board with wirebond connection. **Right** 10pF MOS capacitor embedded in epoxy filled Rogers 4350 test board with via to transmission line.

Embeddable MOS Capacitor

Model - Wirebond vs Embedded - Results

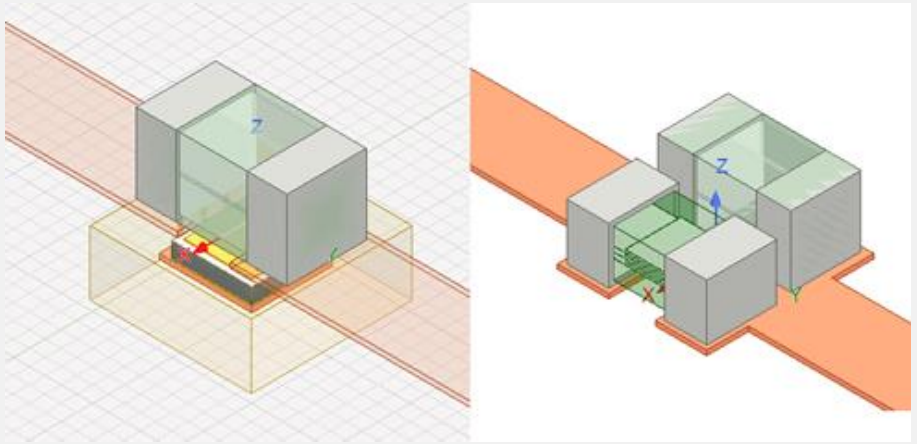
- Wirebond degrades at 5 GHz
- Cap performance extends beyond 20 GHz with minimal loss with embedded method



Embeddable MOS Capacitor

Modeled Performance – Gain Equalizer

- **Modeled performance in Ansys HFSS**
- **Surface mount model**
  - Kyocera-AVX Ultrabroadband Resistor mounted in parallel with generic MLCC style capacitor
    - All components 0402 size
- **Embedded model**
  - Kyocera-AVX Ultrabroadband Resistor mounted with embedded MOS capacitor
    - MOS capacitor is same value as MLCC style capacitor
  - Board space reduced using the embeddable
  - Epoxy filled where the embeddable is used
- **Transmission lines and board remained same other than noted changes**
  - Rogers 4360G2, 50 ohm lines



Left Broadband resistor mounted in series over an embedded 10pF MOS capacitor. **Right** Broadband resistor and surface mount 10pF capacitor in series on test board

Embeddable MOS Capacitor

Model – Gain Equalizer - Results

- Both performance as gain equalizers is similar in the slope
- After equalization slope surface mount components have sharp roll off
- Using embedded capacitor slows the roll off through 40 GHz