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The Coolest Ideas Under the Sun
SAN DIEGO 2023

FROM DESIGN TO HARDWARE

Markus Loerner, Market Segment Manager RF Components

ROHDE&SCHWARZ
Make ideas real

FROM DESIGN TO HARDWARE

TUMA18: From Design to Hardware

Speaker: Markus Loerner

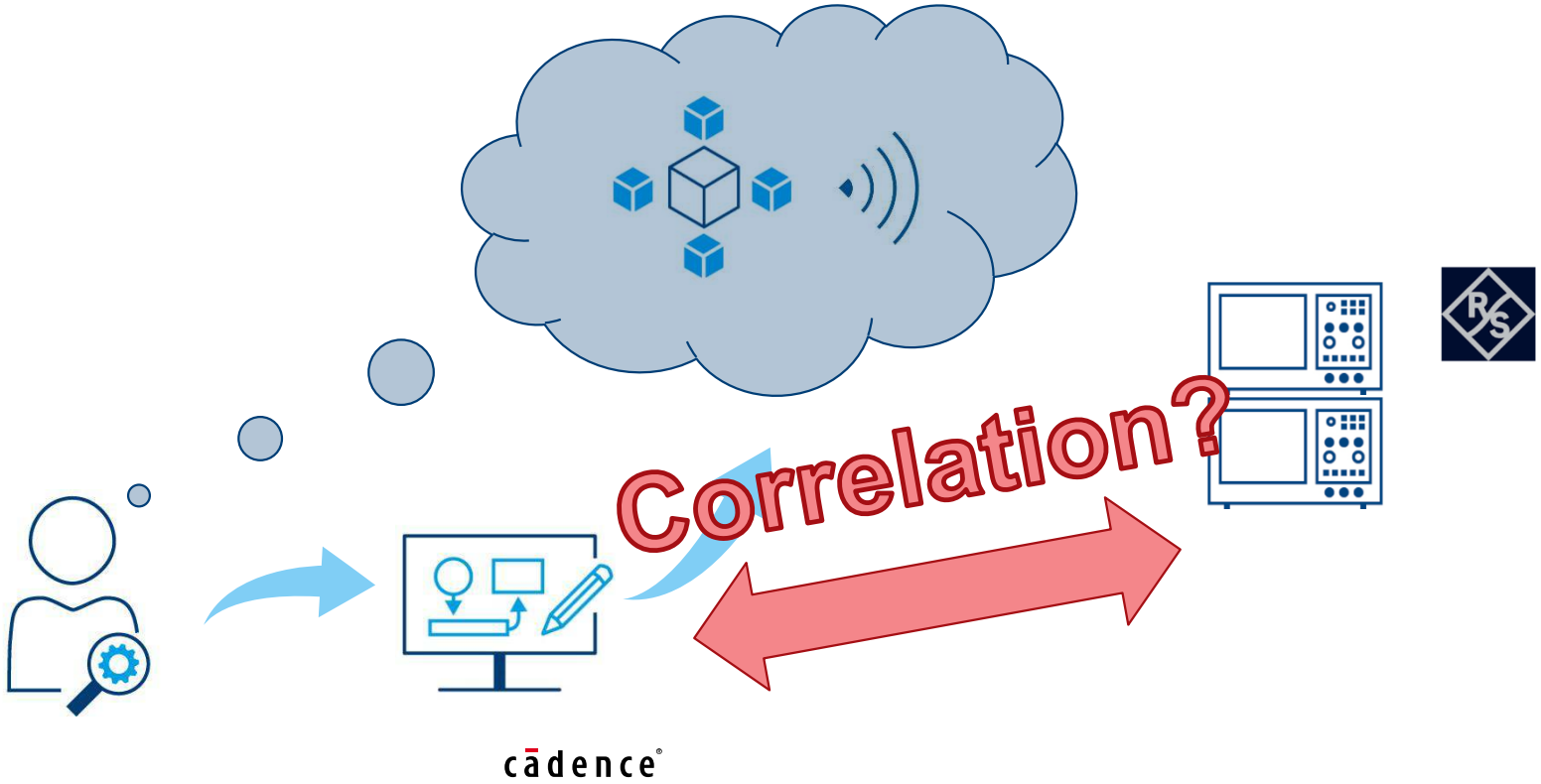
Speaker organization: Rohde & Schwarz

Location: MicroApps Theater, Booth 2447

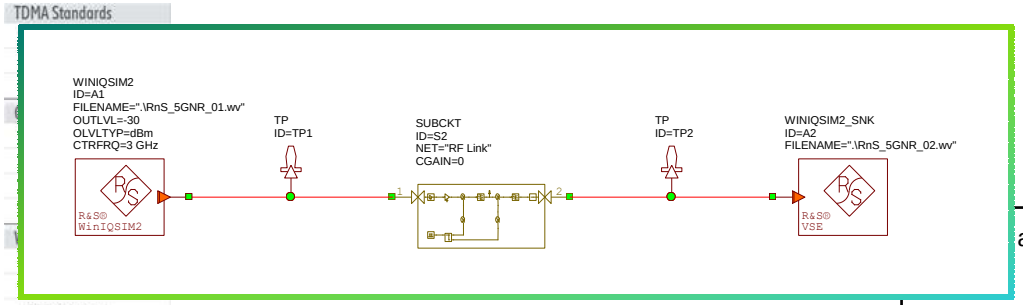
Abstract:

New designs starts in design software and simulation. The important topic is how good can later usage be simulated at an early design phase for risk mitigation. To get as close as possible one wants to simulate with real application data and understand the system level performance with standard compliant key performance indicators such as EVM. Ideally for an active system, the design phase allows a closer look to performance improvement using digital predistortion. This session will look into methods to control risks in the design while looking at standard compliant performance and possible enhancements using DPD.

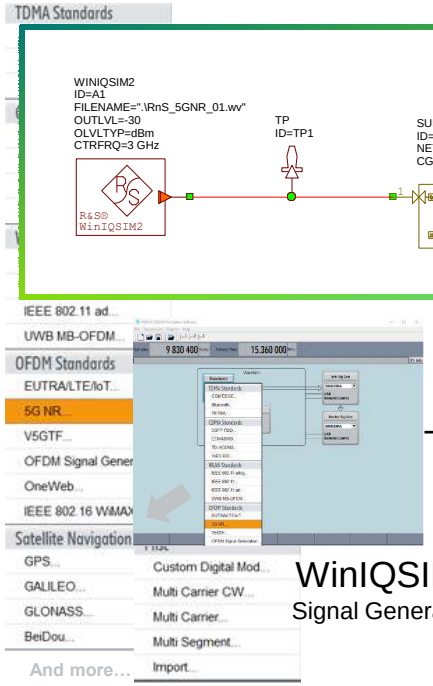
FROM SIMULATION TO HARDWARE IMPLEMENTATION



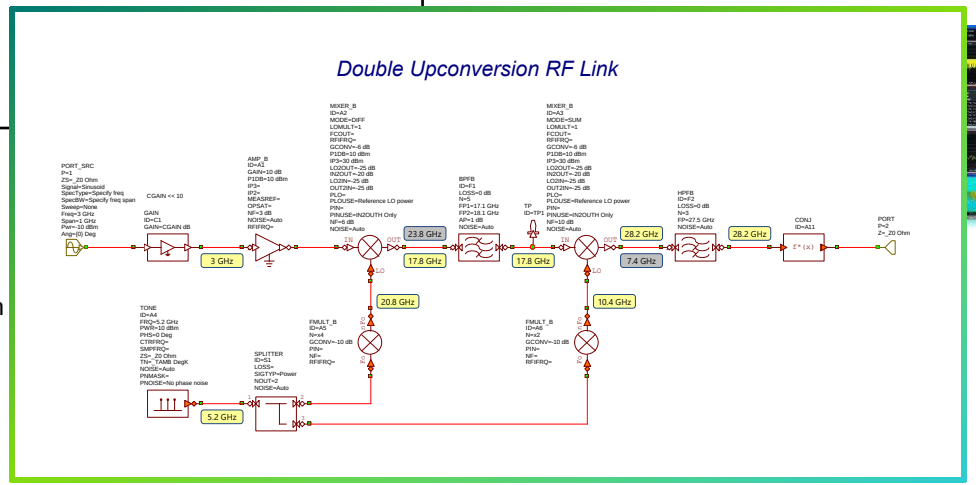
JOINT SOLUTION: R&S AND CADENCE



and/or demodulated data for post processing

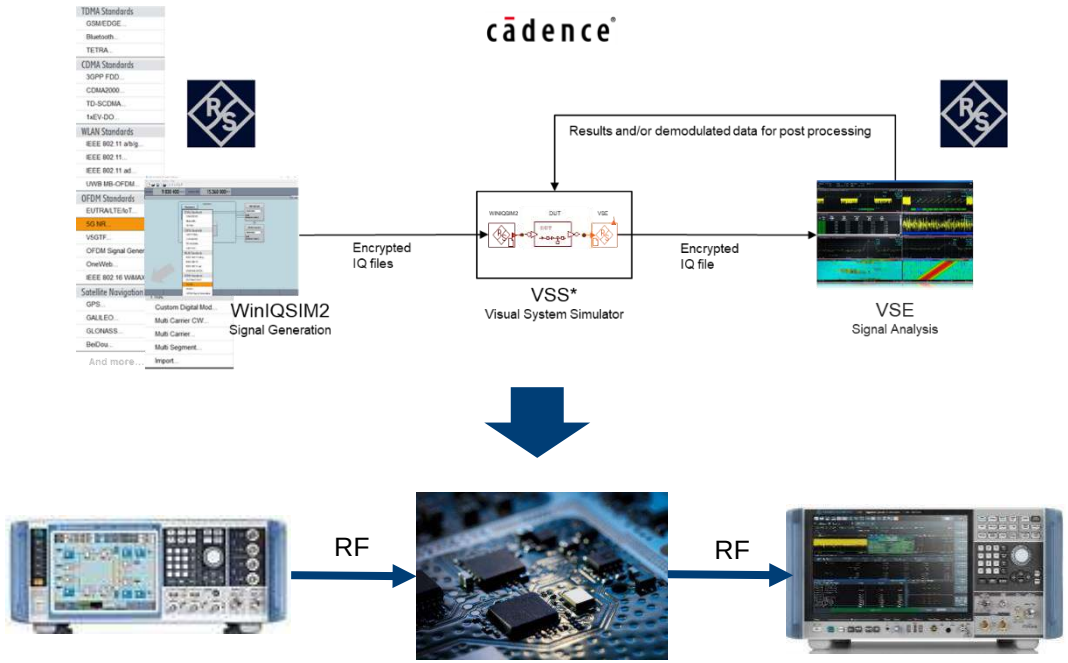


WinIQSIM2
Signal Generation

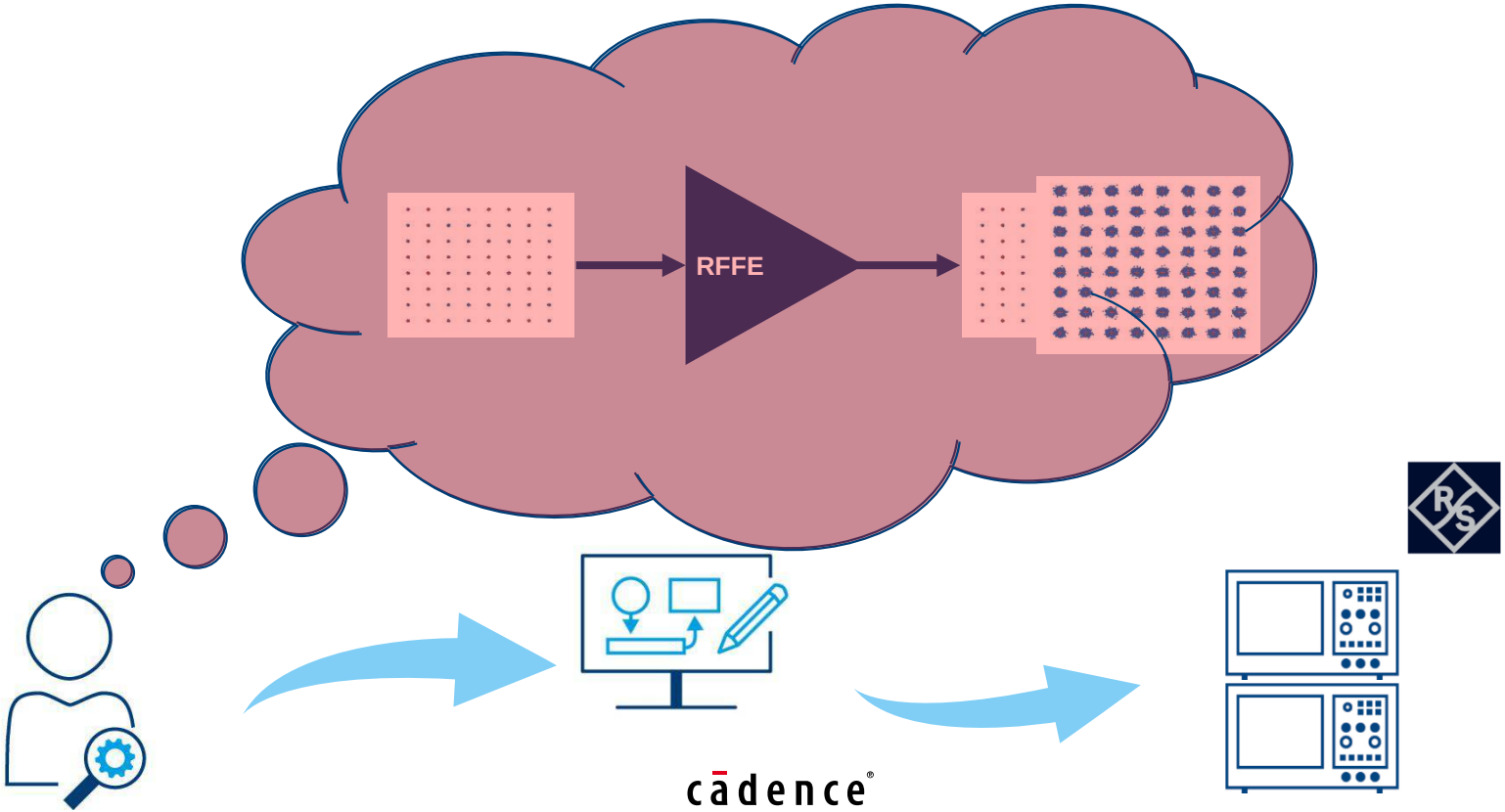


VSE
Signal Analysis

JOINT SOLUTION: AND CADENCE CORRELATION PATH



FIND FULL RFFE CAPABILITIES



LINEARIZATION / DPD

- PAs often driven close to saturation for max power efficiency, but in non-linear operation: compression & memory effect
- Linearization for compensation
- Understand system level performance with ideal predistortion needed

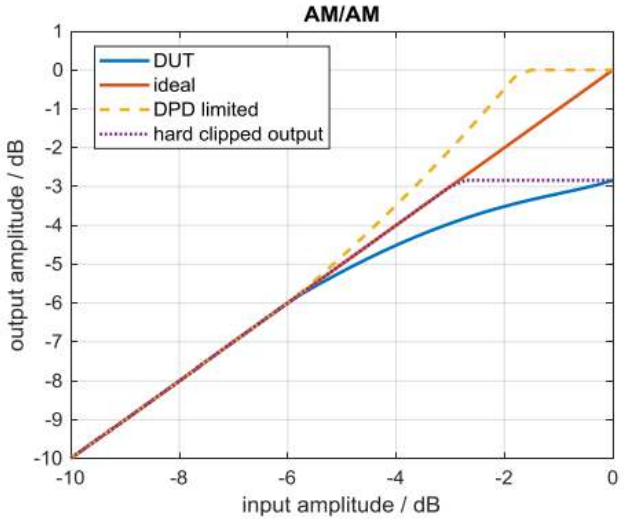
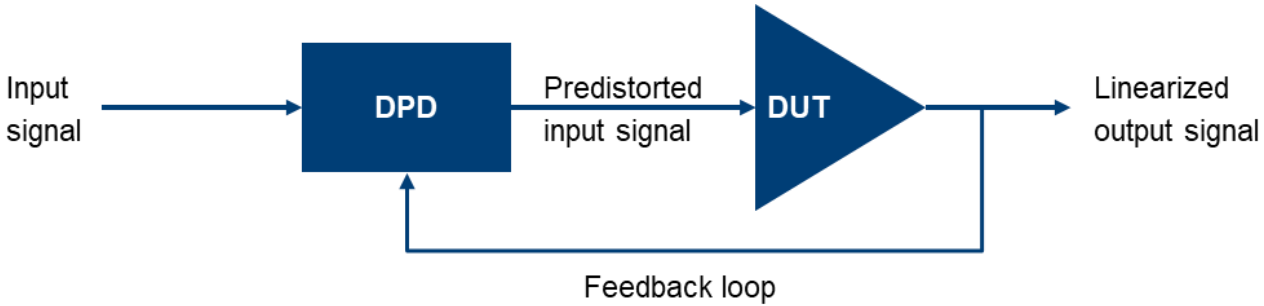
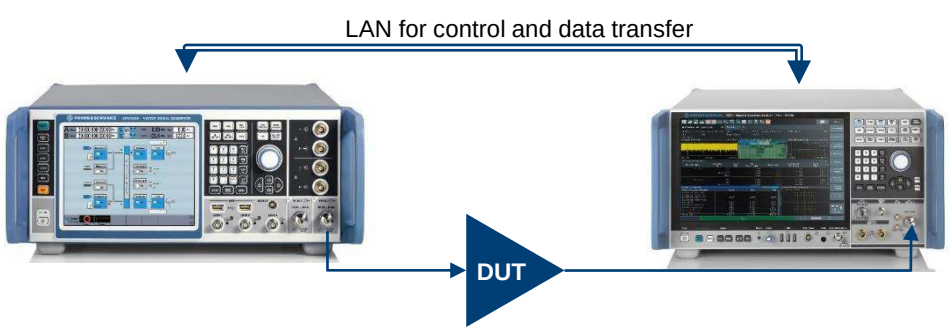
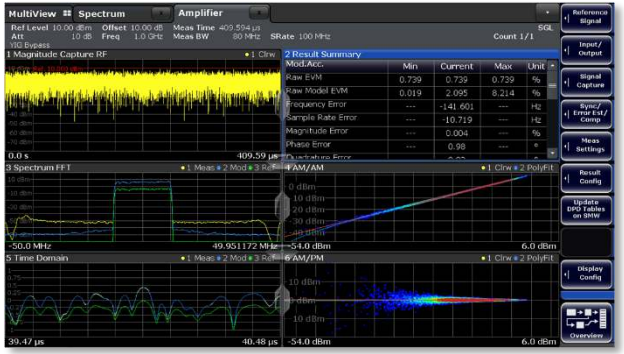


Figure 4 Overview plot: measured AM/AM, ideal output, pre-distorted input signal, and target output signal (hard clipped)



PROVEN HARDWARE SOLUTION





R&S®FSW-K18D Direct DPD

- Iterative approach
- Compensates for memory effects
- Excellent performance especially for amplifiers with memory effects

- Reference for best possible
  - Suppliers typically do not have access to DPD algorithms used by system integrators

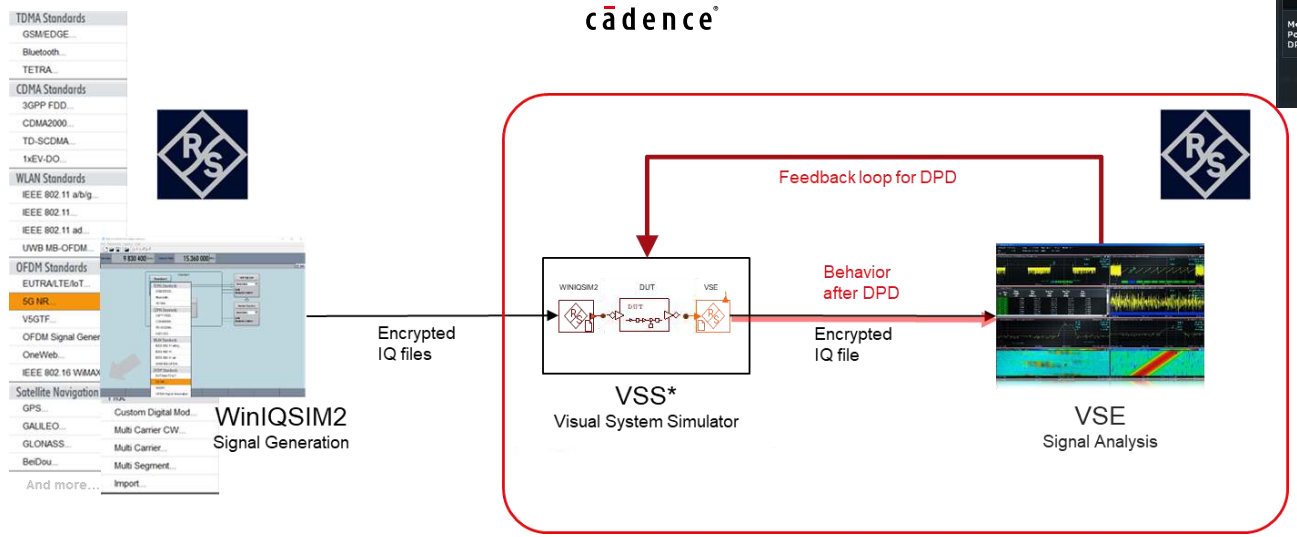
R&S®FSW-K18M memory polynomial

- Memory polynomial model based on Direct DPD result
- Modeling can be adopted in order and memory depth
- Model verification on DUT

- Proves easy linearization of RFFE solution

LINEARIZATION / DPD IN EDA

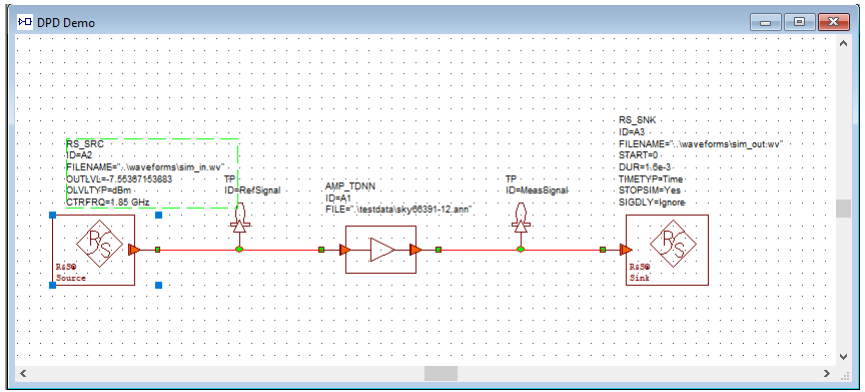
- Why wait until tape out?
- Apply same concept to simulation
- Improve hardware before 1st run



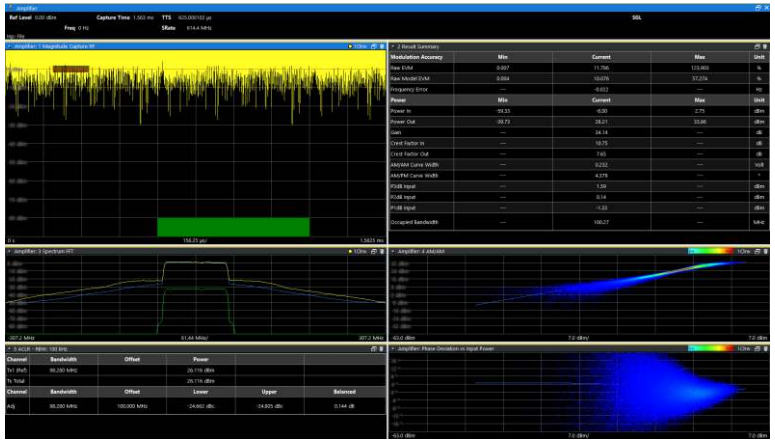
PRE-DISTORTING AN RF-AMPLIFIER PURELY IN SIMULATION

Script controlling both
software packages:
Cadence VSS and R&S VSE

RF simulation of PA in Cadence VSS



Iterative Direct DPD in R&S VSE



TAKE AWAY'S

- The earlier you understand linearization benefits the better
  - Risk management and faster design
  - Able to take pre-caution and action in physical design
- Combination of Cadence VSS EDA with signal processing and Direct DPD by Rohde & Schwarz gives you access to proven process
- Matching approach between EDA system simulation and hardware verification

- NEW: Works also for devices developed in Cadence® Virtuoso through VSS

- Further reading: Investigate RF Power Amplifier Linearization Benefits in EDA | Rohde & Schwarz (rohde-schwarz.com)

- **Reached goal of faster and more accurate design process for an efficient RF front end**