Leibniz Institute for high performance microelectronics

SiGe BiCMOS Technologies for Integration of THz and Power Efficient mm-wave Systems

Andreas Mai – Department Head Technology

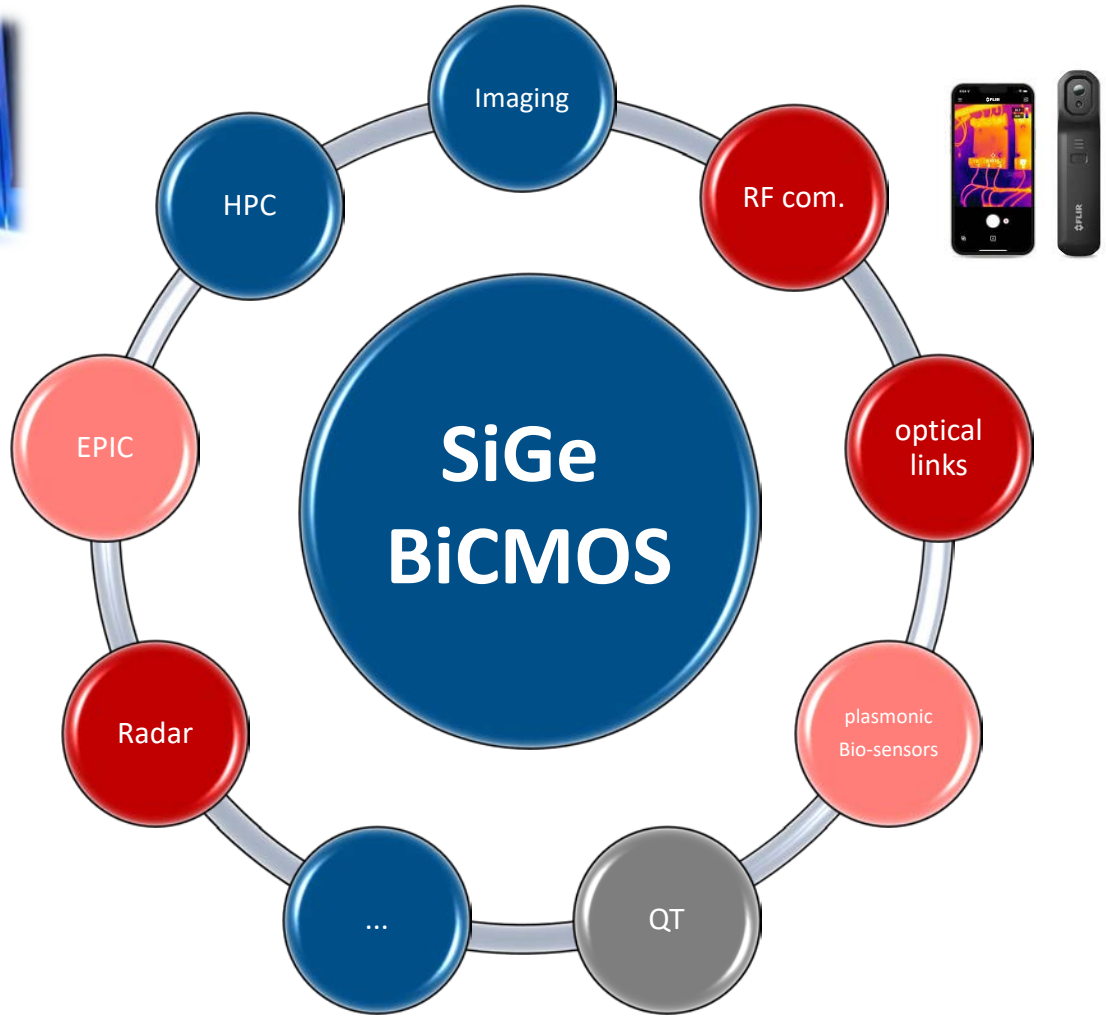
IMS 2023 MicroApps Session

June 13th 2023

SiGe BiCMOS Technology & Applications

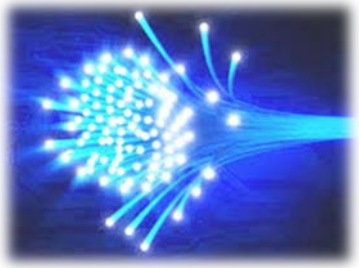
- Datacenters & HPC servers

- For automotive transport
  77 GHz & > 100 GHz

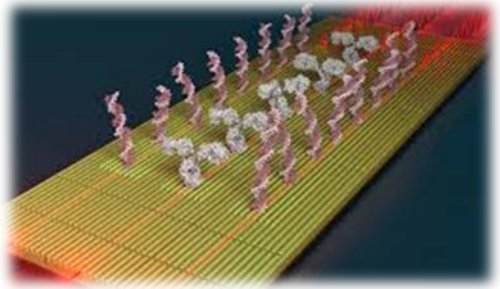


- Wireless modules & backhaul

- Fiber communication



- On-chip for edge sensing

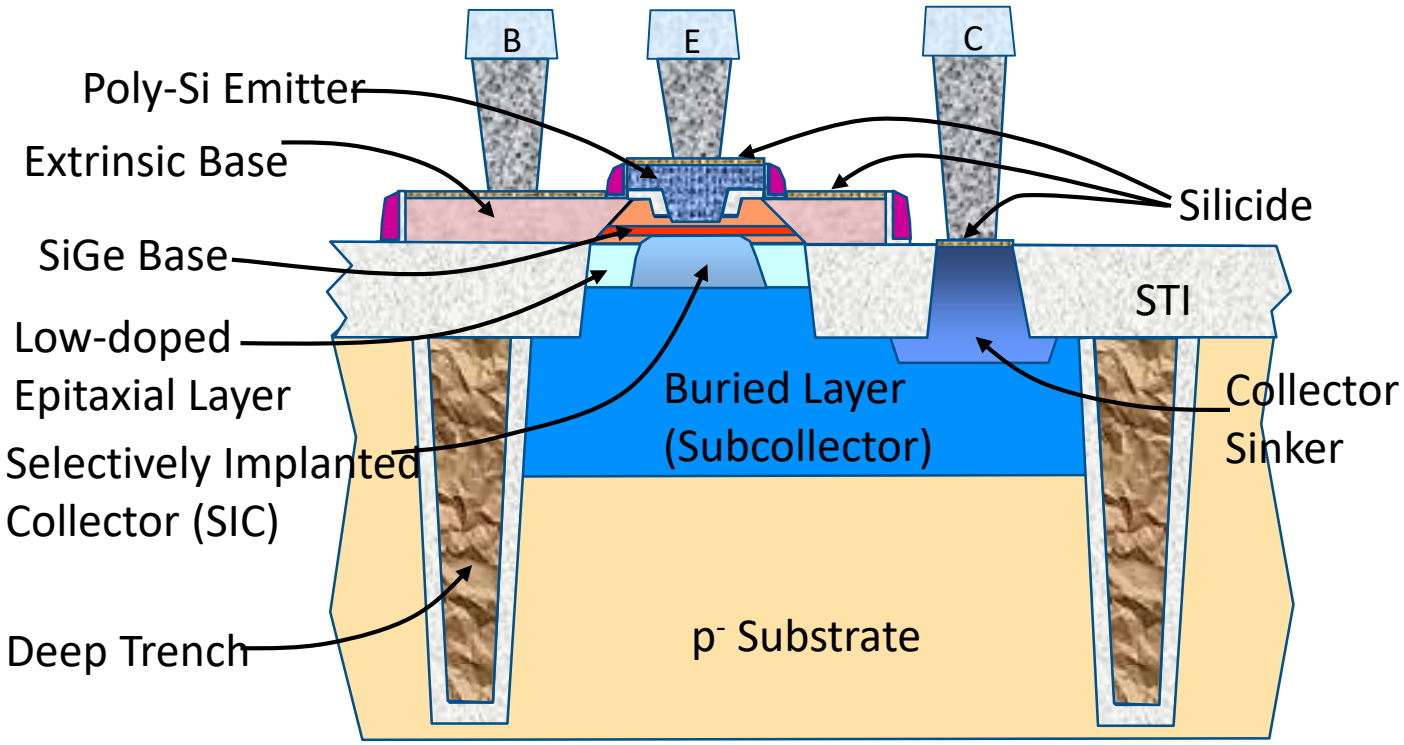


SiGe BiCMOS Technology

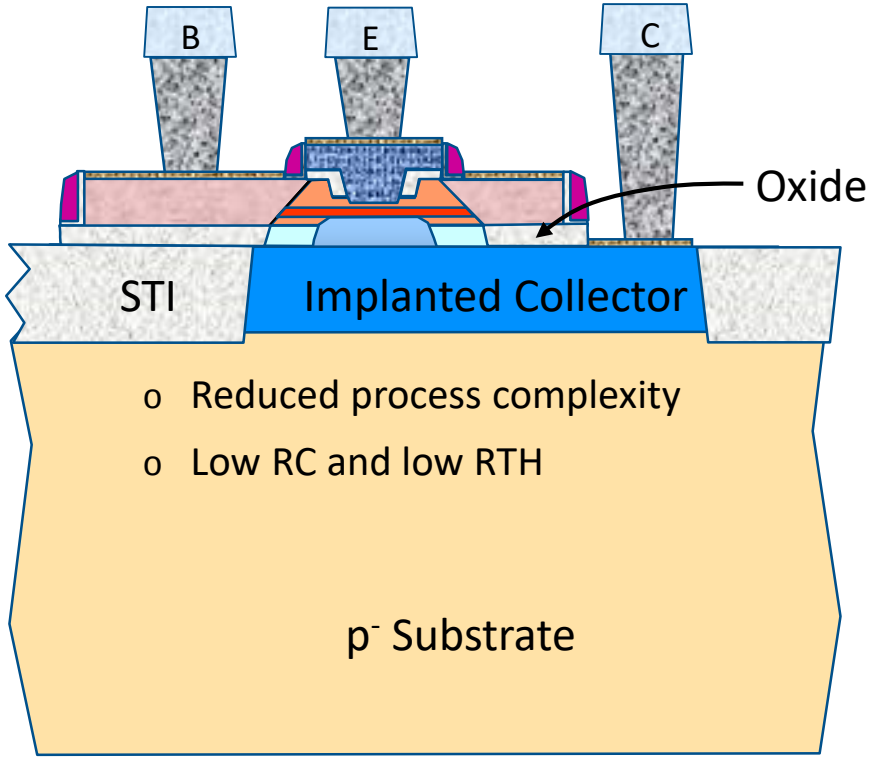
- Ongoing demand for increasing operation frequencies of MMICs
  - Higher communication bandwidth
  - Higher special resolution of radar
  - THz imaging and sensing ...
- SiGe HBTs extend RF performance beyond that of state-of-the-art CMOS
- IHP aims at providing high-performance BiCMOS technologies before their availability at industrial level
  - 3rd generation of 130 nm BiCMOS technology currently developed => **SG13G3**
  - First early access for IC fabrication => tapeout March 2023

Cross Section of High-Performance SiGe HBT

Classical approach with deep trench isolation

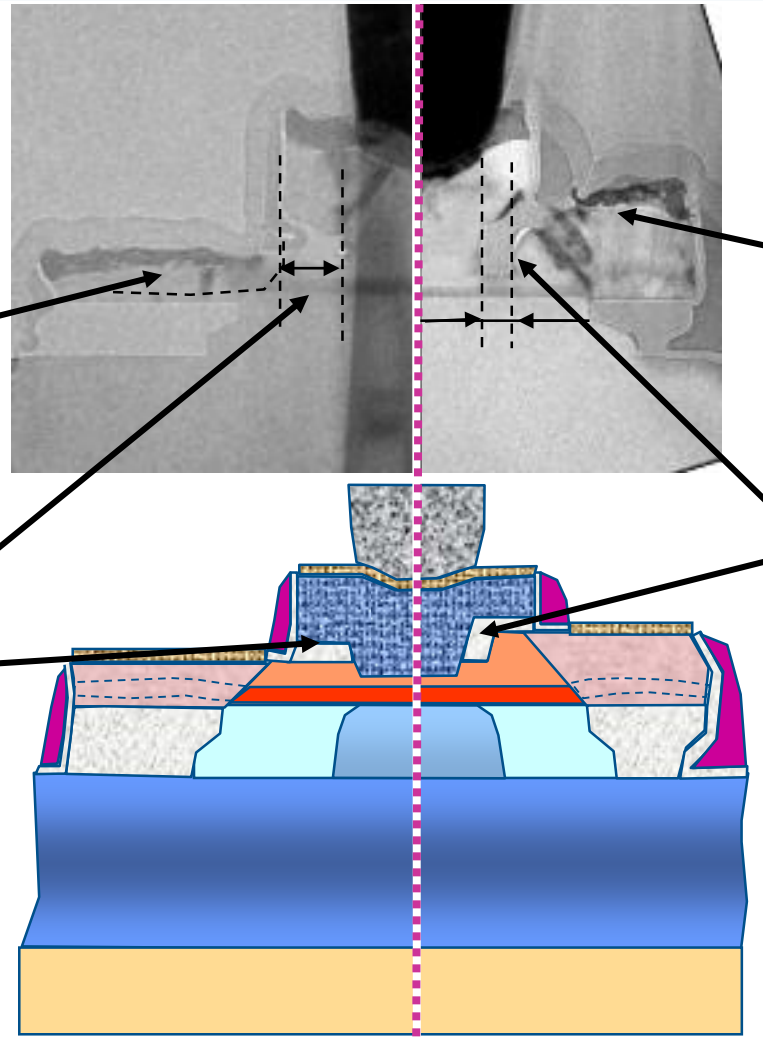


IHP approach w/o deep trench



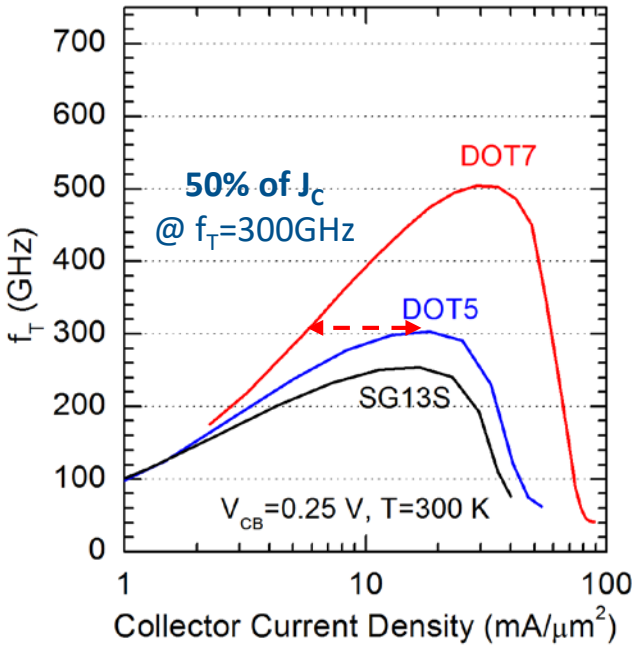
SiGe-HBT Structure with Elevated Extrinsic Base

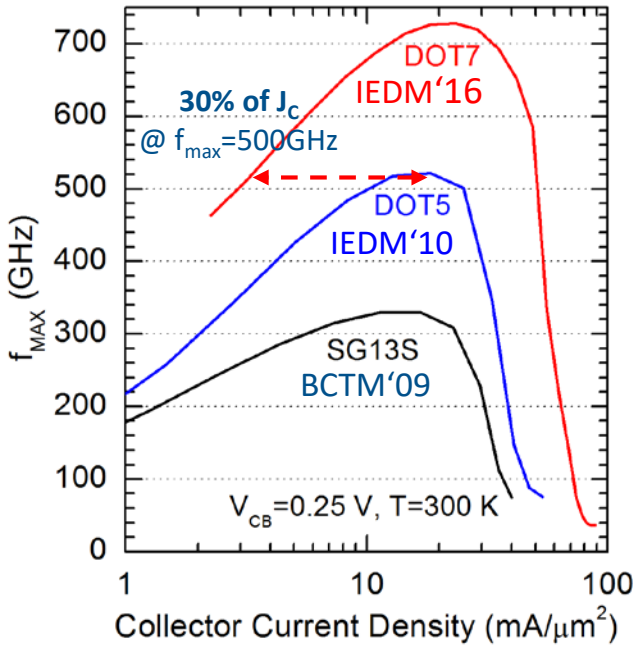
- Single-Poly HBT with non-selective base epi (IHP 0.25 µm BiCMOS)
- Extrinsic base grown with base epi
- Base-link region not self-aligned to emitter window

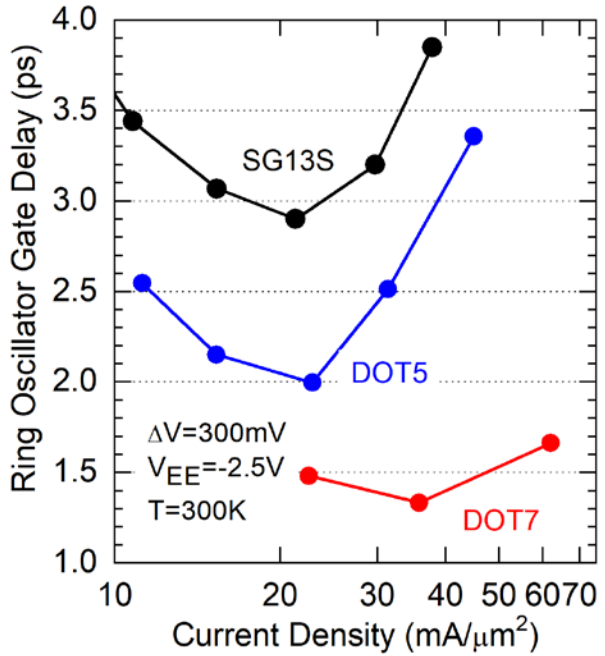


- Elevated Extrinsic Base (IHP 130 nm BiCMOS)
- Additional Si epi for extrinsic base
- Base-link region self-aligned to emitter window
- Thin emitter-base spacer

Evolution of RF-Performance of SiGe HBT





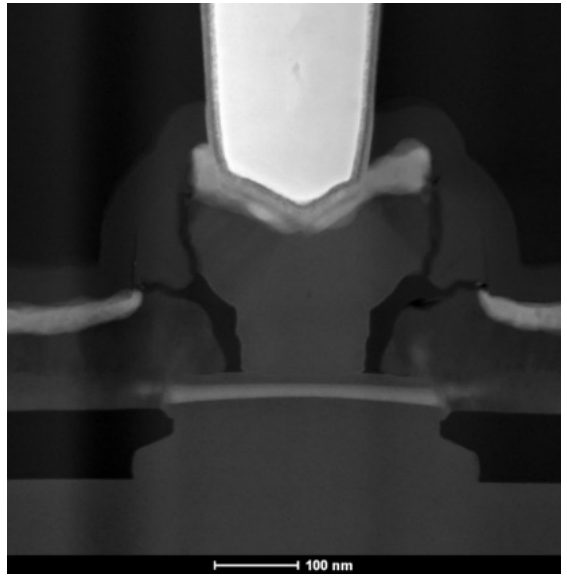


- SG13S: IHPs 1st generation 130 nm BiCMOS
  - HBT with non-selective epitaxial growth of base and elevated extrinsic base
- HBT optimization towards 500 GHz f_{MAX} (DOT5) & towards 700 GHz f_{MAX} (DOT7) ➔ EU project DOTFIVE & DOTSEVEN
- obvious collector current densities & power consumption @ mm-wave frequencies

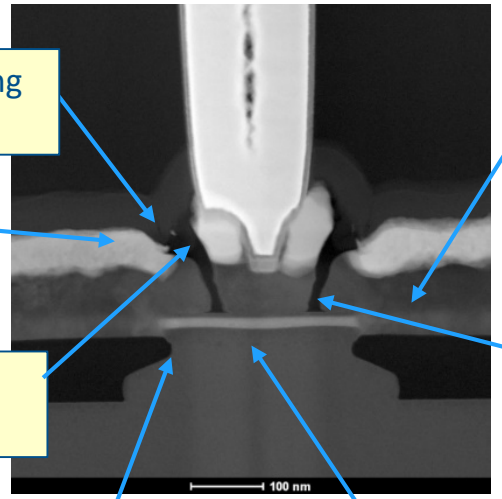
SiGe HBT Process Modifications

- Starting point: IHP's 130 nm BiCMOS "**SG13G2**"
  - Highly-doped collector isolated by STI
  - NSEG with elevated extrinsic base
- Exploration of HBT performance limits irrespective of CMOS process constraints

Starting Point SG13G2



Final Status (D7)



Narrower Silicide Blocking Spacers

Ni Silicide

Scaled Emitter-Poly Width & Collector Window

External Base Formation

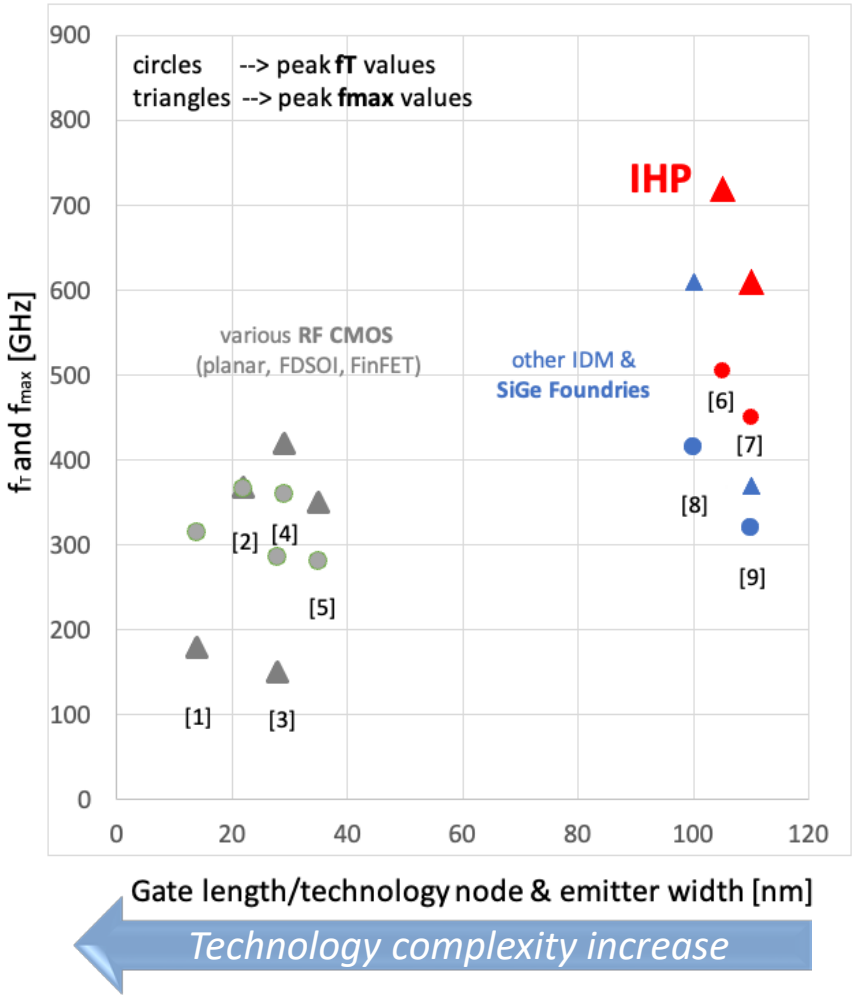
Reduced Width of Emitter & Emitter-Base Spacer

[Heinemann, IEDM 2016]

Millisecond Flash Annealing & Low-Temperature Backend

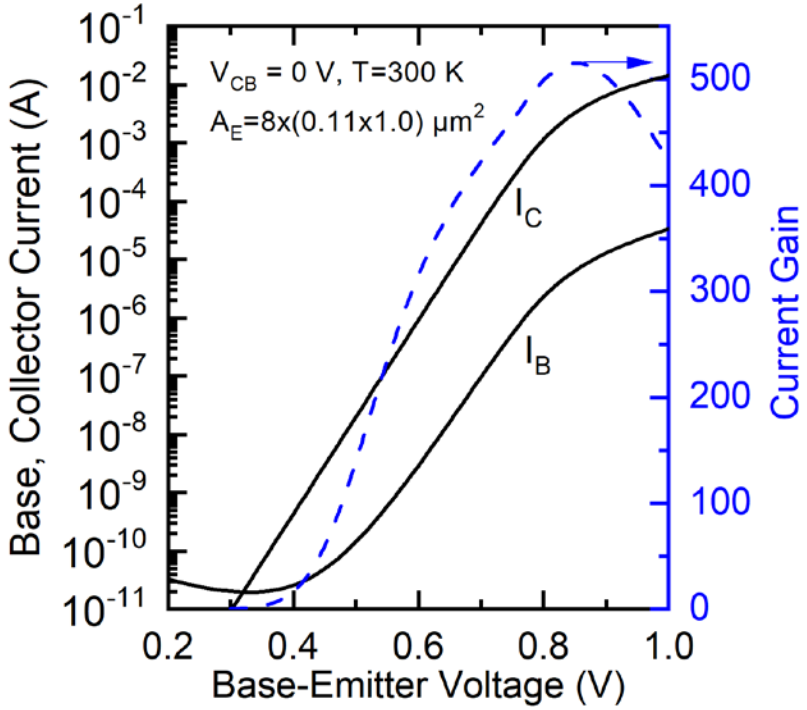
SiGe Base Profile & Adjacent Low-Doped Emitter & Collector Region

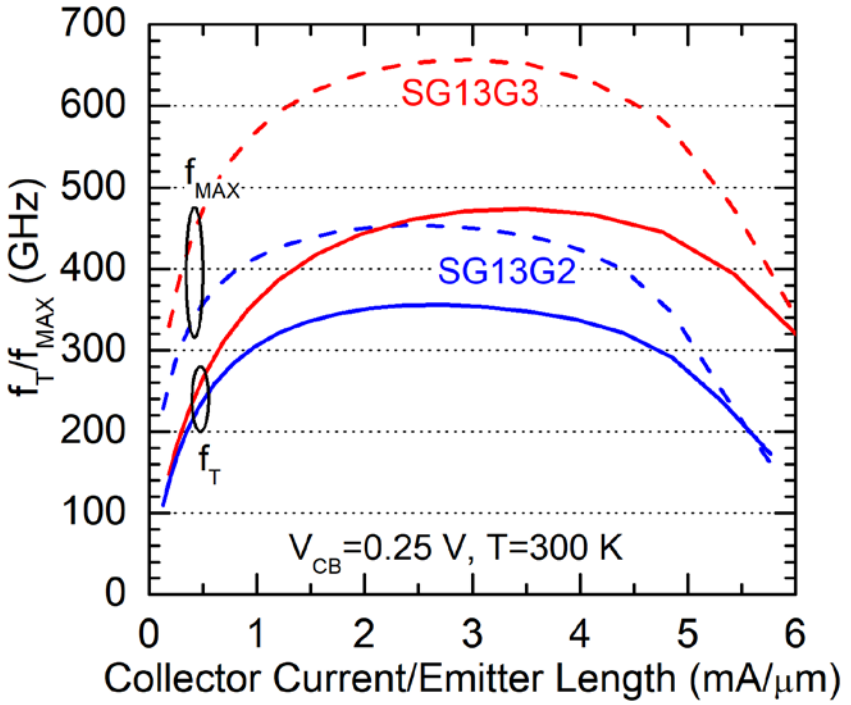
SiGe HBT and BiCMOS



- SiGe BiCMOS targets frequencies and data rates which are out of reach for state-of-the-art CMOS ➔ physical limitations for RF-CMOS
- Compact and highly scalable technology
- Cut-off frequencies (f_T, f_{MAX}) are
  - Up to 2x higher for SiGe-HBT/BiCMOS at lower process complexity
  - typically 3-10x larger than operating frequency
  - +100 GHz application as 6G, D-band communication, radar etc. require SiGe RF technology as a scalable manufacturing technology

High-Speed HBT Characteristics (SiGe-BiCMOS)





- HBTs with aggressively scaled doping profiles show ideal I_C and I_B over wide range of V_{BE}
- Non-ideal I_B at V_{BE} < 0.5 V indicate tunnelling through narrow base-emitter junction
- Cutoff frequencies of 470 GHz f_T and 650 GHz f_{MAX} far beyond predecessor process SG13G2

IHPs 130 nm BiCMOS Platform

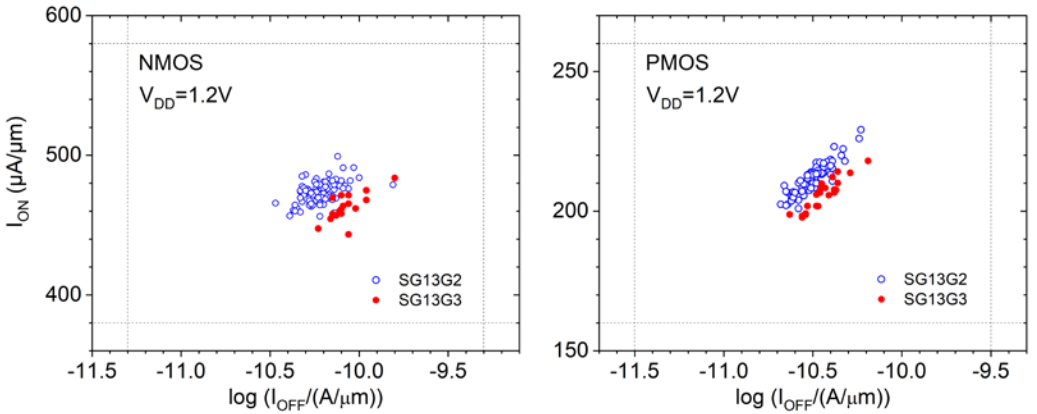
- Progress of HBT technology was adopted for new generations of 130 nm BiCMOS
  - DOTFIVE-HBT integrated in SG13G2
  - DOTSEVEN-HBT integrated in currently developed SG13G3
    - First PDK version available => Early-access run in March 2023
    - Ongoing process development includes: NiPtSi process, HBTs for higher breakdown voltages …
    - Process stabilization/qualification till 2025

Key parameters of high-speed HBTs:

	SG13S	SG13G2	SG13G3
Peak f_T (GHz)	240	350	470
Peak f_{MAX} (GHz)	340	450	650
BV_{CBo} (V)	4.7	4.2	3.7
BV_{CEo} (V)	1.65	1.6	1.5

CMOS Process & Passives

- SG13G3 fulfills same specifications as SG13G2 for 1.2V core and 3.3V I/O devices
  - CMOS process adjusted to accommodate reduced thermal budget for the advanced HBT process
  - $CoSi_2$ process replaced by NiSi
  - Modified gate spacer process to reduce impact on HBT
- Three generations of 130 nm BiCMOS provide similar portfolio of passive components
- Poly-Si Resistors: RPPD, RHIGH, RSIL
  - Sheet resistance values differ slightly for different process generations

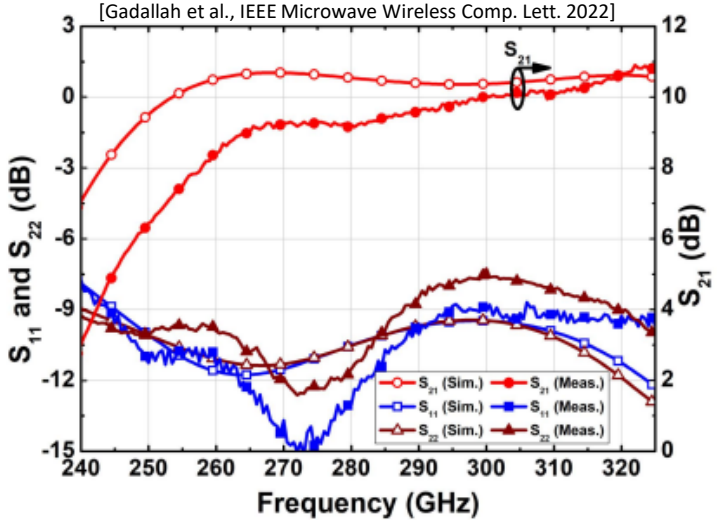


- MOS varactors (SVARICAP)
  - Ongoing development of supplementary devices with improved Q-factor and more linear C(V)
- MIM capacitors
- Thick top metal layers for inductors, transmission lines, and transformers

Benchmark circuit studies

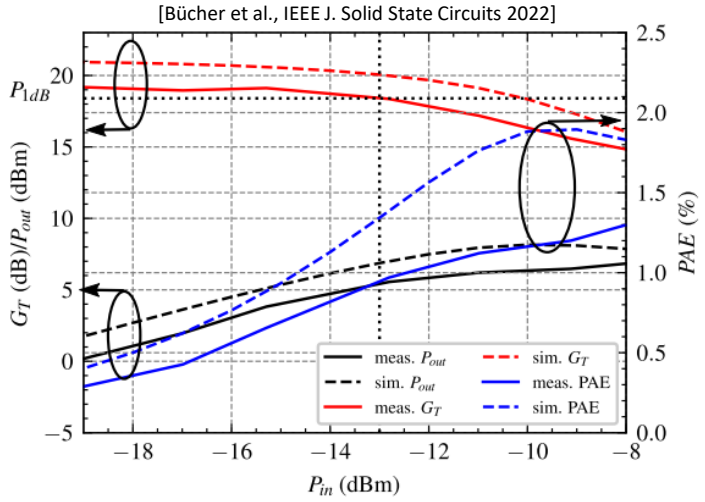
- Performance of new HBT generation benchmarked in early-access fabrication runs of SG13G3 by IHP circuit design groups and external partners
  - 300 GHz low-noise amplifies
  - 300 GHz power amplifiers
  - Distributed amplifier with average gain of 19 dB and over 170 GHz BW

[Gadallah et al., IEEE Microwave Wireless Comp. Lett. 2022]



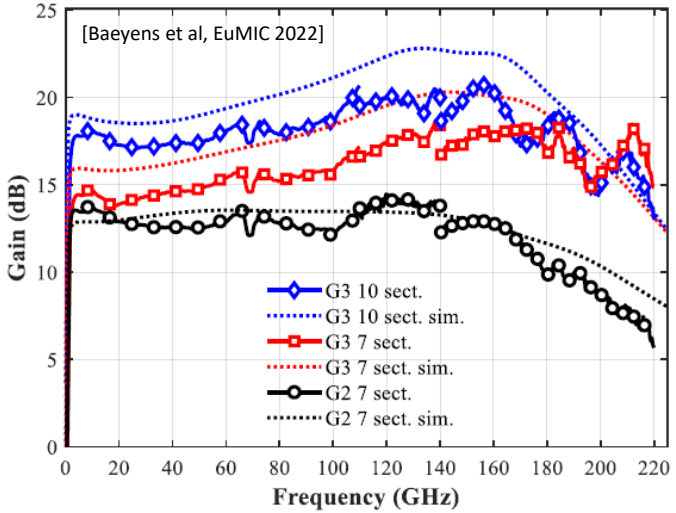
- Measured and simulated S-Parameter of 300 GHz LNA with simulated NF of 11 dB

[Bücher et al., IEEE J. Solid State Circuits 2022]



- P_{out} vs. P_{in}, large-signal gain, and power-added efficiency (PAE) at 270 GHz.
- Output referred compression point and PAE are almost constant over 240-300 GHz band

[Baeyens et al, EuMIC 2022]



- A Single-Stage Low-Noise SiGe-HBT Distributed Amplifier with 13 dBm Output Power and 20 dB Gain in D-Band
- Bandwidth of G3 amplifier >220 GHz, G2 ~184 GHz

Conclusions

- Advances SiGe HBT architecture opened up room for strong performance enhancement
  - Formation of base link by additional epitaxial step facilitates low R_B without compromising C_{BC}
  - Collector module without deep trenches supports low R_C & R_{TH} and reduces process complexity
  - Advanced epi processes support scaling of vertical profiles and lateral device dimensions
  - Reduced thermal budget of NiSi vs. $CoSi_2$ supports high dopant activation
- Advanced SiGe HBTs integrated in three generations of 130 nm BiCMOS process
- SG13G3 provides unsurpassed cutoff frequencies f_T of 470 GHz and f_{MAX} of 650 GHz with BV_{CES}= 3.7 V

Acknowledgment

- Thanks to my colleagues at IHP in particular:
  - My team of **Technology Department at IHP**
  - Holger Rücker, Bernd Heinemann, Yuji Yamamoto, PDR-group
- Thanks to different public founded projects (EU, ILB & BMBF) as TARANTO, FMD

- *Reference list for slide XX:*

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5) H. Li et al., IEEE Symposium on VLSI Technology, 2007, pp. 56-57,
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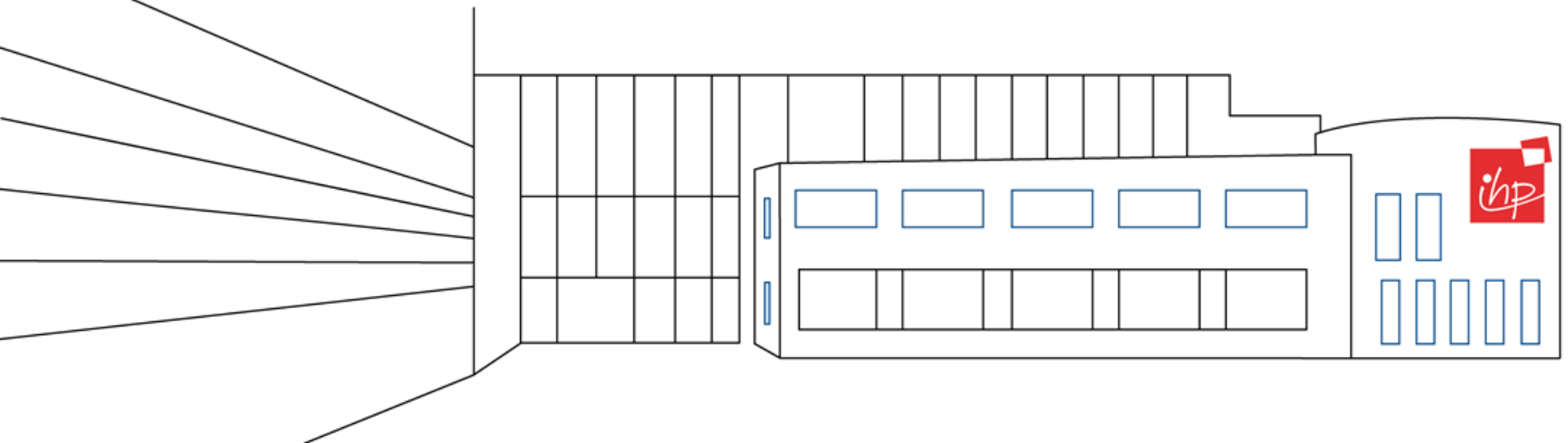

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SiGe BiCMOS Technologies for Cryogenic Applications

René Scholz – Group Leader Reserch & Prototyping Service

IMS 2023 MicroApps Session

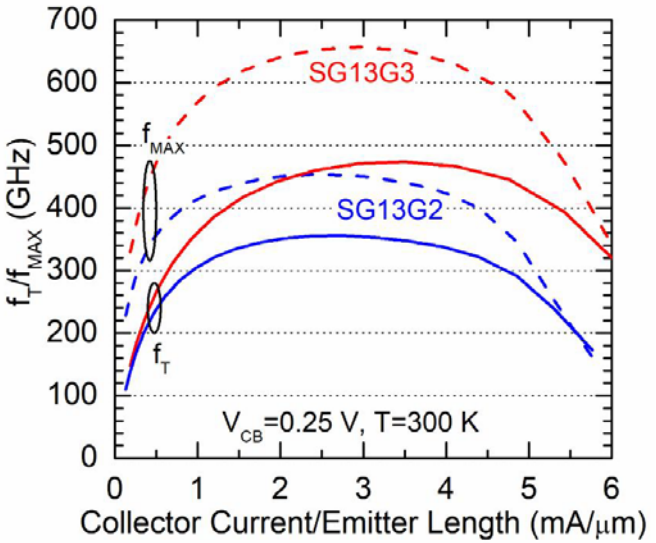
June 13th 2023

Evolution of High Performance BiCMOS Technologies

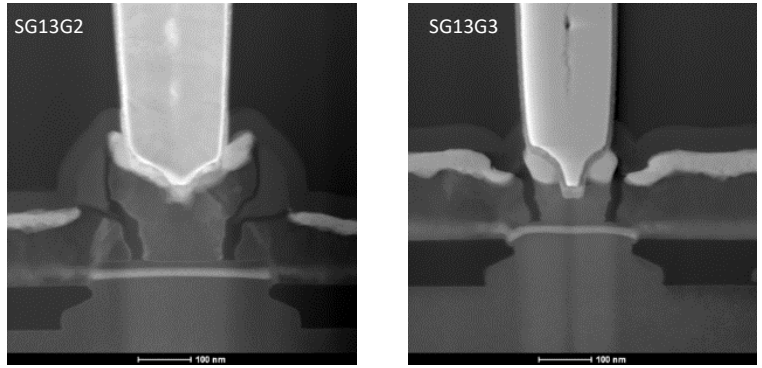
	SG13S	SG13G2	SG13G3
HBT f_t / f_{max}	250 / 340 GHz	350 / 500 GHz	470 / 650 GHz
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CE0}	1.7 V	1.6 V	1.5 V
CMOS node	130 nm		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
Resistors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	2.1 fF / µm²
Metallization	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm)	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm	*Cu: 4 + 2 (3µm) Al: 2 (3µm

*Cu BEOL from X FAB

- SG13G2 technology is selected for cryogenic applications



f_t and f_{max} of IHP SG13G2 and SG13G3 technology



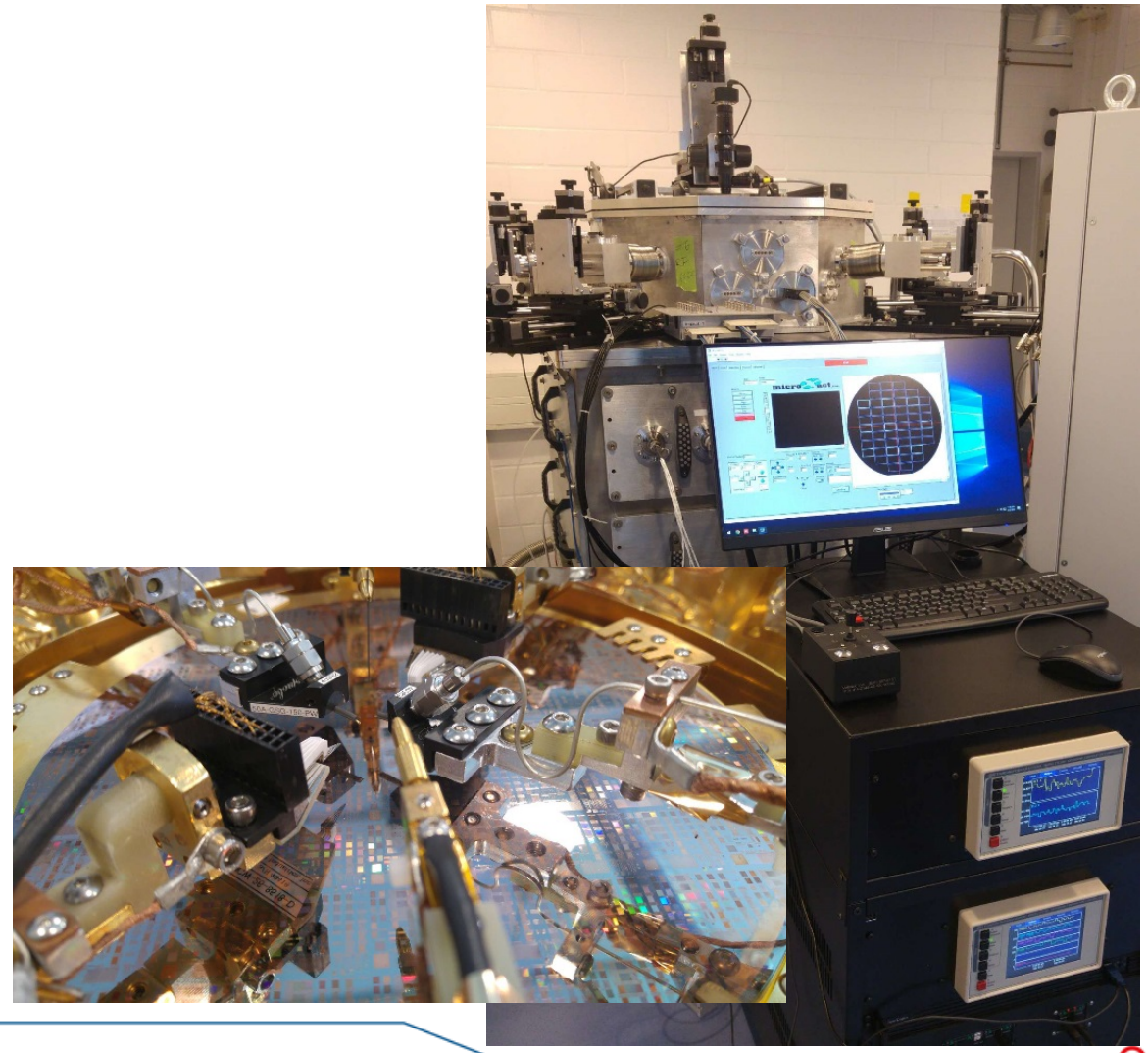
TEM cross section of an HBT with elevated extrinsic base regions from (a) the SG13G2 process and (b) a t SG13G3 HBT

Steps to Develop PDK for Cryogenic Applications

- Modelling and manufacturing of a state-of-the-art IHP SG13 BiCMOS process.
- Development of Cryo-PDK for IC design in CAD tools at 4..10 K.
- Development of test structures and circuits for Cryo-PDK evaluation.
- Annotate the data from the measurement results of the provided test circuits back to PDK to tune the model cards.

200 mm Semi-Automatic Cryogenic Probe Station

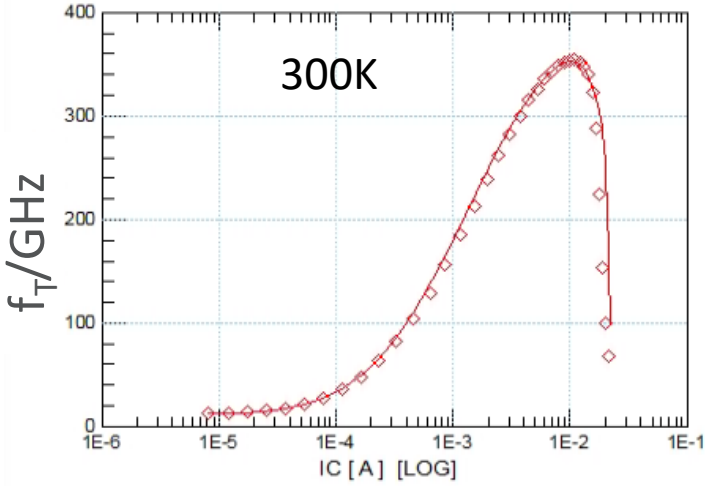
- DC and RF on-wafer measurements
  - 6 probe arms simultaneously
  - 6 x DC single needles
  - 2 x DC multi-probe wedges (10 pin)
  - 2 x RF (67 GHz)
- Measurement of PCM structures including statistical data
- Probe Station installed Q1 2023
  - 10 K base temperature verified
  -

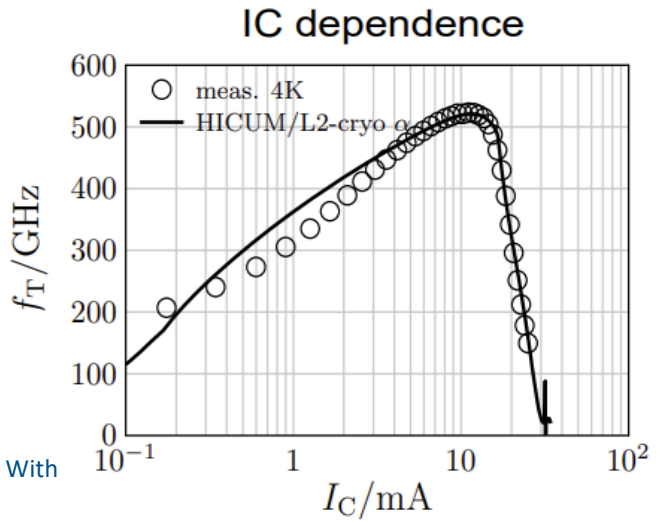


HBT Model improvements

- Physics-based SiGe HBT compact model for cryogenic application is released (HICUM/L2-cryo alpha 0.2)*:
  - Direct tunneling for forward and reverse components
  - TAT BC current
  - Modelling of lower and upper boundaries of model parameters
  - Effective bandgap related model parameters added
  - Power law model with linear extension for resistance
  - Thermal voltage for all smoothing functions

- Increasement of transit frequency f_T from 317 GHz (measured at 298 K) to 525 GHz (measured at 4.3 K)





* J. Xiaodi, M. Mueller, P. Sakalas, A. Mukherjee, Y. Zhang and M. Schroeter, "Advanced SiGe:C HBTs at Cryogenic Temperatures and Their Compact Modeling With Temperature Scaling," IEEE Journal, 2021.

HBT Model Roadmap

- HICUM/L2-cryo beta version: T_0 = 298 K, T_{sim} = 4 K which includes:
  - VC dependence of current
  - SH (downward bending of IBE and IBC, Increase of IC for output characteristics)
  - noise
  - down to low frequency -> multi-pole thermal network
- HICUM/L2-cryo gamma version: T_0 = 298 K, T_{sim} = 4-77 K (with modelling of avalanche current)
- HICUM/L2-cryo delta version: T_0 = 298 K, T_{sim} = 4-400 K

Cryogenic MOS models

Achievements

- LV+HV MOS model cards (4 K)
- Reasonable agreement with the measurements at 4 K
- Verification for different device geometries
- Verification tool (sim *vs* meas)

Plans

- A ring oscillator measurements at ~4 K are planned for the Q3
- Another model iteration is planned for Q4 2023

Cryogenic Resistor Models

Achievements

- Sheet resistance (SR) was measured for all resistor types at 4 K
- Resistor model cards were updated in accordance to SR-value
- Resistor test circuit has been submitted for fabrication
- The provided model cards have a perfect agreement (simulation *vs* measurements) at 4 K

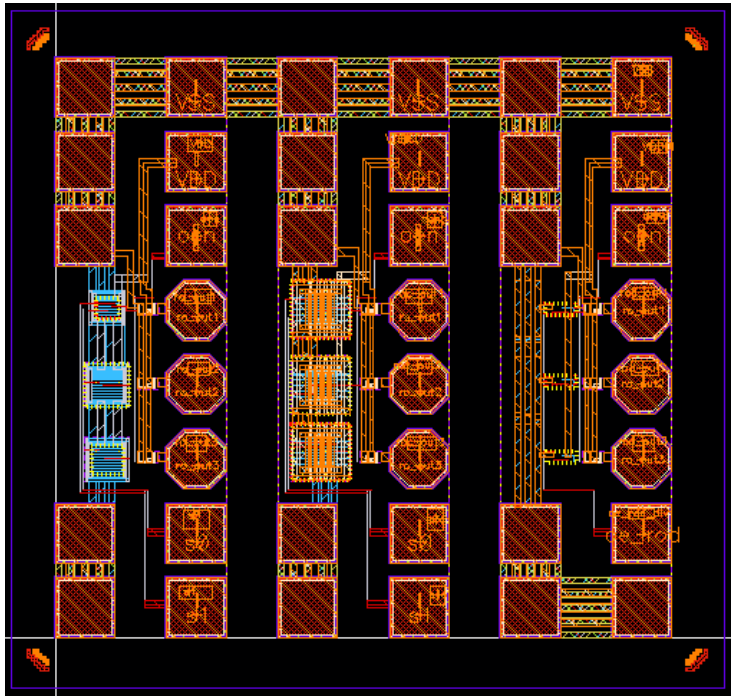
Plans

- Measurements of test circuit and full model extraction of test circuit at 70 K… 4 K

Test circuits development

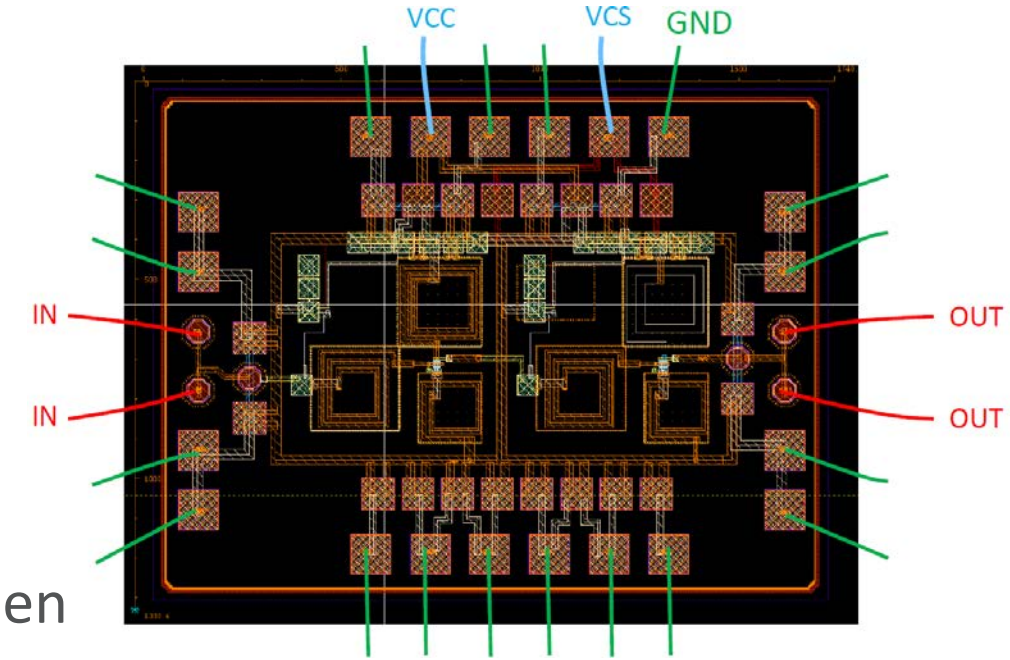
Test circuits were designed and submitted for fabrication:

- Two-stage ring-VCO followed by 1:128 frequency divider
- Bipolar differential amplifier
- Three-stage ring VCO. Output frequency 5.2-7.5 GHz depending on value of the control voltage VC3 (0-3 V)
- Voltage regulator producing a DC output voltage of 2.8 V from a supply voltage VCC between 3 V and 4 V, nominally 3.3 V
- Rppd, Rhigh, Rsil for model extraction



LNA test circuits development

- Four LNAs in G2 are in fabrication:
  - 0_LNA1: 6 GHz LNA, single stage
  - 0_LNA2: 10 GHz LNA, single stage
  - 0_LNA1CAS: 6 GHz LNA, 2 stages
  - 0_LNA2CAS: 10 GHz LNA, 2 stages



- S… …CS open

	f_0	ICC	Gain	NF	Noise Temp.
LNA1	5.5 GHz	1.2mA	14 dB	0.08 dB	6K
LNA2	10 GHz	0.5mA	11 dB	0.13 dB	10K
LNA1CAS	5.5 GHz	2.4mA	27 dB	0.08 dB	6K
LNA2CAS	11.5 GHz	1mA	18 dB	0.13 dB	10K

PDK Status

- Cadence and ADS PDKs alpha versions are available for IHP customers
- Available cryogenic devices: npn13G2, nmos_cryo, pmos_cryo, nmosHV_cryo, pmosHV_cryo, rsil_cryo, rpp_cryo, rhigh_cryo
- Physical Verification Tools: Cadence PVS, Mentor Calibre (not calibrated for cryogenic temperatures yet)
- Simulators: Cadence Spectre (encrypted HBT Spice model),
- ADS (compiled Verilog-A model)
- Initial Version of digital library based on cryogenic models has been released

Roadmap Plans

- Measurements of ring oscillator to verify HBT & MOS models (Q3 2023)
- PEX Measurements of PCM structures to calibrate PEX EDA tools (Q3 2023)
- Measurements of key devices in mK range (Q3 2023)
- Extraction of complete resistor models (Q4 2023)
- Tuning of PDK models and settings based on the measurement results of the test circuits and re-engineer Pcell profiles for best noise performance (Q4 2023)
- Introduction of new devices: TAPs, ESD-devices, Svaricap (Q4 2023)
- ADS and Cadence beta PDK releases (Q4 2023)

Acknowledgment

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Munich Quantum Valley Quantencomputer Demonstratoren – Supraleitende Qubits (MUNIQC-SC)

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https://www.quantentechnologien.de/forschung/foerderung/quantencomputer-demonstrationsaufbauten/muniqc-sc.html

Hochintegrierte und skalierbare Interfaceschaltungen für Quantenprozessoren (HIQuP)

The HIQuP project acknowledges the support of the Federal Ministry of Education and Research (BMBF) within the framework program “Enabling Technologies für die Quantentechnologien” (Grant No.13N15911).
https://www.quantentechnologien.de/forschung/foerderung/enabling-technologies-fuer-die-quantentechnologien/hiqup.html

Thank you for your attention!

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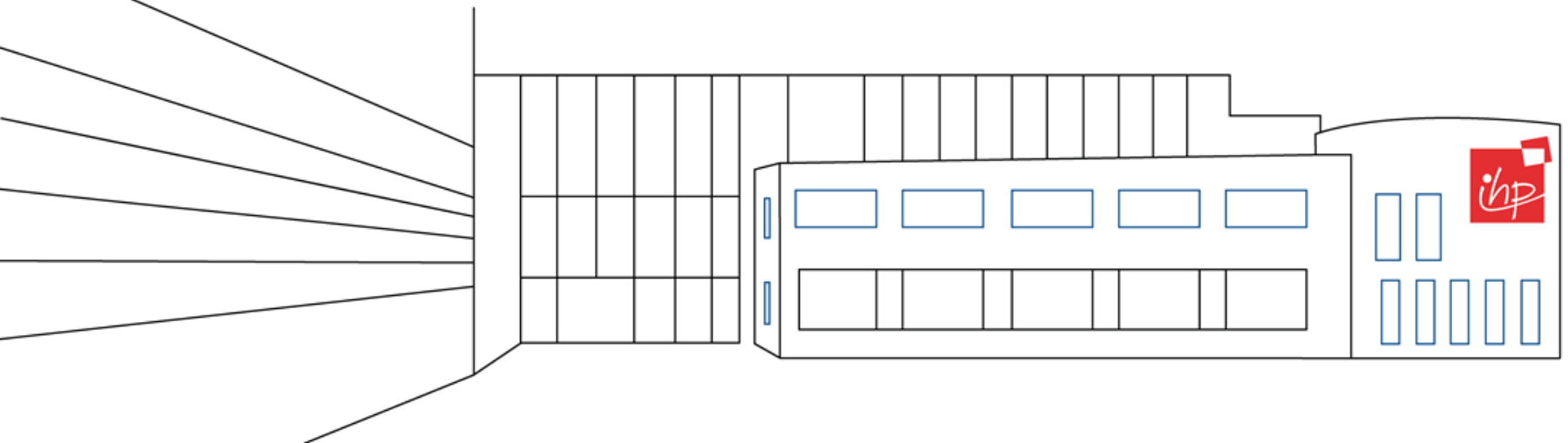

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