mmTron

Unleashing the
mmWave Frontier

mmWave PAs – Why Sacrifice High Power for Linearity?

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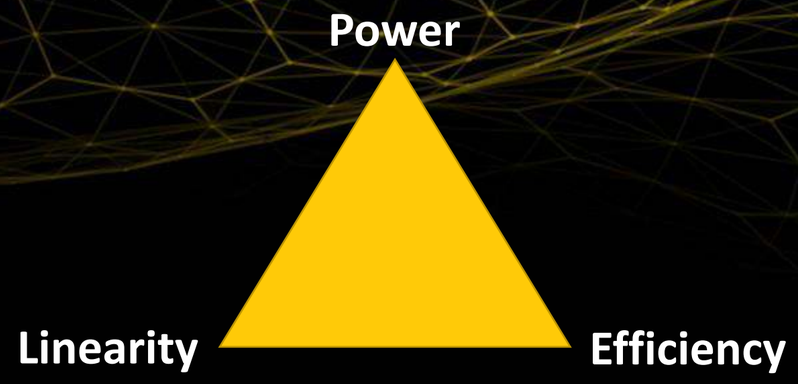


Outline

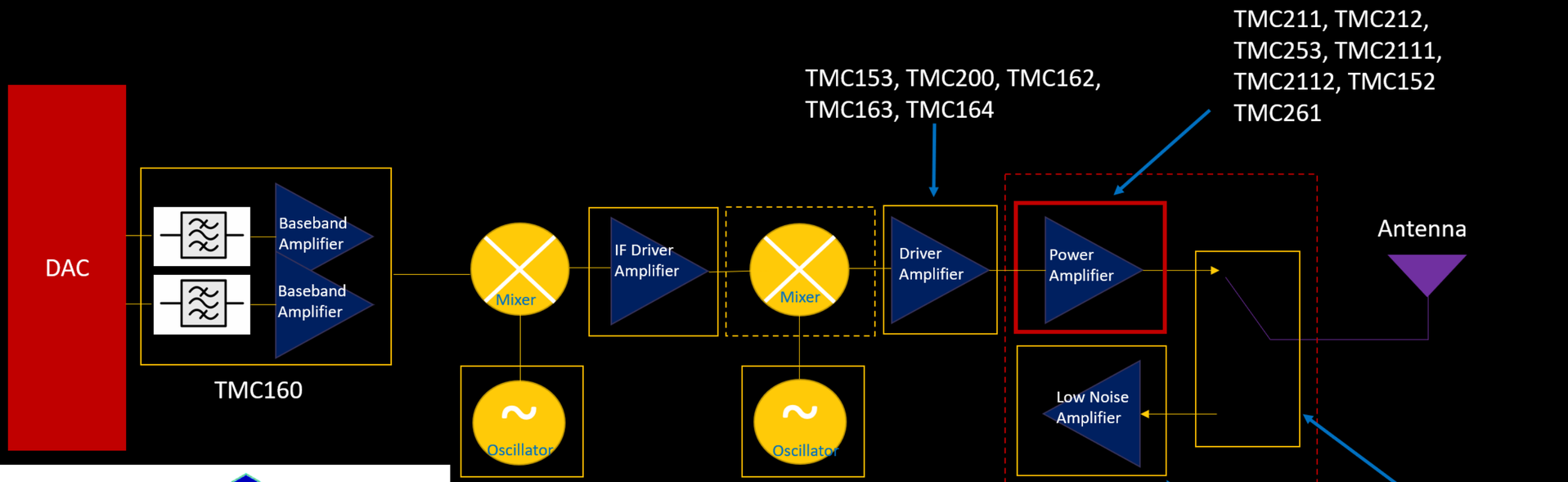
- mmTron Company Overview
- Dealing with the plethora of Linearity Specifications
- Simultaneous Power, Linearity and PAE – Challenges and Solutions
- Simulated and Measured Design Examples
- Conclusion

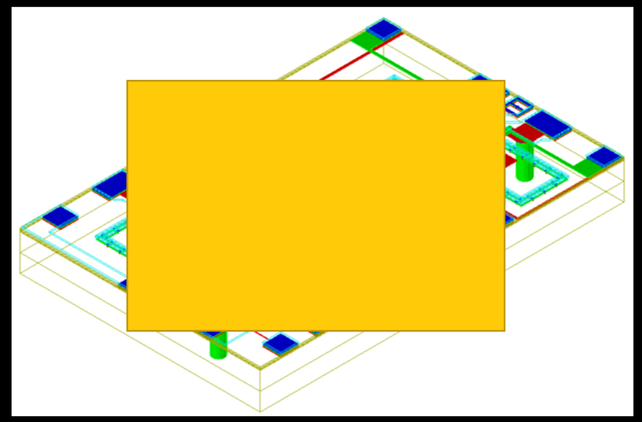
mmTron Company Overview

- We have analyzed processes, developed models, and have designed cutting-edge MMICs in most GaAs, GaN and InP processes (Qorvo, NGC, HRL, UMS, GCS, WIN, OMMIC, BAE, Raytheon, Teledyne) for more than a decade
- mmTron's chipsets deliver the highest power in the industry which enables a significantly longer range and wider reception area
- mmTron chips are ultra-linear and reduce distortion and transmit more data
- mmTron chips are super Efficient and allow more devices to be biased with limited DC power

mmTron PRODUCT Rollout

mmTron semiconductor-proven products have the highest linear power and Efficiency in mmWave





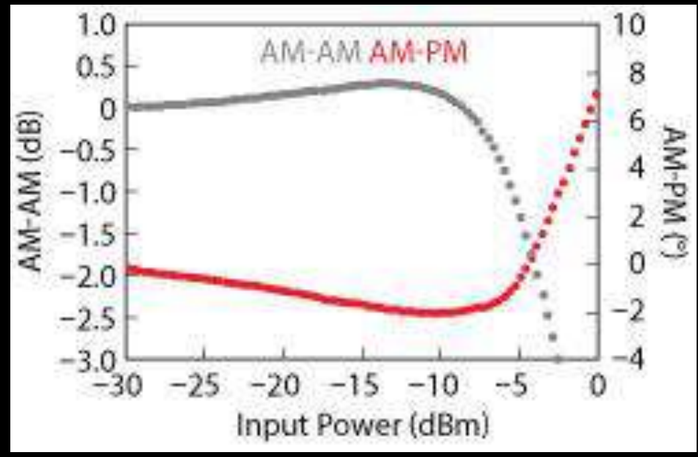
Linearity Specs – It's Complicated…

- AM / AM and AM / PM distortion are the simplest linearity measurements to make and understand
  - Both metrics are calculated from the ratio of the PA output signal to PA input signal versus input (or output) power.
  - AM / AM is the magnitude distortion while AM / PM is the phase distortion

- The bulk of power amplifier linearity can be evaluated from this simple measurement which only requires single tone measurements versus input power

- Often, the 1dB compression point (P1dB) is extracted from this measurement, as well at the point which phase deviates from small signal by a certain amount (e.g. 5 degrees)

- The shapes of the distortion curves greatly impact the ability to linearize the PA!

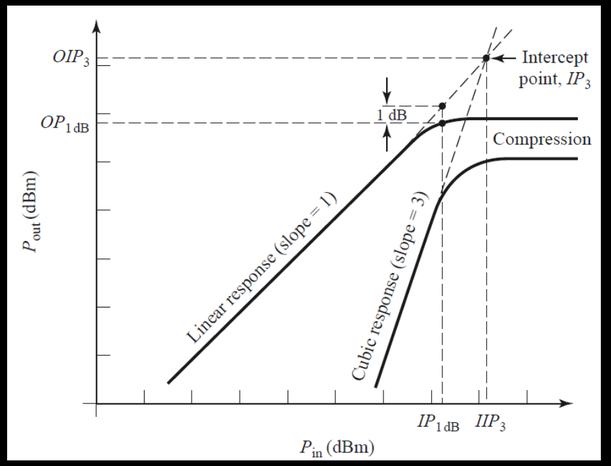


https://www.microwavejournal.com/articles/28699-predicting-evm-in-the-rfic-design-flow

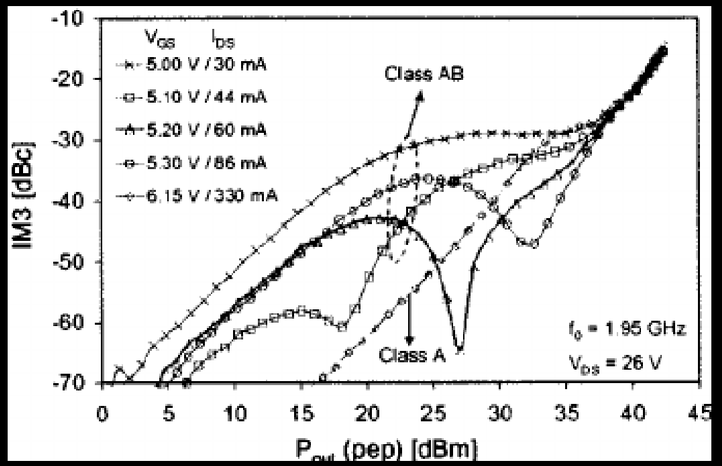
Linearity Specs – It's Complicated…

- Output Third Order Intercept Point (OIP3) is the standard for linearity characterization of a PA at high levels of backoff, with OIP3 / Pdc being an important figure of merit
  - OIP3 and OIP3 / Pdc are sensitive to PA quiescent point as well as device matching.

- For lower order modulation schemes (e.g. low PAPR signals), an IMD3 and IMD5 level (relative to the fundamental tones) required to consider the PA "linear" is typically specified (e.g. total output power at IMD3 and IMD5 less than -25 dBc)
  - OIP3 in small signal can be sacrificed to maximize the output power at this intermod level. This is typically seen in GaN PAs operating at low quiescent current density (e.g. optimized in the sweet spot)



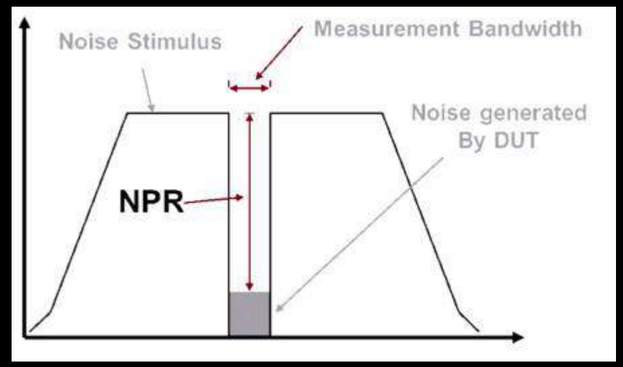
https://www.everythingrf.com/community/what-is-ip3



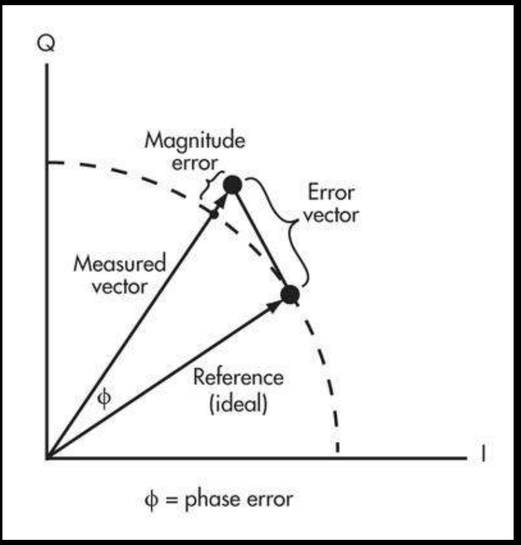
https://www.researchgate.net/figure/Measured-IM3-versus-peak-envelope-output-power-for-a-conventional-class-AB-LDMOS-power_fig5_3122090

Linearity Specs – It's Complicated…

- For higher order modulation schemes (e.g. high PAPR signals), there are two typical linearity characterization techniques
- Noise Power Ratio (NPR) is a very common technique (particularly in the satellite industry)
  - A band-limited noise-like signal is passed through a notch filter and used as the PA input. The noise-regrowth at the output of the PA is then measured relative to the noise outside the notch, defining the NPR
  - This technique is intended to mimic the system operating with a large number of carriers such that the aggregate signal is effectively noise
- Error Vector Magnitude (EVM) is also a common technique (particularly for 5G mmWave systems)
  - The magnitude of the error vector between the desired and measured signal constellation point is defines the EVM



https://militaryembedded.com/radar-ew/signal-processing/making-noise-power-ratio-measurements-with-real-world-signals



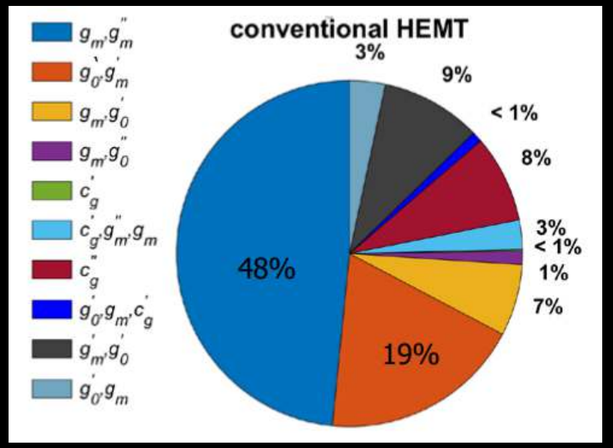
https://www.everythingrf.com/community/what-is-evm

Simultaneous Power, Linearity and PAE

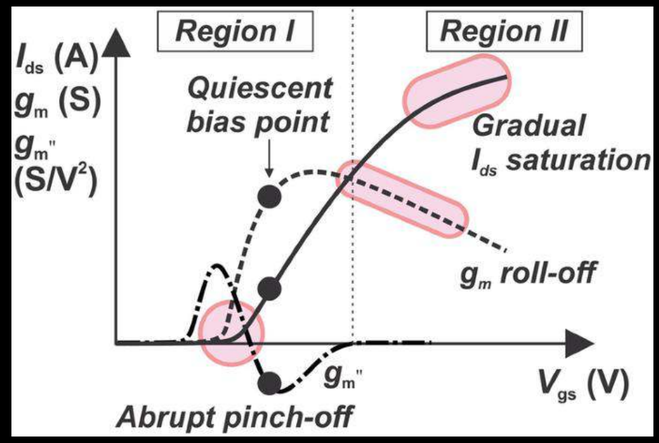
- Optimum Source and Load Match values are different for best PAE vs highest power vs best Linearity
- Adjusting transistor epi layer structure (thickness, composition, density,…), process steps, and layout configuration (gate pitch, slot via positions,…) impact power, linearity, and PAE
- A flexible device model to accurately predict power, linearity, and PAE is developed. The device model learns and improves with data from every MMIC measurement.
- Circuit topologies, in particular output and interstage matching circuits including bias circuitry play a significant role in achieving power, linearity, and PAE.

GaN Device Challenges

- The transconductance (gm) curve greatly impacts linearity
- It is well known that the linearity will be best where the second derivatives of the gm curve (gm’ and gm’’) are minimum.
- For typical devices, there are two places within the gm curve where this happens
  - 1: Low current density. This is typically referred to as the sweet spot as it is relatively sensitive. Device parameters in this region are quite sensitive to the current density. Gain is a challenge!
  - 2: At high current density near peak gm. This is typically referred to as the near class-A bias point and is quite common for small signal type designs as it maximizes OIP3. However, the higher the bias point the more DC power consumption



“High-speed Graded-channel GaN HEMTs with Linearity and Efficiency”
Jeon-sun Moon et al.



“Linearity Aspects of High Power Amplification in GaN Transistors”
Samuel James Bader et al.

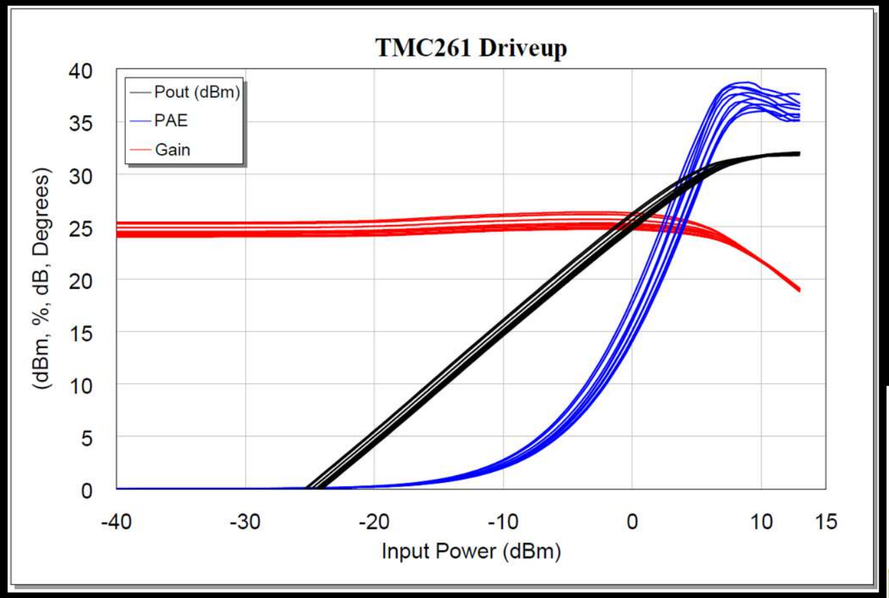
MMIC Design Challenges

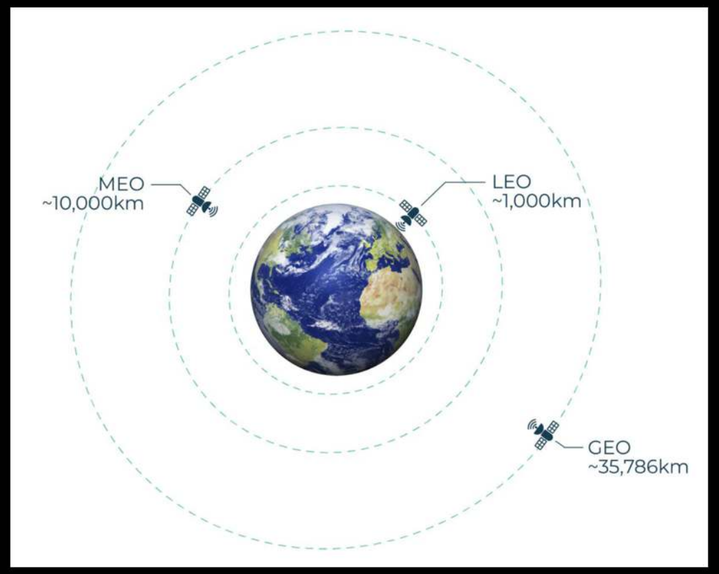
- Device gain is a challenge at mmwave in general. It's even more of a challenge if the design is centered at the "sweet spot" in the gm curve to try to optimize linearity and PAE near Psat
- For high PAPR signals, this technique does not work since the linearity under high levels of backoff is degraded!
- Higher levels of quiescent current must be used in order to maintain linearity at backoff, which can create PAE challenges
- Wide video bandwidth is a new challenge due to the modulation schemes being used in advanced systems
- A linear MMIC design requires many tradeoffs to be made to be useful at the system level

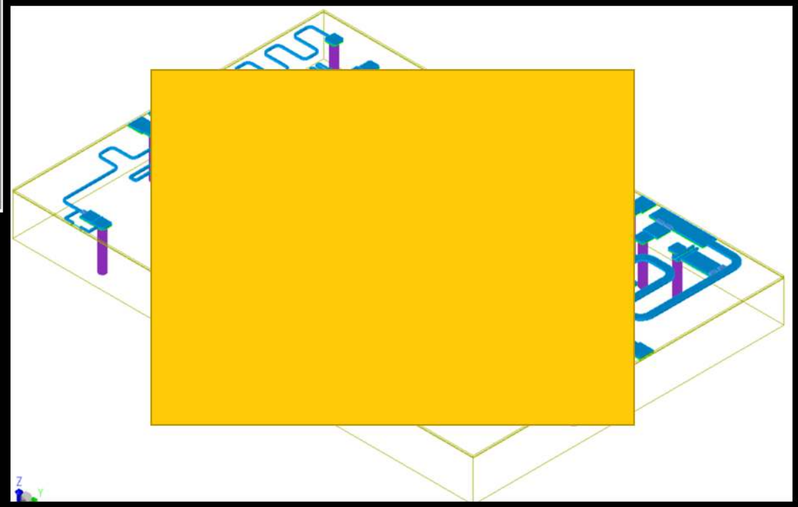
System Design Challenges

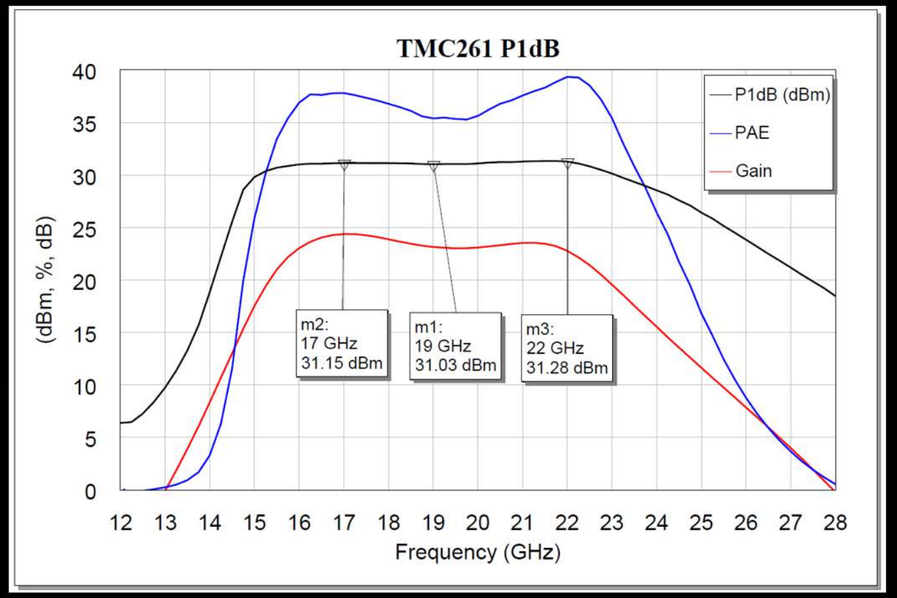
- Thermal is arguable the number one system level design challenge. If it can’t work thermally, nothing works
- GaN is a thermal challenge due to the power level and the difficulty achieving PAE at mmWave frequencies
- Packaging is also an issue, because it can degrade electrical performance and makes the thermal situation worse
- Maximizing PAE at the device and package level is critical in order to make the system level design thermally viable

Simulated Design Example: TMC261



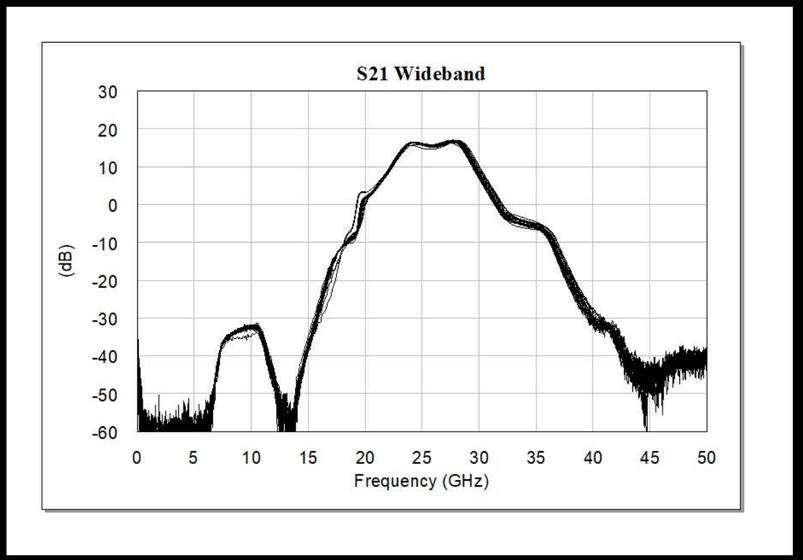


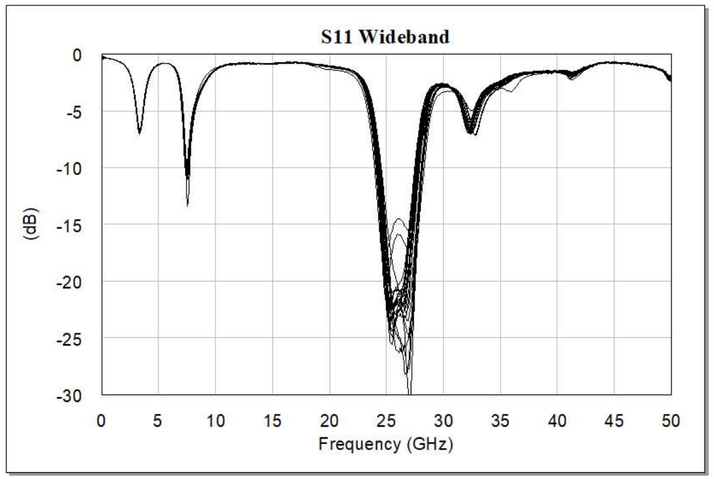


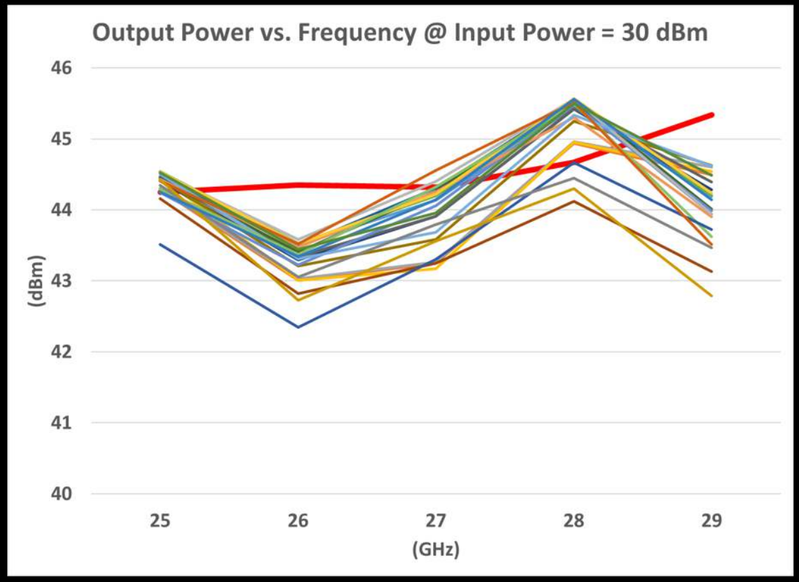


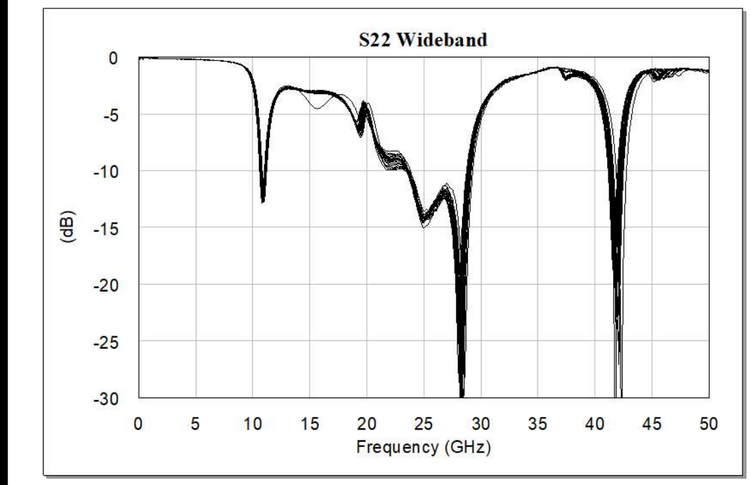
Measured Design Example: TMC2111

Electrical Performance : Vdd = 28 V, Vgg = -3.7 V, TA = 25 °C, F = 27 GHz				
	min	Typ	Max	Units
Frequency	25		29	GHz
Gain		17		dB
Return Loss		10		dB
Psat		46		dBm
PAE		28		%
Bias Voltage		28		V
Bias Current		1300		mA









Conclusion

- Achieving simultaneous Power, Efficiency and Linearity is challenging, but is a core capability of mmTron’s business
- Detailed device modeling as well as MMIC topology and design technique are key to realizing our high power, PAE and linearity products
- Please stop by our booth in the exhibition hall to learn more!

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Thank you

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