Predicting Performance of Xinger Passive Components on Customized PCB Layouts2

RF & Specialty Components Business Unit (RF&S)

TTM Technologies Inc

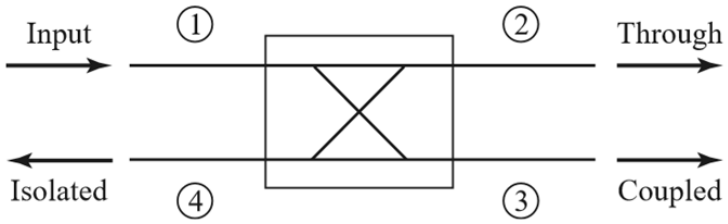
TTM Technologies

Inspiring Innovation

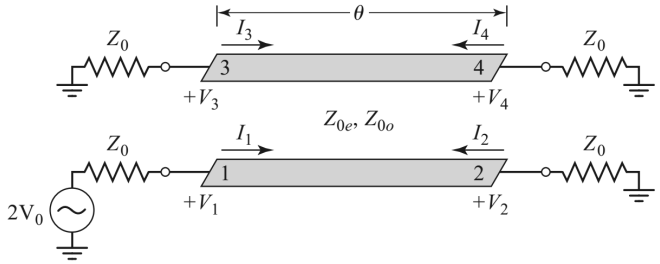
Motivation

- Predicting the performance of commercially available RF/Microwave passive components on custom PCBs is crucial in circuit/system design.
- The use of EM-Circuital simulations can normally be used for this task, especially when not following the recommended layout and PCB stack up.
- Since 3D EM models are not always available, datasheet S-parameters files are typically used as first order models. However, first order models do not account for changes in performance due to the layout or interactions with other components in close proximity.
- This MicroApp discusses recommended techniques for predicting and optimizing the performance of TTM Technologies passive components on custom PCBs by using circuital and EM simulations with both S-parameters and proprietary 3D EM models.
- Examples of performance degradation and layout optimization are presented.

Directional Couplers

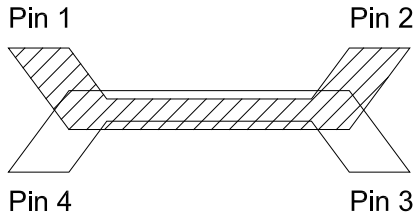


$$[S] = \begin{bmatrix} 0 & \alpha & j\beta & 0 \\ \alpha & 0 & 0 & j\beta \\ j\beta & 0 & 0 & \alpha \\ 0 & j\beta & \alpha & 0 \end{bmatrix}$$



Design Goals

- Low insertion loss
- High directivity



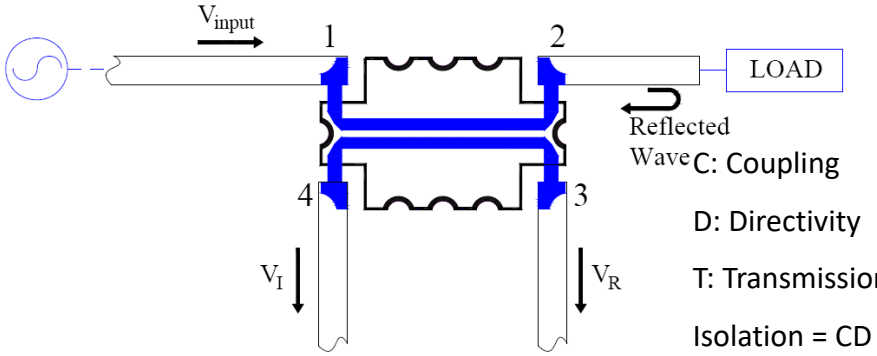
10/20/30dB Directional Coupler Pin Configuration

Pin 1	Pin 2	Pin 3	Pin 4
Input	Direct	Isolated	Coupled
Direct	Input	Coupled	Isolated

Note: For Optimum performance use Pin 1 or Pin 2 as inputs.

Directional couplers are often used in circuits that require the sampling of an arbitrary signal. A 10dB coupler can also be used to inject a correction signal into a main signal path.

Application of Directional Couplers



C: Coupling

D: Directivity

T: Transmission

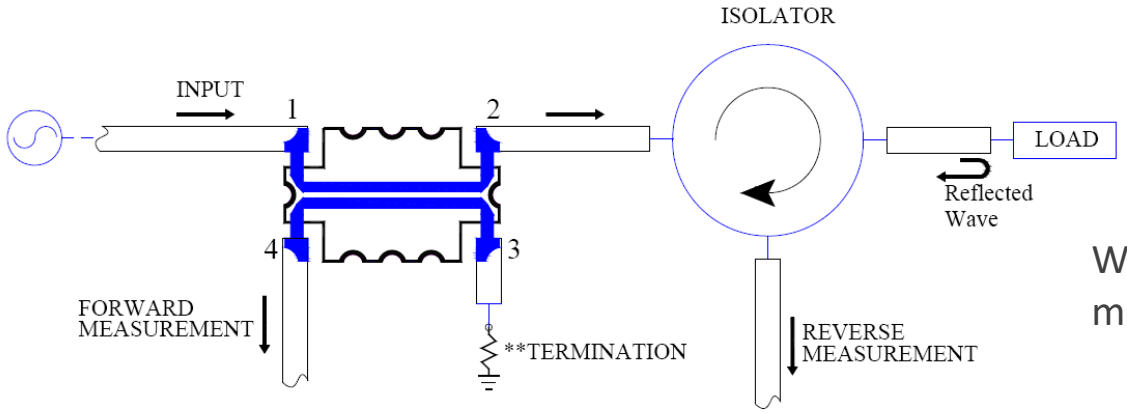
Isolation = CD

$$V_I = C + CDT\Gamma$$

$$V_R = CD + CT\Gamma$$

$$\Gamma \sim= V_R / V_I$$ When D~=0

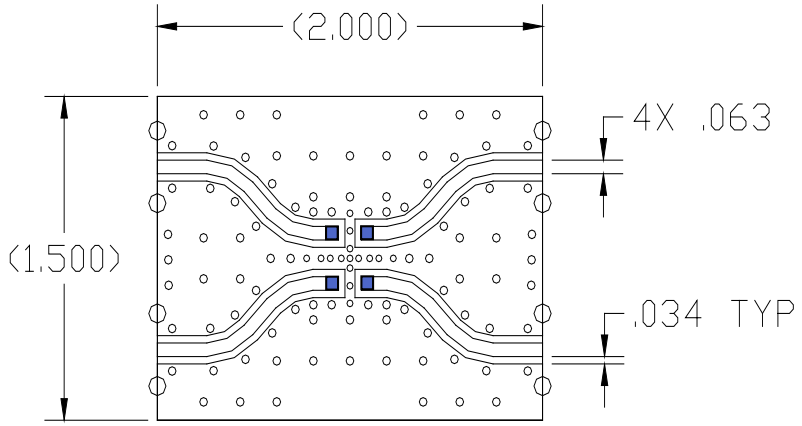
Reflectometer Circuit Schematic



When directivity can not meet requirement

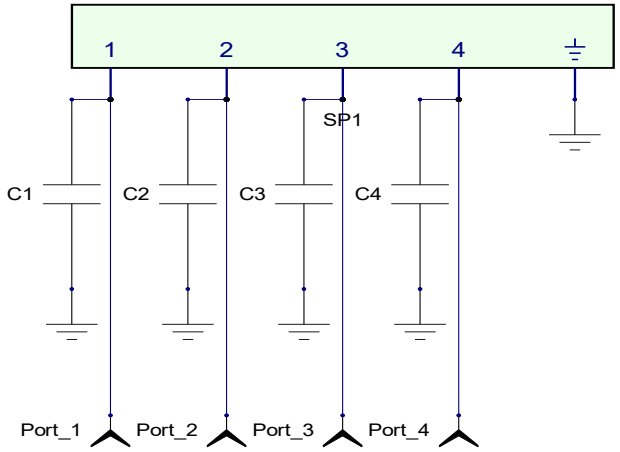
Forward and Reverse Sampling Schematic

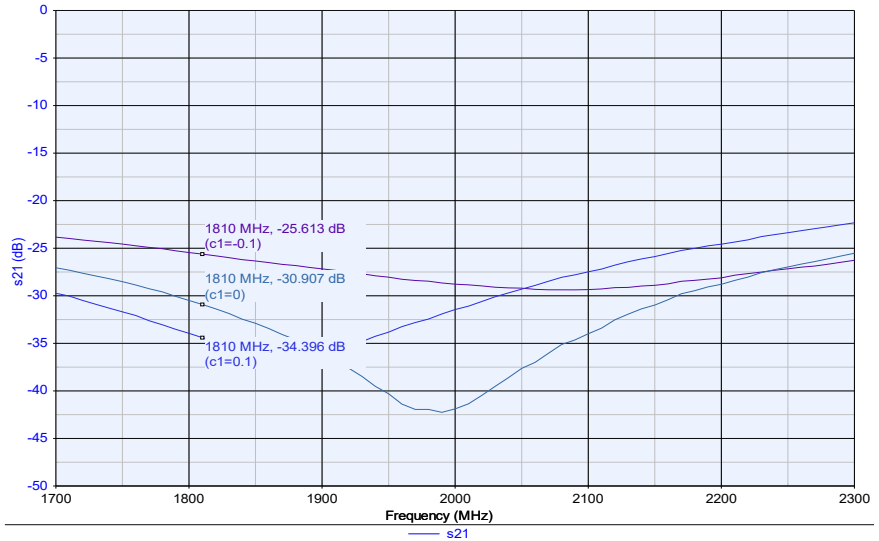
Use of Recommended PCB Layout



- The recommended Xinger III Pico size footprint on TTMs 0.030” RO4350 test board can be modeled as four 0.1pF parasitic capacitors at the coupler ports shunted to ground.
- The S-parameters of all TTM components are deembeded to the beginning of the mounting pads and the effect of the parasitic capacitors is included in the S parameter.
- When a different board material is used, similar parasitic capacitance is desired to maintain the optimized coupler performance.

Modeling Footprint Effect by Parasitic Capacitors

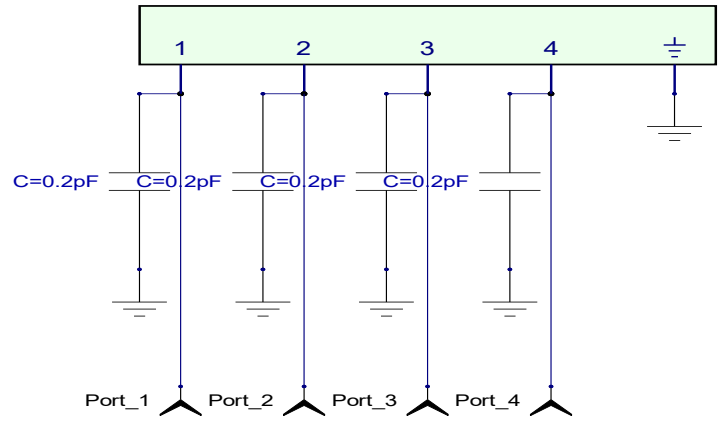


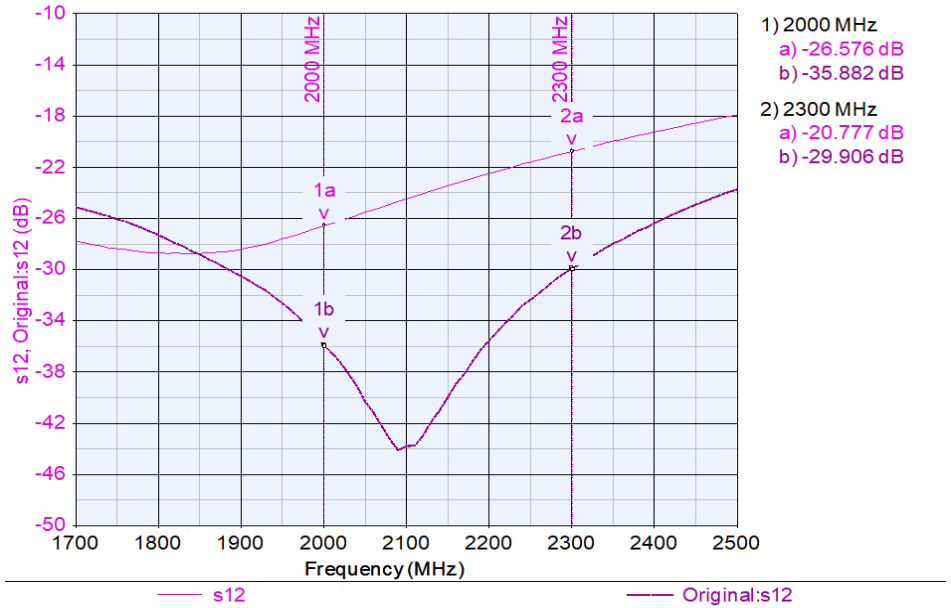


Isolation variation over the mounting footprint

Changes in the PCB Layout

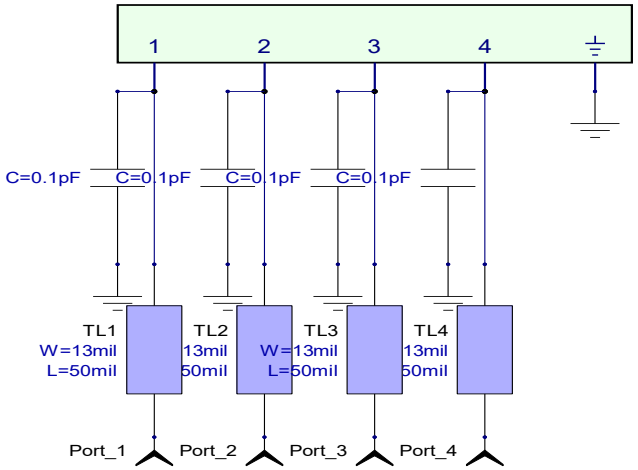
- Footprint optimization for an X3C21P1-03 coupler on 10 mil thick Rogers RO4350 (Er=3.48).
- Datasheet Pico size footprint on this board can be modeled as four 0.3pF parasitic capacitors at the coupler ports shunted to ground.
- The effect of the extra 0.2 pF parasitic capacitance can be modeled in a circuit simulation tool by loading in the S parameter file.
- If a 60X60 mil footprint is used on this board material, it can be shown that the isolation at high frequency is degraded from about 30dB to 20dB.

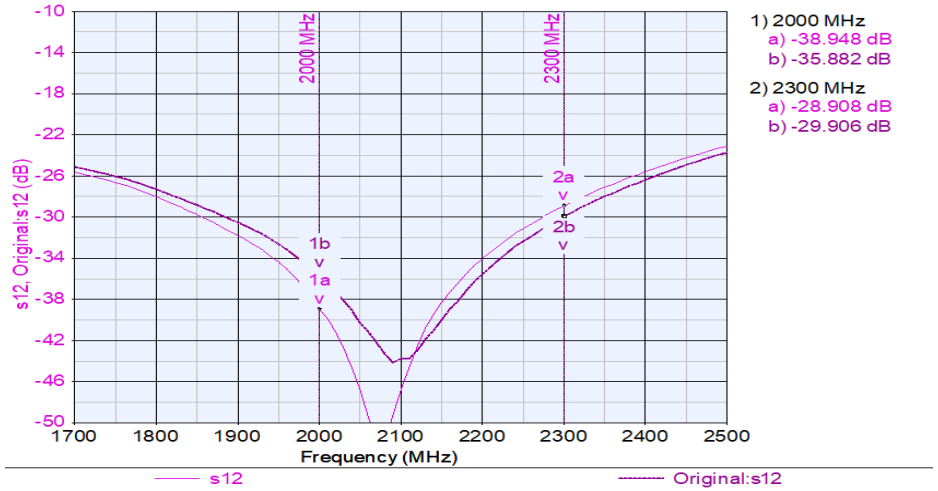




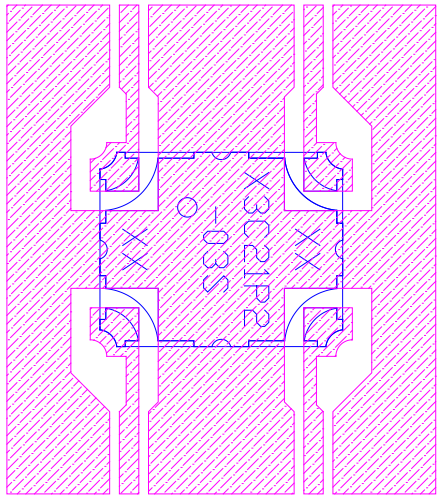
Isolation (10mil board v.s. 30mil board)

Example of Footprint Optimization: Circuital Simulations

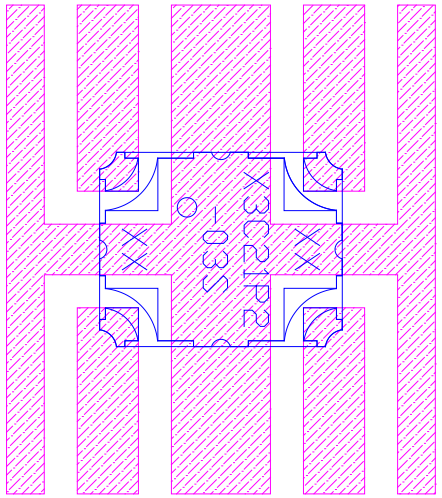




Isolation (new footprint on 10mil board vs. standard footprint on 30mil board)



Recommended footprint
for Pico on 10 mil RO4350



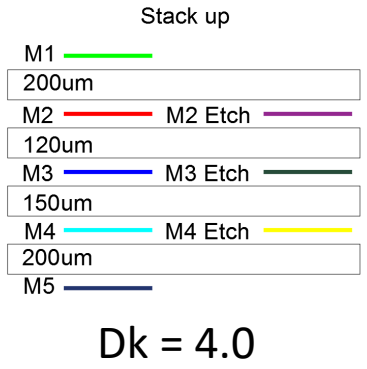
Recommended footprint
for Pico on 30 mil RO4350

Isolation performance is restored by:

1. Shrinking the mounting pads to 50X50mil thus reducing the parasitic capacitance down to 0.2pF.

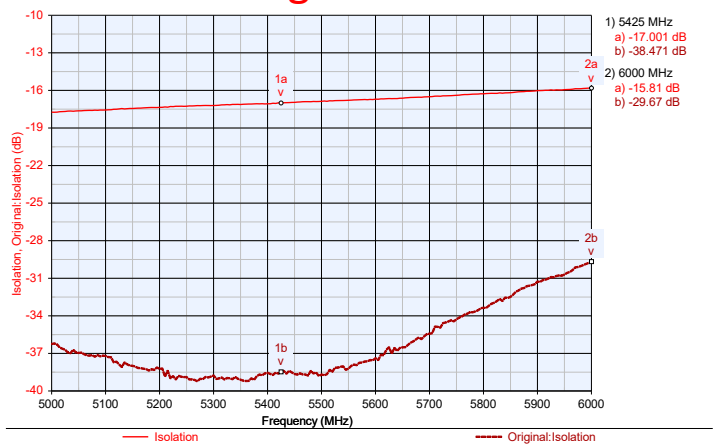
2. The extra 0.1 pF parasitic capacitance can be further compensated by a short piece of high impedance line.

Example of Footprint Optimization (1M810S Coupler)

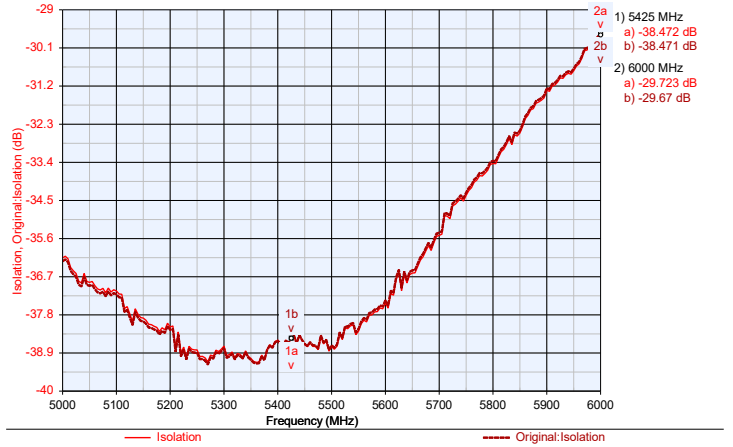


Dk = 4.0

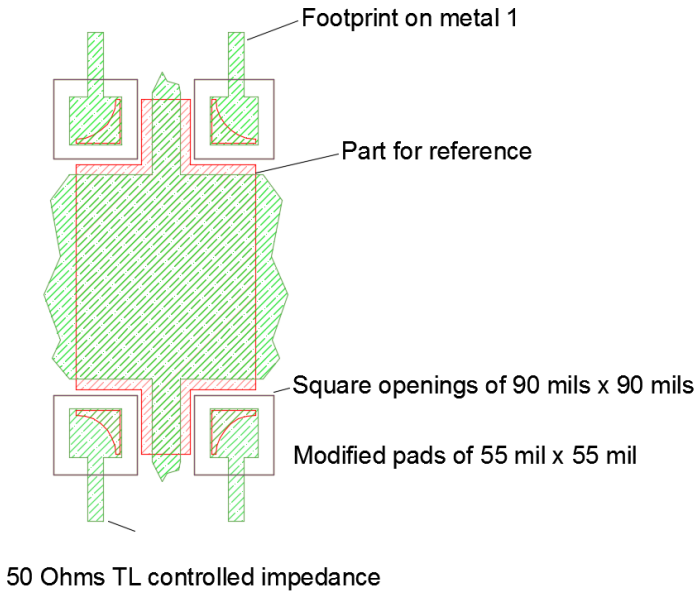
Degraded



Tuned



Isolation (new footprint on Multilayer board vs standard footprint on 30mil board)



50 Ohms TL controlled impedance

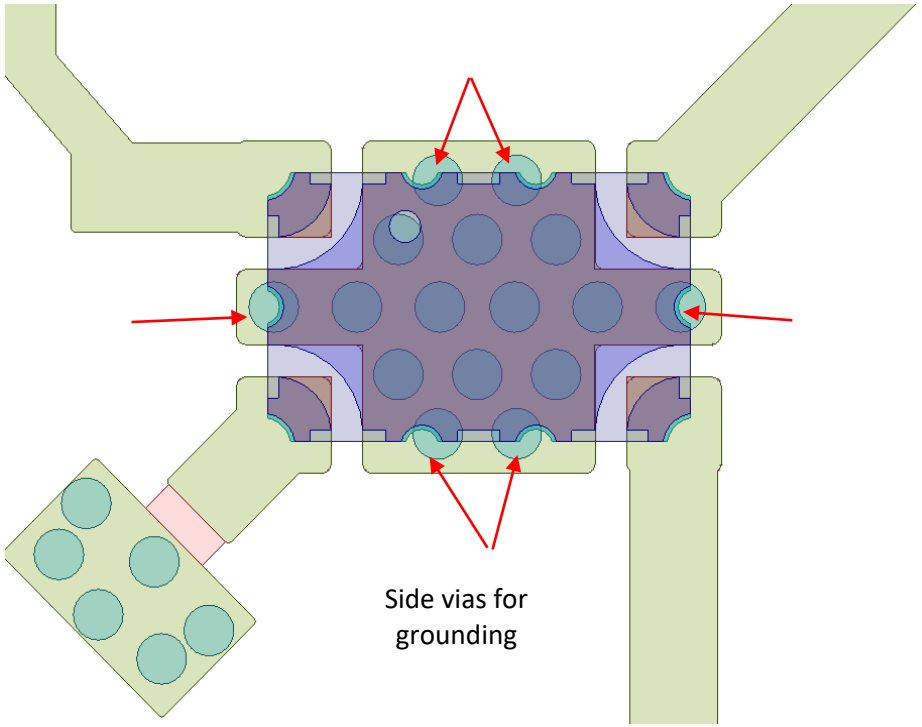
Isolation performance can be restored by:

- Creating square openings on layers M2,M3 and M4 in order to get ground reference from layer M5.
- Modifying the mounting pads to 55x55 mil.

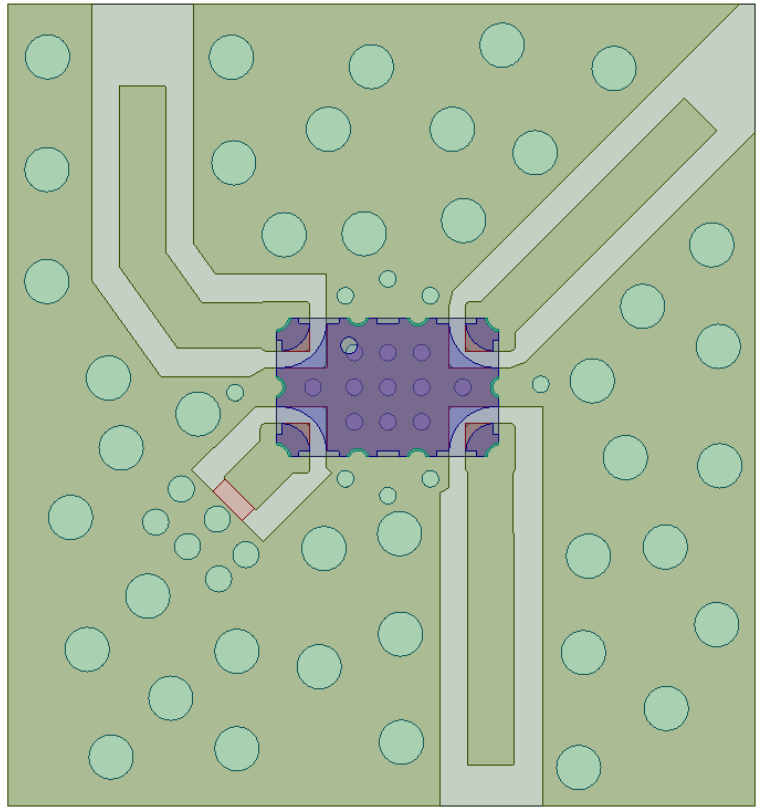
Total dielectric thickness = 0.670 mm
Pad Capacitance = 0.103pF

Example of Footprint Optimization (1M810S Coupler)

Feeding with Microstrip Lines



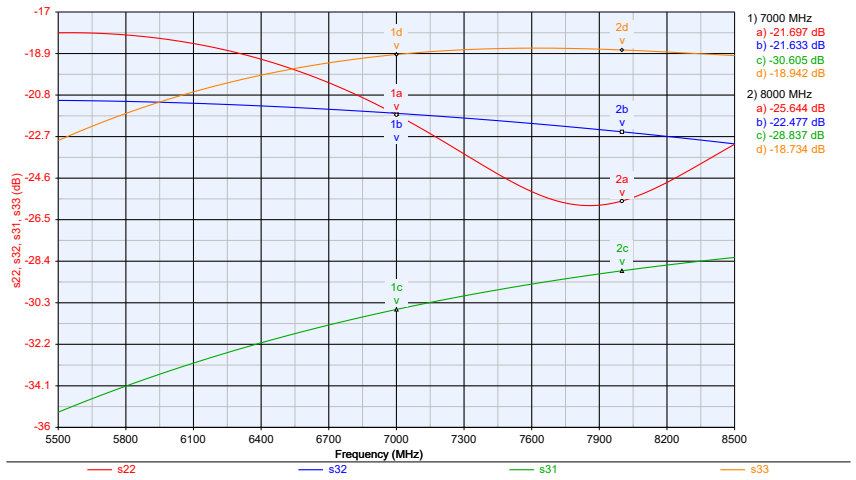
Improved Layout



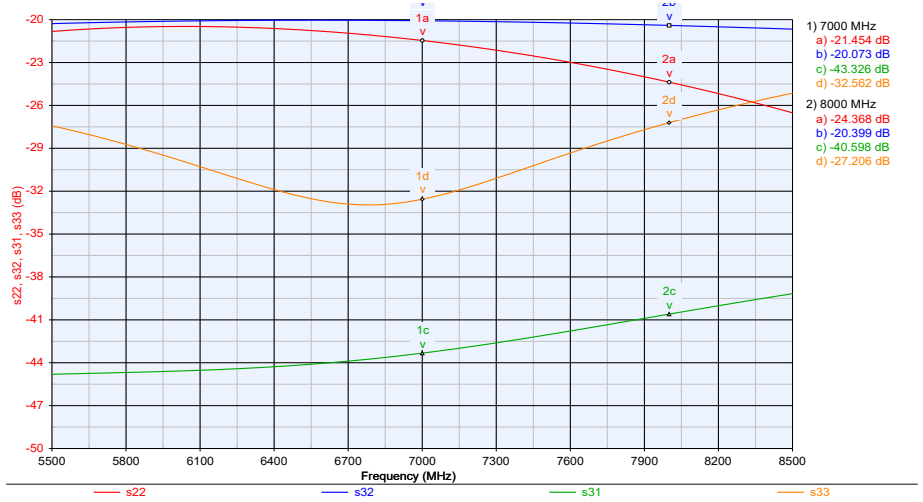
Above 5 GHz, the salient details of Microstrip and Grounded Coplanar lines, as well as the location of grounding vias, affect the isolation and coupling in Femto and smaller packages.

Footprint Optimization Results

Degraded



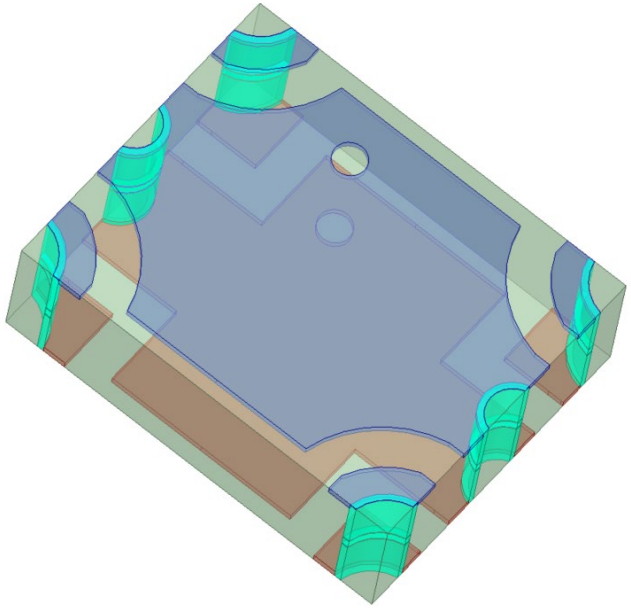
Tuned



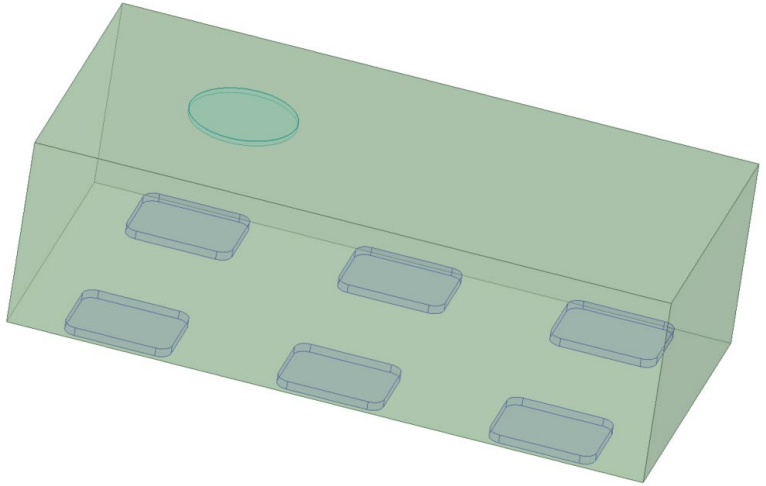
- Isolation degradation due to grounding problems and the use of microstrip lines.
- Better isolation is obtained with the use of CBCPW lines.
- Full wave 3D EM simulations are used in this case.
- A customer's test board via pattern can prevent the sidevias of the component from being properly grounded.
- When the layout and via pattern is changed to something similar to the vendor's recommended layout, the predicted performance is significantly improved.

TTM 3D EM Component Models

- To optimize PCB layout, 3D full wave EM models can be very useful.
- TTM is currently building a library 3D component models for most Xinger brand passive devices.
- Full wave simulations and co-simulations can be rapidly performed by customers with TTM assistance.

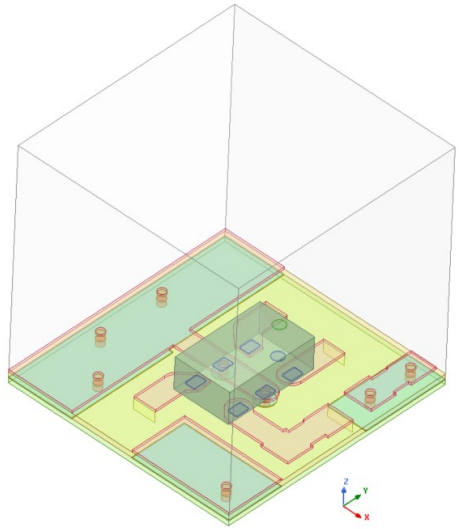


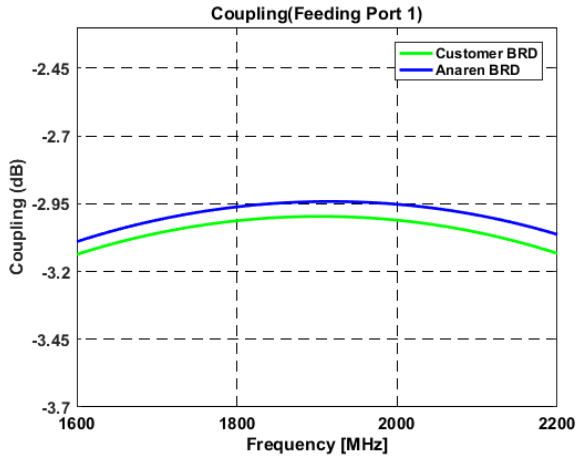
Xinger III Coupler

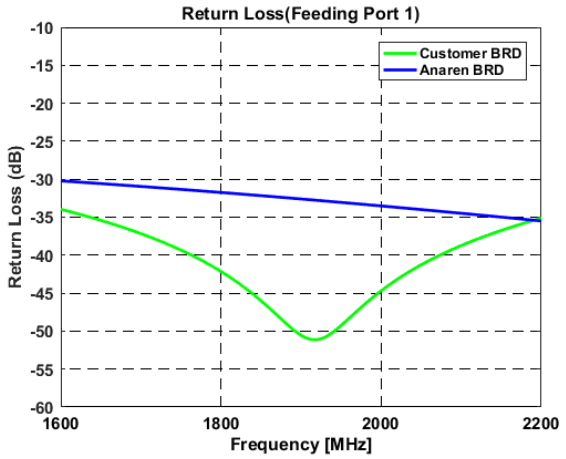


Mini Xinger Coupler

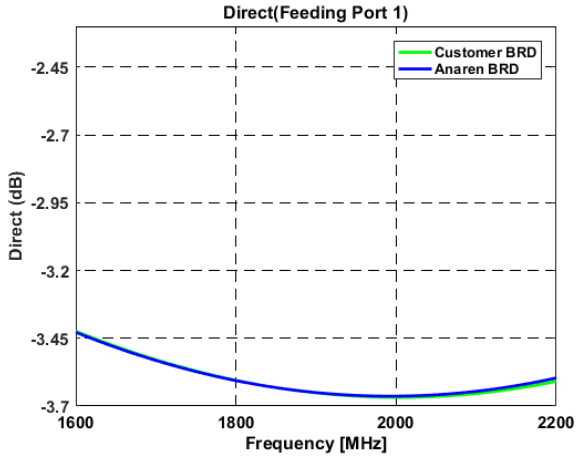
Use of TTM 3D EM Component: Mini Xinger Coupler







- No problems are found with full 3D EM simulations on customized PCB board.
- Main discrepancies are in return loss, coupling and directivity due to the different EM models of both boards.
- Performance in both cases is good for the frequency band of interest (1.7 GHz to 2.0 GHz).
- Any bad performance might be attributed to grounding problems, connectors, soldering, and few vias to ground.
- It is not recommended to place vias to ground right on the pads because this can cause soldering and proper contact problems.



Summary

- Grounding, ground via pattern, pad capacitance, feed line isolation, and close proximity with other components are main contributors to performance degradation in passive devices.
- S-Parameter files provided by vendors are good first order models to be used during circuit/system design and layout optimization.
- Pad capacitance influences the performance of passive devices. Customers need to optimize their layout in order to keep similar pad capacitance values to that provided by models.
- Quick circuital simulations allow for fast debugging of performance issues related to the mounting of the component.
- TTM will soon have 3D full wave EM component models for most of Xinger brand passive devices.
- The use of 3D EM models provide a more comprehensive and accurate design.

Thank You

Contact Information for Support

Mark Bowyer| Director Business Development – SYR-W |
1-315-278-5420 Cell | mark.bowyer@ttm.com

TTM Technologies

Inspiring Innovation