Sustainability of technology scaling by 3D Integration for 5G applications

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Outline:

• Why 3D integration?
• How to move from current arts to 3D SiP integration?
• Motivation of this work
• Challenges to 3D SiP integration
• Synthesis of technologies for 3D SiP integration
• Summary
Intro: A Typical MCM SiP

- Observe key components to integrate a typical MCM (Multi Chips Module) SiP integration.
- Varies the key components by the applications (ex: Operable frequency; Digital, RF, mm-Wave, etc.).
Intro: Key Components for SiP Integration

- Four key components for SiP integration: SiP flow, interconnect, substrate, and passive devices.
- Varies the key components by applications.
Why 3D Integration?

- Improve interconnect loss for mm-wave applications. (~λ)
- Improve PKG formfactor (X-Y-Z).
- Aggressive Integration rules (KOZ).
- Add more functions through SiP.
Motivation:

- Survey key components of SiP integration.
- Review PKG substrates.
- Define interconnects for MCM SiP integration.
- Review process variation.
- Passive devices integration.
- Consider best integration flow through key components.
- Synthesis of 3D SiP integration.
PKG Substrate: “Interposer”

- Enable “space transformer” and “fanout” through substrate.
- “Signal routings” between chip to chip through substrate.
- “Interposer” as a main role in SiP integration.

### I/O Pin-pitch P1 & P2

<table>
<thead>
<tr>
<th>#</th>
<th>Substrate</th>
<th>Material</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>L-Substrate</td>
<td>Organic material</td>
<td>Low-cost, thicker Cu-metal layers, Core/Coreless</td>
</tr>
<tr>
<td>2</td>
<td>R-Substrate</td>
<td>RDL</td>
<td>RDL BEOL, lower substrate height (vs. L-substrate)</td>
</tr>
<tr>
<td>3</td>
<td>S-Substrate</td>
<td>Silicon</td>
<td>Interposer substrate by TSV</td>
</tr>
</tbody>
</table>
Define Substrates

- Substrates for SiP integration
  - “L-Substrate”: Laminate (organic material) substrate, Core/ETS
  - “R-Substrate”: RDL (Re Distribution Layer) substrate
  - “S-Substrate”: Silicon substrate for silicon interposer
  - “H-Substrate”: Hybrid substrate (≥ 2 types of substrates in one substrate platform)
Typical Substrates:

- **L-Substrate**
  - (o) Low cost, easy to use
  - (o) Inductor integration
  - (x) Process-variation
  - (x) L/S feature-size (Coarse)

- **R-Substrate**
  - (o) L/S feature-size (Fine)
  - (o) Lower PKG height
  - (x) Lower perform inductor
  - (x) Less metal routing layers

- **S-Substrate**
  - (o) L/S feature-size (Very fine)
  - (o) Process control
  - (x) Need TSV
  - (x) BSRDL

(Note) Trend to move to RDL from L-Substrate.

(Note) Silicon interposer PKG integration
Hybrid Substrate

“Hybrid substrate” uses at least two different substrate into a single substrate platform due to the specific routing constraints.

Substrate: Process Variation (σz)

- Critical challenge to control process variation (σz) of L-Substrate due to process-flow (coarse feature-size and flow).
- Substrate’s thickness variation (≈ height) is critical to integrated passive devices for high-frequency applications.
• 2D inductor (integrated into substrate) can be varied ~5% of inductance at 10GHz.
• Process variation ($\sigma_z$ M6, $\sigma_z$ V5, $\sigma_z$ M6, and others) is caused of inductance variation.
• It is difficult to design inductor into substrate in higher frequency.
3D Inductor into Substrate: $\sigma_z$

- 3D inductor (integrated into substrate) can be varied $>15\%$ of inductance at 10GHz.
- Process variations is caused of inductance variation.
- 3D inductor is more sensitive than 2D inductor for substrate thickness variation ($\sigma_z$).
- It is difficult to design inductor into substrate in higher frequency.

<table>
<thead>
<tr>
<th>$t$</th>
<th>$L$</th>
<th>$Q$</th>
<th>$\Delta L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10um</td>
<td>1.527</td>
<td>62.328</td>
<td>+15.9</td>
</tr>
<tr>
<td>15um</td>
<td>1.317</td>
<td>61.284</td>
<td>Typ.</td>
</tr>
<tr>
<td>20um</td>
<td>1.210</td>
<td>58.595</td>
<td>-8.1%</td>
</tr>
</tbody>
</table>
LC Resonator Integration: σz

- Resonant frequencies are shifted by inductor process variation (Convert ±5% inductance variation to ±2.5% resonant frequency variation).
- Substrate thickness variation may degrade performance significantly.
Define PKG Interconnects

PKG Interconnects for SiP Integration

<table>
<thead>
<tr>
<th>#</th>
<th>Note</th>
<th>Interconnects</th>
<th>Connection</th>
<th>Types</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ZIC</td>
<td>Zero-Level Interconnect</td>
<td>Silicon to Silicon</td>
<td>Micro bumps, Cu-to-Cu HB</td>
</tr>
<tr>
<td>2</td>
<td>FIC</td>
<td>First-level Interconnect</td>
<td>Silicon to Non-silicon substrate</td>
<td>C4, Cu-pillar</td>
</tr>
<tr>
<td>3</td>
<td>SIC</td>
<td>Second-level Interconnect</td>
<td>Substrate to PCB</td>
<td>BGA, LGA</td>
</tr>
</tbody>
</table>

• Considering factors (Interconnect height, pitch, underfill material).
• To reduce parasitic component (inductance), better use advanced interconnects (smaller micro-bump or Cu-to-Cu HB).
• Pitch scaling is to increase the signal coupling between interconnects.
Signal Routing through Interconnects

Signal routing length is decreased by the specific interconnect

<table>
<thead>
<tr>
<th>#</th>
<th>Interconnect</th>
<th>Height</th>
<th>2 Pins</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C4 Solder bump</td>
<td>85um</td>
<td>170um</td>
<td>Parasitic components</td>
</tr>
<tr>
<td>2</td>
<td>Cu-Pillar</td>
<td>40um</td>
<td>80um</td>
<td>Parasitic components</td>
</tr>
<tr>
<td>3</td>
<td>Micro Bump</td>
<td>20um</td>
<td>40um</td>
<td>Parasitic components</td>
</tr>
<tr>
<td>4</td>
<td>Cu-to-Cu HB</td>
<td>5um</td>
<td>10um</td>
<td>Minimize interconnect parasitic</td>
</tr>
</tbody>
</table>
3D MCM with AiP Integration: Cu-to-Cu HB

[ A Proposed 3D AiP Integration Cross-Section ]

Antenna on PCB
Antenna on PKG Substrate
Antenna on special substrate


3D MCM with AiP Integration: TSV

- Mainly high aspect-ratio (TSV: Height/Diameter) TSV process available at Fabs.
- Low aspect-ratio TSVs are difficult to process.
- Consider of TSV density-rule.
- Consider of silicon substrate resistivity (RRS vs HRS).
- Utilize TSV bundle (ex: 4 TSVs into 1 bundle) design to meet the requirement of signal routing specifications.

Summary:

• Defined Key components of 3D SiP integration through substrate, interconnect, process-variation, and passive device integration.

• Substrate technology is evolving rapidly and may require hybrid substrate technology to fulfill the integration specifications.

• Need to aware of the process-variations ($\sigma_z$) to degrade performance through inductor integration into substrate.

• Proposed 3D MCM with AiP integration.
References