Terahertz Transceivers for Dielectric Waveguide Communication

Kenneth K. O, Shenggang Dong, Ibukun Momson, Qian Zhong, Zhiyu Chen, Zhe Chen, Pavan Yelleswarapu, Sandeep Kshattry, Navneet Sharma, Wooyeol Choi, Rashaunda Henderson

University of Texas at Dallas
Outline

• Overview
• 180-GHz transceiver
• 315-GHz transceiver
• Summary
High Data-rate Communication over a Dielectric Waveguide

- 5 frequency channels each of 45GHz bandwidth.
- Polarization diversity allows 2 channels at each frequency band.
- Up to 30-Gbps MSK data stream per channel.
Overall Transmitter Architecture

- Modulator and IF amplifier (40-GHz BW) core is common to all transmitters.
- Frequency of LO for the up-conversion mixer and output matching of mixer must be customized for each TX. LO frequencies are 45, 90, 135, 180 and 225 GHz.
- Avoid image problem without using SSB mixers.

Receiver Architecture

- Phase-Locked Loop Receiver to avoid use of I/Q demodulation of MSK.
  - Lower power consumption
  - Smaller area.
  - Carrier tracking
- Baseband amplifier chain and limiter/1-bit ADC are common to all receivers.
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Modulation Choice: MSK

- MSK is a special form of FSK which provides minimized correlation between two frequencies. It also makes a simple self-synchronized PLL-based receiver possible.
- MSK constant envelope allows reduced out-of-band emission and 0-dB PA power back-off in the transmitter.

\[ s(t) = a_i(t)\cos\left(\frac{\pi t}{2T}\right)\cos(2\pi f_c t) + a_Q(t)\sin\left(\frac{\pi t}{2T}\right)\sin(2\pi f_c t) \]

\[ s(t) = \cos\left[2\pi f_c t + b_k(t)\frac{\pi t}{2T} + \phi_k\right] \]

\[ b_k(t) = a_i(t)a_Q(t) \]

\[ \phi_k = \begin{cases} 0 & a_i(t) = 1 \\ \pi & a_i(t) = -1 \end{cases} \]

T: bit period


Cross-correlation of \(f_1\) & \(f_2\) vs \(\Delta f\) [1]
Modulation Choice: MSK

\[ s(t) = a_I(t) \cos \left( \frac{\pi t}{2T} \right) - a_Q(t) \sin \left( \frac{\pi t}{2T} \right) \]

\[ s(t) = \cos \left[ 2\pi f_c t + b_k(t) \frac{\pi t}{2T} + \phi_k \right] \]

- The objective of the demodulator is to recover \( a_I(t) \) and \( a_Q(t) \) from \( s(t) \).
- The original digital data information is contained in the phase of the carrier.
- By differentiating the phase of the carrier, we can recover \( b_k(t) \).
- By performing a sequential logic operation on \( b_k(t) \) we can recover \( a_I(t) \) and \( a_Q(t) \).
- VCO control voltage \( (v_d(t)) \) is a scaled version of \( b_k(t) \).

Self-Synchronized Receiver Architecture

80-GHz QPSK RX [1]
✓ Self-carrier-recovery
✗ DC Power and area
✗ FDMA
✗ Design complexity
✓ Compatible with QAM

120-GHz Self-mixing RX [2]
✓ Self-carrier-recovery
✗ Mixer LO requirement
✗ LNA
✓ Data Bandwidth (Gbps)
✓ One LO path

PLL based RX [3]
✓ Self-carrier-recovery
✓ Mixer LO requirement
✗ LNA
✓ Sub-THz carrier
✗ Data Bandwidth (Mbps)
✓ One LO path

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PLL-based MSK Receiver Architecture

PLL design targets

- **Type choice**
  - Type I: larger pull-out range for the same loop gain compared to Type II.

- **Loop gain**
  - 4.5-GHz for 20-Gbps MSK signal from behavioral model. Increased $K_{vco}$ (>12 GHz/V).

- **Wideband phase detector**
  - IF BW>25-GHz, double-balanced APDP, subharmonic LO.

- **Stability**
  - Sufficient phase/gain margin, behavioral model and extra zero peaking.
APDP Double Balanced Mixer

- Floating N-well APDP NMOS diode pair.
- Double balanced APDP sub-harmonic mixer removes the $\lambda/4$ stub @90GHz.
- Like an optical receiver, to counter $C_p$, the mixer is followed by a TIA to increase the bandwidth.

Conversion Gain and Noise Figure of Mixer

- Mixer down-conversion power gain is simulated with actual TIA input impedance.
- Simulated 3-dB IF bandwidth of mixer is > 25 GHz.
- Mixer SSB NF=14.7dB and TIA SSB NF=4.5dB in simulation.
Zero Peaking

Phase detector $K_{PD}$
Loop filter $H_{LF}(s)$
Inserted zero $N_z(s)$
Demodulated data

MSK signal

$K_{PD} \approx V_{RF}V_{LO}$
$K = 4.5$ GHz
Filter BW = 30 GHz
$T_d = 10$ ps

$T_d$: 1st order expansion

$H_{open2}(s) \approx \frac{H_{LF}(s)K_{PD}K_{VCO}}{s}(1 - j\omega T_d)$

Extra phase shift, deteriorating PM

Add a zero

$H'_{open2}(s) \approx \frac{H_{LF}(s)K_{PD}K_{VCO}}{s}(1 + j\omega T_{d,c})(1 - j\omega T_d)$

If $T_{d,c} = T_d$

$H'_{open2}(s) \approx \frac{H_{LF}(s)K_{PD}K_{VCO}}{s}(1 + (\omega T_d)^2)$

Zero Peaking

- Zeroes formed by inductor peaking are inserted to increase the phase margin.
- PMOS transistors are used to tune the zero location and compensate the DC offset of the in-loop amplifier chain.

LO Path: VCO

- NMOS cross-coupled pair only.
- Accumulation mode varactor.
- High $K_{VCO}$: minimize NMOS size while maintaining oscillation.
- 20-Gbps MSK demodulation requires a 5-GHz tuning range for a 90-GHz VCO.
LO Path: VCO Buffer

- With LO buffer, output power variation is <4% over the frequencies of interest.
- Neutralization transistor reduces loading capacitance for VCO to increase $K_{VCO}$.
- Minimize signal delay. There is no room for spiral inductor.

Measurement Results: Continuous Wave

Open loop bias condition

3-dB BW of open-loop CG: 150GHz~198GHz

SSB NF$_{min}$ = 18.6dB

|S$_{11}$| < -10dB from 145GHz to 220GHz
Measurement Setup

180-GHz PLL RX:

- On-chip link
- 180 GHz VCO & LO buffer & APDP in loop amps
- 50 Ω driver
- 0.95mm

180-GHz MSK TX [1]:

- 65-nm foundry CMOS.
- On-chip link is formed to measure the RX performance. TX power is backed-off during measurement.
- No external LO for the receiver.
- Wire-bonded to a PCB for testing.

180-GHz MSK Transmitter

Prior work: AWG is used for shaping signal generation and alignment [1].

\[ s(t) = a(t) \cos \left( \frac{2\pi}{T} f(t) \right) \cos 2\pi f_c t + a(t) \sin \left( \frac{2\pi}{T} f(t) \right) \sin 2\pi f_c t. \]

\[ s(t) = \cos \left[ 2\pi f_c t + b(t) \frac{\pi}{T} \phi_c \right] \]

180-GHz MSK Transmitter

PS1: 90° between CLKI/Q
PS2/3: diff phase for CLKI/Q
PS4: phase offset between CLKI/Q and I/Q DATA

Misaligned-to-aligned method to minimize phase offset between CLKI/Q and I/Q DATA[1].

PRBS-11
Jitter_{RMS}=5.6ps
Jitter_{PP}=34.9ps

10Gbps Eye, BER<1×10^{-12}

Measurement Setup

- No need for external RX LO, making the connection to RX much simpler.
- Most of the effort is for the TX phase alignment.
- Non-ideal TX (spurs & gain imbalance) causes extra difficulty for receiver.
Measurement Results

- The 10-Gbps on-chip link with BER $< 1 \times 10^{-12}$ is demonstrated.
- Compared to simulation, the highest data rate drops from 20 Gbps to 12.5 Gbps.
  - TX VCO frequency is shifted up by 3 GHz while RX VCO is shifted down by 1.5 GHz.
  - Reduction of receiver open-loop conversion gain and bandwidth.

Sensitivity:
- 6Gbps, BER$<1 \times 10^{-12}$: 735mV*
- 10Gbps, BER$<1 \times 10^{-12}$: 100mV
- 12.5Gbps, BER$<1 \times 10^{-4}$: 120mV

*Add external 50Ω driver

Simulated eye: 20Gbps

## Comparison with State-of-the-art Coherent Receivers

<table>
<thead>
<tr>
<th></th>
<th>JSSC 2016</th>
<th>CICC 2007</th>
<th>JSSC 2016</th>
<th>ESSCIRC 2016</th>
<th>JSSC 2011</th>
<th>ISSCC 2017</th>
<th><strong>This Work</strong></th>
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<tbody>
<tr>
<td>(f_c) (GHz)</td>
<td>240</td>
<td>60</td>
<td>120</td>
<td>120</td>
<td>87</td>
<td>2.4</td>
<td>180</td>
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<td>I/Q mixer</td>
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<td>17.7</td>
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<td>0.002</td>
<td>10 (^b)</td>
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<td>Sensitivity (dBm)</td>
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<td>-70</td>
<td>-32.5</td>
<td>-12.6</td>
<td>-</td>
<td>-87</td>
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<tr>
<td>BER</td>
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<td>(&lt;10^{-12})</td>
<td>(&lt;10^{-12})</td>
<td>(&lt;10^{-11})</td>
<td>-</td>
<td>(&lt;10^{-12})</td>
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<td>130nm SiGe</td>
<td>40nm CMOS</td>
<td>40nm CMOS</td>
<td>65nm CMOS</td>
<td>40nm CMOS</td>
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<tr>
<td>(P_{DC}) (mW)</td>
<td>260</td>
<td>32.4</td>
<td>89.2(^a)</td>
<td>59.6(^a)</td>
<td>166</td>
<td>1.55</td>
<td>126(^c/160)</td>
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<td>Energy/Bit (pJ/bit)</td>
<td>16</td>
<td>16.2</td>
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<td>3.37</td>
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<td>No</td>
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<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

- \(^a\) Includes 50-Ohm driver
- \(^b\) Characterized using on chip MSK transmitter
- \(^c\) Excludes 50-Ohm driver

**Self-synced coherent RX:** highest \(f_c\) when published.

**MSK RX:** Data Rate improved by 50%

**PLL RX:** Data rate \(\times 100^+\)

**BER:** state-of-the-art 65-nm CMOS

Amplifier chain is over-designed for 20 Gbps.

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\(<WME-4>\)
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300-GHz QPSK mode transmitter

315-GHz MSK Transmitter

- 135-GHz quadrature carrier generated by QVCO.
- 135-GHz MSK up converted to 315-GHz using integrated 180-GHz LO.
- Extension of previously reported 300-GHz multimode QPSK transmitter.
- Up to –11-dBm single-tone RF output power at 315-GHz.

315-GHz MSK Receiver

- PLL-based self-synchronizing MSK receiver.
- 78.75-GHz fundamental VCO.
- In-loop doubler and 2nd harmonic mixer for 315-GHz down-conversion.

315-GHz MSK Receiver

- Only input signal to RX is 315-GHz MSK modulated RF.
- No separate carrier recovery or external LO synchronization between TX and RX.

157.5-GHz LO chain

- 78.75 GHz VCO output doubled to 157.5 GHz.
- ~0.5 V simulated LO swing @ 157.5 GHz (node D).
- ~18 ps response time from Vctrl to node D.
315-GHz 2nd Harmonic Mixer

- 315-GHz 2nd harmonic APDP.
- 17.5-dB CL, 13.5-dB SSB NF, 15-GHz IF bandwidth (30-GHz RF bandwidth).
- CG includes RF probe pad, balun and transmission lines with TIA as mixer load.
315-GHz MSK RX Continuous Wave Measurements

- VCO tuning range.
- Closed-loop lock-in range.
- Open-loop conversion gain (CG) and noise figure (NF).
315-GHz MSK RX Continuous Wave Measurements

- 76.5–80.9 GHz VCO tuning over 0.6 V control (306–323.6 GHz RF).
- ~8 GHz/V VCO gain at 78.75 GHz.
- Open loop CG is 14 dB less than simulated, NF is 3 dB greater than simulated.
- Estimated ~11 dB gain reduction from 8-stage baseband amplifier chain.
- 6.8-GHz closed loop RF lock-in range (311.6–318.4 GHz) with –21-dBm RF input.
- 6.8-GHz lock-in range can support up to 13-Gbps MSK.
• 315-GHz MSK TX and RX integrated on the same die.
• TX and RX connected by RF on-chip transmission line.

• 10-Gbps on-chip link with BER < 10^{-11} at RX output.
• –21-dBm RF input power to RX.
• RX DC power: 195 mW (Baseband amp: 155 mW, VCO: 28 mW, Doubler: 12 mW).

315-GHz MSK Receiver Performance Summary

Performance comparison with state-of-the-art millimeter wave self-synchronizing coherent receivers

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<td>Data Rate (Gbps)</td>
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<td>Sensitivity (dBm)</td>
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<td>-32.5</td>
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<td>&lt;10^{-12}</td>
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<td>Data Pattern</td>
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- Room for improvement in receiver sensitivity.
Summary

• Use of MSK modulation enables
  – Improvement of power efficiency due to its constant envelope property
  – Improvement of bandwidth efficiency
  – Attenuation of out of band emission to relax filtering requirements
  – Implementation of compact and power efficient frequency tracking receivers.

• 180-GHz and 315-GHz MSK transceivers are demonstrated.
• Possible to implement transceivers for the other bands in CMOS.
• Biggest challenge is not having an MSK signal generator and a demodulator that can support the receiver and transmitter testing.
• Integrate them for dual band operation.
• Demonstrate FDMA and PDMA operation.
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