THz/sub-THz Interconnect, Complement to Electrical and Optical Interconnects

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Continuous Datasphere Expansion and Challenges

Data Age 2025: The Evolution of Data to Life-Critical, IDC 2017


Continuous datasphere expansion challenges sustainable advancements in datalinks
Key Metrics of Interconnect

To support sustainable data rate increasing, all the above metrics should be advanced correspondingly.
BW Density / Energy Efficiency

FOM drops exponentially vs link distance

Big gap around meter range, where both EI and OI face great challenges!

Fiber extraordinary performance desensitize link distance

Sources: DARPA PIPES program
Electrical Media Channel Attenuation

A typical electric channel loss profile

The attenuation constant increasing with signal bandwidth constrains the maximum reachable distance

\[ SNR = S - N - \alpha \times BW \times L - 10 \log(BW) \]

The key is to use channels with frequency insensitive attenuation constant.
**Frequency Insensitive Attenuation Media**

- **Dielectric waveguide** is a great medium to have frequency insensitive low attenuation constant. Optic fiber is a great example at optical frequencies.

\[ SNR = S - N - \alpha \times L - 10 \log(BW) \]

**Data Bandwidth vs. Distance**

- To reach 10 meter with > 1GHz, attenuation constant needs to be < ~ 10 dB/m
- To reach 1 meter with > 1GHz, attenuation constant can be up to 70 dB/m

**Remarkable observations**
- With 5 dB/m for 10 meters, signal bandwidth can reach 280 GHz
- With 10 dB/m for 1 meter, signal bandwidth can reach \(2.5 \times 10^6\) GHz
- With 30 dB/m for 1 meter, signal bandwidth can reach \(2.5 \times 10^4\) GHz

Compared with the theoretical capabilities, what has our society achieved?

Assume: Pout=0dBm, NF=10 dB, SNR=0dB
**DWG Link State-of-the-Arts**

- 105 Gbps up to 0.3m
- 220-to-335GHz Signal freq.


- 36 Gbps up to 1m
- 130 GHz Carrier freq.

M. Sawaby et. al., “A Fully Packaged 130-GHz QPSK Transmitter With an Integrated PRBS Generator,” IEEE SSC-L, 2018

- 18 Gbps with 1m
- 7.6 Gbps with 8m
- 120 GHz Carrier freq.


Recall: with 30 dB/m attn. constant, signal BW can reach $2.5 \times 10^4$ GHz theoretically for 1 meter

**What are the caveats in the theoretical analysis?**
Caveat-1: higher BW requires higher carrier frequency with degraded performance

- Higher BW requires higher carrier frequency
- Circuit/system performances degrade with higher frequencies

\[ C = \Delta f \times \log_2 (1 + 10^{\frac{S(f) - N(f) - \alpha L - 10 \log(\Delta f)}{10}}) \]

\[ P_{out} \propto \frac{1}{f^2} \quad NF \propto f^2 \]

Assume: Pout=0dBm and NF=10 dB at 100 GHz, 1 meter link distance, 10% fractional bandwidth

- Active circuit performances at higher frequencies are important.
- Smaller attenuation constant leads to higher optimum carrier frequency, thus larger capacity.

Even after considering the carrier frequency effect, we still do not see 100 Gbps over 1 meter. Why?
Caveat-2: Dispersion is another devil

Supportable signal BW due to channel loss

$$\Delta f = 10 \times \frac{S-N-SNR-\alpha L}{10}$$

Supportable signal BW due to channel dispersion

$$\Delta f = \sqrt{\frac{1}{D_0 \lambda^2 L 10^{-20}}}$$

Within short reaches, up to a few meters, the supportable maximum bandwidth is limited by dispersion.

Q. Jane Gu, “Sub-THz/THz Interconnect, Complement to Electrical and Optical Interconnects,” Fall 2020 IEEE Solid-State Circuits Magazine
Dispersion Types and Mitigation Techniques

- Material dispersion
- Modal dispersion of waveguides

\[ \beta = k_1 \sqrt{1 - \left(\frac{\omega_c}{\omega}\right)^2} \]

- Device and circuit bandwidth limitation
  - Active device finite speed
  - Circuit time constant

- Dispersion suppression in electrical domain
  - Feedforward and decision feedback equalizations
  - Filters, predistortion, pulse shaping
  - Pros: Agile and flexible;
    Cons: high power consumption for high speed signal processing

- Optical dispersion compensation approaches
  - Dispersion-compensation fiber with opposite group delay profile structures
  - Use zero-dispersion wavelength
  - Pros: passive implementation, low power consumption;
    Cons: limited tunability
Outline

• Interconnect Gap and Current Approaches
• New Approach: THz Interconnect
• THz Interconnect Channel for Planar Silicon Technologies
  • Far Field Coupling Channel
  • Near Field Coupling Channel
  • Ortho-mode Channel
• THz Interconnect Active Circuits and Systems
• Conclusions
Interconnect Gap

Big Data Era: Increasing gap between I/O bandwidth requirements and limited I/O pin numbers for Chip-to-Chip communications.

- Off-chip I/O bandwidth: 10X / 5 years
- I/O Pin numbers: 1.7X / 5 years

Demand increasing growth of bandwidth density and energy efficiency
Current Interconnects

Electrical Interconnect

- Low cost due to mature processing
- Scalable friendly with process development
  - Lossy channels with high data rate and operating speed
  - Limited channel bandwidth

Optical Interconnect

- Wide bandwidth
- Low loss optical fibers or waveguides
  - Complicated integration processing with higher cost
  - Sensitive to environmental changes

Both Electrical and Optical Interconnects face challenges to completely address the interconnect issues separately.
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New Approach: THz Interconnect

Leverage THz unique spectrum position to combine the advantages of both electrical and optical interconnects.

THz Interconnect complement OI and EI to address the meter range interconnect challenge.

New Approach: THz Interconnect

Potential Advantages of THz Interconnect

- Based on mainstream processes, therefore scale with electronic devices to support wide bandwidth for high data rate with **low cost and high reliability**
- Leverage low loss channels similar to the optical fibers to alleviate link budget for **high energy efficiency**
- Leverage small size of the channel for **high bandwidth density**
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THz Interconnect Channel

The key requirements:

- Low loss
- Compact
- Wide bandwidth
- Compatible with planar silicon processes
- Allow batch processing

High resistivity silicon based dielectric waveguide Channels

- Low material loss
- Large permittivity
- Low channel cutoff frequency
- Same material with silicon technologies
Far Field Coupling Channel

- Channel Design Requirements
  - Low loss
  - Bending structures for planar intra-/inter- chip coupling
- Channel Coupler Design
  - Compatible with silicon processes
  - High coupling efficiency

Patch based Channel Coupler

Transition Loss: 0.14 dB each
Microstrip Loss: 0.39 dB/mm

Directivity = 7.43 dBi
Efficiency= 61.5% = -2.14 dB
Far Field Coupling Channel

-8.4 dB minimum insertion loss
-3dB bandwidth of 12.6 GHz

Near Field Coupling Channel

Tapered DWG and MSL overlap each other to let EM waves transit smoothly.

Sub-THz Interconnect
Transition

Impedance Matching

MSL
DWG

Sub T=100\,\mu m
Freq = 160\,GHz

DWG H=500\,\mu m
Freq = 160\,GHz

0 50 100 150 200
50 100 150 200

Re\{Z_0\} (\Omega)
Width (\mu m)

-1.5
-1.0
-0.5
0.0

Im\{Z_0\} (\Omega)

MSL
50\Omega \leftrightarrow 218\,\mu m
120\Omega \leftrightarrow 20\,\mu m

DWG
45\Omega \leftrightarrow 30\,\mu m
133\Omega \leftrightarrow 450\,\mu m

<WME-6/THz/sub-THz Interconnect, Complement to Electrical and Optical Interconnects>
Near Field Coupling Channel

The measured insertion loss is 4.0 dB with 59 GHz 3-dB bandwidth

Orthomode Channel

- Share physical channel to boost bandwidth density
- Alleviate the bandwidth requirement for each logic channel to reduce dispersion effect

\[ P_{2+} \pm P_{2-} = P_{1+} \pm P_{1-} \]

\[ E_{y_{11}} \]

\[ E_{x_{11}} \]
Orthomode Channel

- Planar rectangular Rat-Race balun for differential to single-ended signal conversion
- Backside trench to reduce the wave leakage into the substrate
- Overpass trace for signal routing

B. Yu, Y. Ye, X. Ding, Y. Liu, Z. Xu, X. Liu, and Q. J. Gu, "Ortho-Mode Sub-THz Interconnect Channel for Planar Chip-to-chip Communications", TMTT 2017
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THz Oscillator

How to choose the transistor size?

\[ F_{\text{OM}} = \eta_A \cdot P_{\text{out,A}} \]

\[ F_{\text{OM,OSC}} = F_{\text{OM}} \cdot (IL_{\text{min}})^2 \]

\[ IL_{\text{min}}(\text{dB}) \approx -10\log\left(1 - \frac{2}{kQ_T}\right) \]

Lower coupling coefficient \( k \) leads to higher impedance boosting index however with higher minimum insertion loss.

Y. Ye, B. Yu, and Q. J. Gu, “A 165 GHz Transmitter with 10.6% Peak DC-to-RF Efficiency and 0.68 pJ/bit Energy Efficiency on 65 nm Bulk CMOS,” TMTT 2016
THz Oscillator Measurement Results

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Process</th>
<th>Center Frequency (GHz)</th>
<th>Output Power (dBm)</th>
<th>DC Power Consumption (mW)</th>
<th>DC-to-RF Efficiency (%)</th>
<th>No. of Harmonic</th>
<th>Phase Noise (dBc/Hz)</th>
<th>Chip Size (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>JSSC'11</td>
<td>130nm CMOS</td>
<td>121</td>
<td>-3.5</td>
<td>21.6</td>
<td>2</td>
<td>Fund.</td>
<td>-88 @1MHz</td>
<td>0.135</td>
</tr>
<tr>
<td>JSSC'11</td>
<td>130nm CMOS</td>
<td>104</td>
<td>-2.7</td>
<td>28</td>
<td>1.9</td>
<td>Fund.</td>
<td>-93.3 @1MHz</td>
<td>0.16</td>
</tr>
<tr>
<td>JSSC'13</td>
<td>120nm SiGe HBT</td>
<td>232</td>
<td>-3.6</td>
<td>54</td>
<td>0.8</td>
<td>Fund.</td>
<td>-98 @10MHz</td>
<td>N/A</td>
</tr>
<tr>
<td>TMTT'13</td>
<td>32 nm CMOS</td>
<td>240</td>
<td>-7</td>
<td>13.3</td>
<td>1.5</td>
<td>Fund.</td>
<td>-93 @10MHz</td>
<td>0.0552</td>
</tr>
<tr>
<td>JSSC'14</td>
<td>32nm CMOS SOI</td>
<td>208.7</td>
<td>-13.5</td>
<td>42</td>
<td>0.1</td>
<td>Fund.</td>
<td>-81 @1MHz</td>
<td>0.04*</td>
</tr>
<tr>
<td>IMS'15</td>
<td>65nm CMOS</td>
<td>213</td>
<td>-1.6</td>
<td>43.2</td>
<td>2.1</td>
<td>2nd</td>
<td>-66 @1MHz</td>
<td>0.0625</td>
</tr>
<tr>
<td>ISSCC'14</td>
<td>65nm CMOS</td>
<td>256</td>
<td>4.1</td>
<td>227</td>
<td>1.14</td>
<td>2nd</td>
<td>-94 @1MHz</td>
<td>0.4355</td>
</tr>
<tr>
<td>TTST'13</td>
<td>90nm CMOS</td>
<td>217</td>
<td>-8.8</td>
<td>128</td>
<td>0.1</td>
<td>3rd</td>
<td>N/A</td>
<td>0.531</td>
</tr>
<tr>
<td>TMTT'13</td>
<td>130nm SiGe BICMOS</td>
<td>201.5</td>
<td>-7.2</td>
<td>30</td>
<td>0.64</td>
<td>2nd</td>
<td>-87 @1MHz</td>
<td>0.0725</td>
</tr>
<tr>
<td>TCAS-I'15</td>
<td>65nm CMOS</td>
<td>239</td>
<td>-4.7</td>
<td>18.5</td>
<td>1.47</td>
<td>2nd</td>
<td>-98.4 @1MHz</td>
<td>0.225</td>
</tr>
<tr>
<td>ISSCC'16</td>
<td>130nm SiGe BICMOS</td>
<td>190.5</td>
<td>-2.1</td>
<td>294</td>
<td>0.21</td>
<td>2nd</td>
<td>-102.6 @10MHz</td>
<td>0.64</td>
</tr>
<tr>
<td>RFIC'16</td>
<td>130nm SiGe BICMOS</td>
<td>210</td>
<td>1.4</td>
<td>61</td>
<td>2.4</td>
<td>2nd</td>
<td>-87.5 @1MHz</td>
<td>0.08</td>
</tr>
<tr>
<td>This work</td>
<td>65nm CMOS</td>
<td>177</td>
<td>3.43/0.66**</td>
<td>23.4/4.5**</td>
<td>9.4/25.9**</td>
<td>Fund.</td>
<td>-104.8 @1MHz</td>
<td>0.132 (0.0169*)</td>
</tr>
</tbody>
</table>

- Maximum efficiency of 25.9% with the output power of 0.66 dBm.
- Maximum output power of 3.43 dBm with the efficiency of 9.4%
OOK THz Transmitter

Distance = 46.2 mm

Data Rate = 12.1 Gb/s

Our demo for the single mode Sub-THz interconnect

- Data Rate = 12.1 Gb/s  \( (\text{BER} < 1 \times 10^{-12}) \)
- Distance = 46.2 mm
- Best Energy Efficiency = 0.32 pJ/b
- Best BW Density = 80.7 Gb/s/mm²

OOK THz Transmitter Meas. Results

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<th>ISSCC '16</th>
<th>ISSCC '16</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>40 nm CMOS</td>
<td>40 nm CMOS</td>
<td>65 nm CMOS</td>
<td>28 nm CMOS</td>
<td>28 nm SOI</td>
<td>65 nm CMOS</td>
<td>65 nm CMOS</td>
</tr>
<tr>
<td>Frequency (Hz)</td>
<td>135G</td>
<td>120G</td>
<td>107G</td>
<td>0</td>
<td>194T</td>
<td>68G - 102G</td>
<td>165G</td>
</tr>
<tr>
<td>Modulation</td>
<td>ASK</td>
<td>CPFSK</td>
<td>OOK</td>
<td>N/A</td>
<td>OOK</td>
<td>16-QAM</td>
<td>OOK</td>
</tr>
<tr>
<td>Distance (mm)</td>
<td>100</td>
<td>1000</td>
<td>300</td>
<td>5000</td>
<td>N/A</td>
<td>100</td>
<td>46.2</td>
</tr>
<tr>
<td>Chip Area (mm²)</td>
<td>2</td>
<td>0.48</td>
<td>0.68</td>
<td>25.3</td>
<td>N/A</td>
<td>6</td>
<td>1.6</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>98</td>
<td>52</td>
<td>34</td>
<td>403</td>
<td>123</td>
<td>560</td>
<td>3.2 / 15.6</td>
</tr>
<tr>
<td>Data Rate (Gb/s)</td>
<td>10</td>
<td>12.7</td>
<td>10</td>
<td>25.8</td>
<td>25</td>
<td>56</td>
<td>10 / 12.1</td>
</tr>
<tr>
<td>Channel Cross Section Area (mm²)</td>
<td>&gt; 1.4</td>
<td>3.14</td>
<td>&gt; 3.23</td>
<td>103.36</td>
<td>N/A</td>
<td>&gt; 3.23</td>
<td>0.15</td>
</tr>
<tr>
<td>Energy Efficiency (pJ/b)</td>
<td>9.8</td>
<td>4.8</td>
<td>3.4</td>
<td>15.6</td>
<td>4.9</td>
<td>10</td>
<td>0.32 / 1.29</td>
</tr>
<tr>
<td>Bandwidth Density* (Gbps/mm²)</td>
<td>7.1</td>
<td>4</td>
<td>3.1</td>
<td>0.25</td>
<td>N/A</td>
<td>17.3</td>
<td>66.7 / 80.7</td>
</tr>
<tr>
<td>FoM (fJ/mm²/b)</td>
<td>137.2</td>
<td>15.1</td>
<td>36.6</td>
<td>323</td>
<td>N/A</td>
<td>323</td>
<td>1 / 4.2</td>
</tr>
</tbody>
</table>

- Max. output power: 0.63 dBm
- Highest DC-to-RF efficiency: 10.6% at 6.4mW DC power consumption with -1.67 dBm output power.

Y. Ye, B. Yu, and Q. J. Gu, “A 165 GHz Transmitter with 10.6% Peak DC-to-RF Efficiency and 0.68 pJ/bit Energy Efficiency on 65 nm Bulk CMOS,” TMTT 2016
Orthomode TI System Demonstration

(a) Both paths at 4.0 Gb/s, and (b) Both paths at 7.5 Gb/s.

- The data rates for P31 only and P42 only are up to 10.0 Gb/s.
- With the interference from each other, the data rates are up to 7.9 Gb/s and 9.0 Gb/s for P31 and P42

Q. J. Gu, B. Yu, X. Ding, Y. Ye, X. Liu, and Z. Xu “THz interconnect: the last centimeter communication,” SPIE, May 2019
Conclusions

• Interconnect gap is a long-standing challenge.
• The most challenging communication distance is around meter range, where both EI and OI face great difficulties.
• Low loss frequency insensitive channel is the key to reach 100 Gbps over meters.
• Circuit/system performance at higher frequencies need to keep advancing.
• Within the meter range, the maximum achievable bandwidth is also determined by dispersion, for which channelization is a good approach to mitigate its effects.

THz Interconnect has the potential to complement electrical and optical interconnects for the meter range communications.
Acknowledgements

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• Prof. Xiaoguang Liu
• NSF for funding support