Tbps Massive MIMO: Mapping System Performance to Hardware Specs

Presenters: Upamanyu Madhow (UCSB) and Sundeep Rangan (NYU)
The Context

Center for Converged TeraHertz Communications and Sensing
https://comsenter.ece.ucsb.edu/

Using the electromagnetic spectrum between 100 and 1000GHz, we seek to develop wireless communications systems having unprecedented data capacity and compact radio imaging systems having unprecedented resolution.

Design approach requires tight coupling of systems, signal processing & hardware
- 6G and beyond thought experiments
- Aggressive system performance targets
- Exploit scale (number of antennas, available bandwidth) to relax hardware specs
This talk

• Part 1 (Madhow): How scale helps alleviate hardware bottlenecks
• Part 2 (Rangan): Understanding receiver energy efficiency
Part 1: Alleviating hardware bottlenecks via scale

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University of California, Santa Barbara
Key hardware bottlenecks for all-digital architectures
1) Need one RF chain for each antenna. Can we relax the specs enough that CMOS works?
2) Phase noise is high at millimeter wave and THz. Don’t things get worse as we scale to a large number of antennas?
3) ADC cost, power consumption and availability is limited as we scale up bandwidth

Message: Hardware bottlenecks can be alleviated via scale
The Message: Hardware Bottlenecks can be alleviated by Scale

- CMOS allows scaling, but is sloppy ➔ nonlinearities, phase noise

Typical 3\textsuperscript{rd} order nonlinearities and input distributions (average over antennas)

- Bandwidth of 5-10 GHz ➔ severe ADC constraint

Phase noise PSD (average over tiles)

Standard low-precision ADC (average over antennas)
Designing around nonlinearities


System parameters

Load Factor $\beta = \frac{\text{Number of users}}{\text{Number of antennas}}$

Min and Max Link Distances: $R_{\text{min}}, R_{\text{max}}$

Power control factor

System parameters to be mapped to hardware specs
Nonlinearities considered

Third order nonlinearities (passband & baseband)

\[ g(y(t)) = \begin{cases} 
  y(t)(1 - \frac{0.44|y(t)|^2}{3P_{1dB}}) & \text{if } |y(t)|^2 \leq \frac{P_{1dB}}{0.44} \\
  \frac{y(t)}{|y(t)|}\sqrt{P_{1dB}} & \text{if } |y(t)|^2 > \frac{P_{1dB}}{0.44} 
\end{cases} \]

Overloaded uniform ADC
Design Framework

• Per-antenna nonlinearities modeled as linear + self-noise
  – Standard Bussgang approximation

• Self-noise averages over antennas
  – Effective SNR is reduced compared to a linear system

• Standard linear multiuser detection used
  – Performance of ideal system without self-noise bounds that of system with self-noise

• System performance requires self-noise management ➔ hardware specs for RF, baseband and data conversion
Modeling per-antenna self-noise

- Sum of signals into an antenna well modeled as zero mean complex Gaussian
- Bussgang Approximation: linear fit to nonlinearity

\[ Z \sim CN(0, 1) \quad g(.) \quad g(Z) = aZ + e \]

\[
\begin{align*}
p(y_{\text{Out}}) & \\
\text{Var}(y_{\text{Out}}) & \\
\text{Bias}(y_{\text{Out}}) & \\
\end{align*}
\]

Self-noise
Self-noise averaged across array

\[ Z \sim CN(0,1) \rightarrow g(.) \rightarrow g(Z) = aZ + e \]

**Intrinsic SNR**

\[ SNR(g) = \frac{a^2}{\sigma_e^2} \]

**Matched filter bound** (includes self-noise but not interference)

\[ SNR_k = SNR(g) \left( \frac{1}{\beta} \right) \left( \frac{A_k^2}{A_{rms}^2} \right) \]

Low load factor is better

Take worst-case value for edge user (depends on power control)
Example: Intrinsic SNR for ADCs

<table>
<thead>
<tr>
<th>k</th>
<th>a</th>
<th>$\sigma^2$</th>
<th>SNR(g) (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.63</td>
<td>0.23</td>
<td>2.4</td>
</tr>
<tr>
<td>2</td>
<td>0.88</td>
<td>0.1</td>
<td>8.8</td>
</tr>
<tr>
<td>3</td>
<td>0.96</td>
<td>0.03</td>
<td>14.3</td>
</tr>
<tr>
<td>4</td>
<td>0.99</td>
<td>0.01</td>
<td>19.6</td>
</tr>
<tr>
<td>5</td>
<td>0.997</td>
<td>0.003</td>
<td>24.9</td>
</tr>
</tbody>
</table>

Need better RF specs to maintain intrinsic SNR as #ADC bits increases.
Bounding the impact of multiuser interference

BER for 5% outage

SNR_{edge} reqd for 10^{-3} BER at 5% outage

Upper bound on noise enhancement via analysis or simulation of ideal system
Large # antennas and low load factor is an attractive scaling regime (relaxed RF specs, low required ADC precision)
Phase noise in tiled architectures


Oscillator phase noise

Supposed to be scary at mmWave frequencies
Tiled architectures for scaling

- Tiled architectures are attractive

\[ N = N_T \times N_0 \]

- Single carrier modulation*
- Digital beamforming
- Uplink

- Synchronizing tiles..?

*LMMSE Multi-User Detection (MUD)\[\text{conv. and ADC on tile}\]

Phase noise in tiled architectures

- Clock distribution in the tiled array
  - Distribute lower frequency clock to tiles
  - Perform frequency multiplication on tile using PLL

~ 20 GHz
~ 140 GHz
Phase noise in tiled architectures

- Clock distribution in the tiled array
  - Sources of phase noise: reference (common over array), VCO (independent over tiles)
Analytical framework

Linear PLL model
• Reference phase noise gets lowpass filtered
• VCO phase noise gets highpass filtered

Abstraction for post-MUD derotation

\[ h_W[t/T_s] = \delta[t/T_s] - \frac{1}{W} \sum_{d=1}^{W} \delta[t/T_s - d] \]
Results from analytical framework

- Impact of common phase noise negligible
- Impact of VCO noise insensitive to/improves with #tiles

Self-noise

\[ A_{SU} \sim N\left(N\left(1 - \frac{\sigma_\phi^2}{2}\right), \frac{N_t N_0^2}{2} \sigma_\phi^4\right) \]

- Decreases with # tiles

Multiuser interference

\[ \frac{\sigma_I^2}{S_p} \approx \frac{(K - 1) N_0 G_0^2 \sigma_V^2}{N} \approx \beta \sigma_V^2 \]

- Insensitive to # tiles
- Scales with load factor
Example PSD Mask

<table>
<thead>
<tr>
<th>Parameter:</th>
<th>$N$</th>
<th>$M$</th>
<th>$N_T$</th>
<th>$\beta$</th>
<th>$f_c$</th>
<th>$N_f$</th>
<th>$B$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value:</td>
<td>256</td>
<td>16</td>
<td>16</td>
<td>$\frac{1}{4}$</td>
<td>140 GHz</td>
<td>14</td>
<td>5 GHz</td>
</tr>
</tbody>
</table>

$\beta = 1/4$, SNR = 14 dB, $P_E \leq 10^{-3}$

$$a_0 = 2.25 \times 10^{-11} \text{ W/Hz}, \quad a_1 = 9 \times 10^{-4} \text{ W}, \quad a_2 = 9 \times 10^2 \text{ W Hz}, \quad a_3 = 9 \times 10^8 \text{ W Hz}^2$$
Part 2: Understanding Energy Efficiency in Millimeter Wave Receivers Above 100 GHz

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1NYU Wireless, Brooklyn, NY
2Dept of ECE, University of California, Santa Barbara, USA
Outline

• Motivation
• Analysis Framework
• Results at 140 GHz
• Perspectives and Future Work
Energy Efficiency Above 100 GHz

- **Power consumption**: Key challenge for receivers above 100 GHz
  - Large numbers of antenna elements
  - Poor device efficiency
  - Wide bandwidths

- **Basic questions**
  - What are the real bottlenecks?
  - What power can be achieved?

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Reference Receiver Architecture

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier</td>
<td>140 GHz</td>
</tr>
<tr>
<td>Number RX antennas</td>
<td>16, 64</td>
</tr>
<tr>
<td>Architecture</td>
<td>Fully digital</td>
</tr>
<tr>
<td>Bandwidth per carrier</td>
<td>190.08 MHz</td>
</tr>
<tr>
<td>Num carriers</td>
<td>8</td>
</tr>
</tbody>
</table>

• Consider TX of a single symbol $x$
• RX after beamforming obtains: $z = w^H \Phi(\sqrt{E_s}wx, d)$
  – $\Phi(\cdot)$ memoryless noisy, nonlinear model for RFFE
  – $w$: RX spatial signature
• Model incorporates arbitrary nonlinearities and noise
  – LNA, saturation, quantization, …
Given any noisy non-linear model, define the output SNR

- $\gamma_{out} =$SNR achievable with linear equalization
- Can be computed from joint distribution on $(x, z)$
- Provides a bound on the achievable capacity

Output SNR includes effects of:
- Channel, noise and any non-linear distortion
Input to Output SNR Regimes

- Common input-output SNR relation
  \[ \gamma_{out} = \frac{N_{rx} \gamma_{in}}{F + N_{rx} \gamma_{in}/\gamma_{sat}} \]

- Low SNR regime: \( \gamma_{out} \approx \frac{\gamma_{in} N_{rx}}{F} \)
  - \( F \): Effective noise figure

- High SNR regime: \( \gamma_{out} \approx \gamma_{sat} \)
  - \( \gamma_{sat} \): Saturation SNR
Power Optimization Methodology

**Design parameters** $\theta$
- Choices for each RFFE component (e.g., LNA, mixer, LO, ADC,…)

**For each $\theta$, run link level simulation with component models**
- Find input to output SNR mapping
- Extract performance metrics: Noise figure, saturation SNR and power

**Minimize power for given targets**
\[
\min P(\theta) \quad \text{s.t.} \quad \gamma_{sat}(\theta) \geq \gamma_{sat}^{tgt}, \quad F(\theta) \leq F^{tgt}
\]
Critical performance for higher mmWave bands

The DC power drawn by the LNA, \( P_{\text{LNA}} \), can be calculated as [24]:

\[
P_{\text{DC}} = \frac{G}{\text{FOM}(F - 1)},
\]

- \( G \): Gain
- \( \text{FOM} \): Figure of merit
- \( F \): Noise figure

Common Base (CB) or a hybrid Common Base/Common Emitter (CB/CE) topology

90-nm SiGe BiCMOS HBT technology:

- \( f_{\text{max}} = 310 \) GHz
- Peak performance about 2 mA/\( \mu \text{m} \).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LNA(^{(1)})</th>
<th>LNA(^{(2)})</th>
<th>LNA(^{(3)})</th>
<th>LNA(^{(4)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Stages</td>
<td>3</td>
<td>3</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Topology</td>
<td>CB</td>
<td>CB</td>
<td>CB</td>
<td>CB/CE</td>
</tr>
<tr>
<td>Design [( \mu \text{m} )]</td>
<td>1-2</td>
<td>2-4</td>
<td>4</td>
<td>2-4</td>
</tr>
<tr>
<td>Noise Figure [dB]</td>
<td>7.71</td>
<td>7.69</td>
<td>7.50</td>
<td>7.48</td>
</tr>
<tr>
<td>Gain [dB]</td>
<td>12.22</td>
<td>11.85</td>
<td>11.13</td>
<td>16.56</td>
</tr>
<tr>
<td>IIP3 [dBm]</td>
<td>-3.30</td>
<td>-6.12</td>
<td>-9.15</td>
<td>-8.90</td>
</tr>
<tr>
<td>FOM [mw(^{-1})]</td>
<td>0.3082</td>
<td>0.4551</td>
<td>0.6049</td>
<td>0.6409</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>11.55</td>
<td>7.2</td>
<td>4.8</td>
<td>15.9</td>
</tr>
</tbody>
</table>

Tab: Parameters of the designed LNAs
Mixer

- Double-balanced active mixer designs
- Gilbert cell design
- 90-nm SiGe BiCMOS HBT technology

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Mixer(1)</th>
<th>Mixer(2)</th>
<th>Mixer(3)</th>
<th>Mixer(4)</th>
<th>Mixer(5)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design [μm]</td>
<td>6</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>41</td>
<td>23.6</td>
<td>15.2</td>
<td>9.7</td>
<td>5</td>
</tr>
</tbody>
</table>

Power consumption of the IF mixers
Local Oscillator

- Critical component for digital beamforming
- High power consumption from frequency multiplication

- Tiled LO distribution
  - Divide $N_{rx}$ mixers into $N_d$ tiles
  - Generate one LO for each tile
  - Split LO via power divider in each tile

- Optimize tile distribution
  - Optimize $N_d$
  - Depending on LO power required at mixer

<table>
<thead>
<tr>
<th>$P_{in}$ [dB]</th>
<th>$P_{out}$ [dB]</th>
<th>$f_{in}$ [GHz]</th>
<th>$f_{max}$ [GHz]</th>
<th>$P_{DC}$ [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>-10</td>
<td>2</td>
<td>32.5</td>
<td>130</td>
<td>48</td>
</tr>
</tbody>
</table>

Tab: Parameters and DC power consumption of the ×4 multiplier design

[Graph showing total DC power of the LO as a function of the power of the local oscillator]
A/D Converter

- The power consumption of each ADC is given by [18],
  \[ P = \text{FOM} \, f_s \, 2^n \]
  - FOM: Figure of merit of the data conversion (energy per conversion step)
  - \( f_s \): Sample rate
  - \( n \): Number of bits
- Prior simulations [18]–[21] have indicated that 4 bits are sufficient for the most cellular data and data control operation
- FOM = 65 fJ/conv, based on a 4-bit flash-based ADC designed in [31].
Power Optimization Results (1/2)

Fig: Minimum power consumption for each design choice $\theta$ based on a target noise figure $F^{tgt}$ and target saturation SNR $\gamma^{tgt}_{sat}$.
Power Optimization Results (2/2)

### Tab: Compare a set of optimized designs with a baseline analyzed in [9]. The parameters of the designs (top), the power consumption estimates in mW (bottom).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Baseline [9]</th>
<th>Design(^{(1)})</th>
<th>Design(^{(2)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(N_{rx})</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>(F) [dB]</td>
<td>8</td>
<td>7.95</td>
<td>8.37</td>
</tr>
<tr>
<td>(\gamma_{sat}) [dB]</td>
<td>25</td>
<td>25.64</td>
<td>32.31</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Component</th>
<th>Baseline [9]</th>
<th>Design(^{(1)})</th>
<th>Design(^{(2)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA</td>
<td>76.8</td>
<td>254.4</td>
<td>76.8</td>
</tr>
<tr>
<td>Mixer</td>
<td>-</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td>LO</td>
<td>1568</td>
<td>63.57</td>
<td>76.8</td>
</tr>
<tr>
<td>ADC</td>
<td>65.43</td>
<td>65.43</td>
<td>130.86</td>
</tr>
<tr>
<td>Total</td>
<td>1710</td>
<td>464</td>
<td>358</td>
</tr>
</tbody>
</table>

Tab: Compare a set of optimized designs with a baseline analyzed in [9]. The parameters of the designs (top), the power consumption estimates in mW (bottom).
Acknowledgements

SRC, DARPA, NSF, and the NYU WIRELESS Industrial Affiliates
Conclusions

- General mathematical framework
- Detailed circuit & link simulations for 140 GHz RX
- Dramatic 70 to 80% power reduction
- Open-source MATLAB simulation package
- Future work:
  - Phase shifter architectures
  - Out of band interference rejection

<table>
<thead>
<tr>
<th>Component</th>
<th>Baseline [9]</th>
<th>Design$^{(1)}$</th>
<th>Design$^{(2)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA</td>
<td>76.8</td>
<td>254.4</td>
<td>76.8</td>
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<tr>
<td></td>
<td>307.2</td>
<td>1017.6</td>
<td>307.2</td>
</tr>
<tr>
<td>Mixer</td>
<td>-</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>320</td>
<td>320</td>
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<tr>
<td>LO</td>
<td>1568</td>
<td>63.57</td>
<td>76.8</td>
</tr>
<tr>
<td></td>
<td>6272</td>
<td>82.3</td>
<td>204.15</td>
</tr>
<tr>
<td>ADC</td>
<td>65.43</td>
<td>65.43</td>
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<td></td>
<td>261</td>
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<td>523.44</td>
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<tr>
<td>Total</td>
<td>1710</td>
<td>464</td>
<td>358</td>
</tr>
<tr>
<td></td>
<td>6840</td>
<td>1682</td>
<td>1355</td>
</tr>
</tbody>
</table>

Tab: Power consumption estimates (in mW) for the baseline two optimized designs.

Thank you!