Energy and Spectrally Efficient Communication using mm-Wave and sub-THz Bands

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ComSenTer: The Big Picture

- Basestation MU-MIMO ↔ Handset with Beamforming
- Applications: Sensing, Imaging, and Comm
- Short range (~cm) links to long range (~km)
Presentation Overview

• Step 1:
  – Hydra: How to build mm-wave massive MIMO systems to increase spatial capacity by 10x

• Step 2:
  – Hummingbird: How to build energy efficiency CMOS transceivers to realize 100 Gb/s

• Step 3:
  – Charm: 140 GHz massive MIMO system with 1 Tb/s capacity
HYDRA

Hydra: mm-Wave Massive MIMO

Lorenzo Iotti, Greg Lacaille, Emily Naviasky
Elad Alon, Borivoje Nikolic, Ali Niknejad
Architecture

Multi Module Architecture:

• “Head” Module
  - Radio front-end
  - Conjugate Beamforming

• “Spine” Module
  - Data conversion
  - Aggregation of user data across sub arrays

• “Tail” Module
  - Zero forcing of inter user interference
  - Standard radio backend processing
**MIMO vs MU-MIMO**

- SU-MIMO has low rank at mm-wave / outdoors.
- MU-MIMO channel has full rank because users are spread out.

- Simple beamforming does not cancel interference. The interference is rejected by the level of the sidelobes.
- MU-MIMO can null inter-user interference by placing nulls in undesired directions.
Two-Stage Beamforming

- Linear beamforming algorithm: Conjugate BF
  - Daisy chain subarrays for modularity

\[ H^* = (H_1^* + H_2^* + \cdots) \]
Two-Stage Beamforming

- Improved Linear BF Algorithm: Zero-Forcing
  - Performed in two stages
    1. Improve SNR
    2. Reduce inter-user interference

\[ H_{ZF} = H^*(H^*H)^{-1} \]

(Analog Front-End)  (Digital Back-End)
Analog and/or Digital Beamforming
Top Level Architecture

Goals
- 16 element x 16 user subarray
  - Demonstrate many user analog beamforming
- Low power consumption
  - Can realize massive array with many tiles and manageable power
- E-band
  - 71-76 GHz, 81-86 GHz

ASIC
- 28nm CMOS
- 16 mm²
- 1V Supply

[Naviasky, ISSC 2021]
RX Front-End

- 25GHz analog PLL + frequency tripler
- LO distribution using non-isolated power splitters
  - Use $\lambda/4$ TLines for both matching and LO fan-out
- Per-element quadrature generation

- Mixer-first RX for wideband operation and low power
- Frequency-translational feedback reduces mixer size while preserving matching and noise figure

[Iotti, ISSC 2018]
Packaging

- Interposer with linear patch antenna array
System Power

- Power measured with BF active for all 16 elements and 16 users
  - Can be disabled if not in use, or bypassed for digital BF

Total: 1.71 W
Phase Shifter Characterization

- Angle and amplitude of points measured on 100MHz tone

RMS Vector Error = 3%
Single User Constellations

Single User Lower E-Band
60 cm Line of Sight
PRBS 10 (1k symb)
TX Power: -12 dBm
TX Ant Gain: 22 dBi

Data Rate up to 2 Gb/s
Testing Setup: Multiple User

User positions:
- -36 deg
- -15 deg
- 13 deg
- 40 deg

Distance: ~1.5m
Multi-User Constellations

Multiple User 73 GHz Carrier
150 cm Line of Sight
PRBS 15 (33k symb)
TX Power: 8 dBm
TX Ant Gain: 3 dBi

4 Simultaneous Users
Data Rate up to .5 Gb/s Per User

- Data Rate limited to 250 MBd by off the shelf TX DAC
# Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>JSSC ’19</th>
<th>ISSCC ’16</th>
<th>ISSCC ’19</th>
<th>ISSCC ’20</th>
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<tbody>
<tr>
<td>RX/TX</td>
<td>RX</td>
<td>RX/TX</td>
<td>RX/TX</td>
<td>RX/TX</td>
<td>RX/TX</td>
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<tr>
<td>Freq. (GHz)</td>
<td>71-86</td>
<td>80-100</td>
<td>57-66</td>
<td>71-76</td>
<td>57-71</td>
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<tr>
<td>Phase Shifter Type</td>
<td>BB</td>
<td>RF</td>
<td>BB</td>
<td>BB</td>
<td>RF</td>
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<tr>
<td>No. RX Elements/IC</td>
<td>16</td>
<td>16</td>
<td>4</td>
<td>4</td>
<td>4</td>
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<tr>
<td>No. of Beams/IC</td>
<td>16</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
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<tr>
<td>Total RX Power/IC* (mW)</td>
<td>1710</td>
<td>4300</td>
<td>508</td>
<td>672</td>
<td>355</td>
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<tr>
<td>RX Power/Ant. (mW)</td>
<td>107</td>
<td>269</td>
<td>127</td>
<td>168</td>
<td>88</td>
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<tr>
<td>RX Power/Ant./Beam (mW)</td>
<td>7</td>
<td>269</td>
<td>127</td>
<td>168</td>
<td>44</td>
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<tr>
<td>Gain (dB)</td>
<td>35</td>
<td>42</td>
<td>62</td>
<td>36.7</td>
<td>45.7</td>
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<tr>
<td>NF (dB)</td>
<td>9-11†</td>
<td>6.5-8</td>
<td>4.8-6.2</td>
<td>6</td>
<td>5.8</td>
</tr>
<tr>
<td>Single User Data Rate (Gbps)</td>
<td>2</td>
<td>10</td>
<td>7</td>
<td>7.2 (16 ICs)</td>
<td>32</td>
</tr>
<tr>
<td>RX EVM (dB)</td>
<td>-18</td>
<td>-22</td>
<td>-20</td>
<td>-24</td>
<td>-19</td>
</tr>
<tr>
<td>Die Area (mm²)</td>
<td>16</td>
<td>35.2</td>
<td>7.9</td>
<td>5.04</td>
<td>8.75</td>
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<tr>
<td>Process</td>
<td>28nm CMOS</td>
<td>0.18 μm BiCMOS</td>
<td>45 nm CMOS</td>
<td>22nm FinFET</td>
<td>28nm CMOS</td>
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</table>

* Includes LO circuits and BB output buffers
† Based on single-channel measurements of the RX front-end, plus 0.5dB simulated contribution of baseband circuits
Performance Overview

Hydra Head ASIC Power Budget

<table>
<thead>
<tr>
<th></th>
<th>TOT PDC</th>
<th>PDC/USER</th>
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</thead>
<tbody>
<tr>
<td>RX front-end</td>
<td>190 mW</td>
<td>12 mW</td>
</tr>
<tr>
<td>LO gen+distr</td>
<td>210 mW</td>
<td>13 mW</td>
</tr>
<tr>
<td>BB beamformer</td>
<td>600 mW</td>
<td>37 mW</td>
</tr>
<tr>
<td>BB output buff</td>
<td>500 mW</td>
<td>30 mW</td>
</tr>
<tr>
<td><strong>TOT</strong></td>
<td><strong>1.5 W</strong></td>
<td><strong>92 mW</strong></td>
</tr>
</tbody>
</table>

Power Consumption:
16 W $\rightarrow$ 1.5 W
>10x power reduction

Signal BW:
250 MHz $\rightarrow$ 2 GHz
x8 bandwidth increase
HUMMINGBIRD

*Hummingbird:* A Wireless Dual-Polarization 120 GHz Transceiver Targeting 100Gb/s Data Rate

Chip Overview

- Dual channel to support MIMO, spatial diversity using polarization, and multi-modal excitation on waveguides
Hummingbird Transmitter
Hummingbird Receiver
Wideband BB Gain Stages

- Cherry-Hooper (Gm + TIA) inverter stages low current and wideband (de-couple gain/BW)
- Differential stages added for CM rejection (CMRR ~ 20 dB)
- DC current ~ 16mA per I/Q
Antennas and Packaging
DC Power Consumption Estimates

<table>
<thead>
<tr>
<th>TX (one channel)</th>
<th>RX (one channel)</th>
<th>LO</th>
<th></th>
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<tbody>
<tr>
<td>Modulator + PA</td>
<td>70mW</td>
<td>Baseband amp</td>
<td>10mW</td>
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<tr>
<td>PRBS</td>
<td>40mW</td>
<td>LNA</td>
<td>31mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mixers</td>
<td>26mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RX IQ gen</td>
<td>16mW</td>
</tr>
<tr>
<td><strong>Total:</strong></td>
<td><strong>110mW</strong></td>
<td><strong>Total:</strong></td>
<td><strong>83mW</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Total:</strong></td>
</tr>
</tbody>
</table>

- RX: 297mW/chip @ 50Gb/s/channel for two channels: **3pJ/bit**
- TX: 271mW/chip not including clocking power **2.7pJ/bit**
  - Including clocking becomes 351mW (3.5pJ/bit)
- **Full link: 5.7pJ/bit** @ 100Gb/s dual-channel rate
PCB Closeup

- Chip mounted on PCB directly (COB)
- Patch antennas with “shielding” to minimize effect of substrate modes
Single Channel Performance

- Data captured with **no averaging**. Raw constellation (no processing) can be captured with averaging to demonstrate the link is “real”
- Simple low tap count equalizer to avoid “overfitting” since Tx pattern is PRBS.
### Comparison Chart

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>113GHz</td>
<td>230GHz</td>
<td>96GHz (upper channel)</td>
<td>130GHz</td>
</tr>
<tr>
<td>Data Rate/Channel</td>
<td>80Gb/s</td>
<td>90Gb/s</td>
<td>60Gb/s</td>
<td>12.5Gb/s</td>
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<tr>
<td>Modulation</td>
<td>16QAM, QPSK</td>
<td>16QAM</td>
<td>64QAM, 32QAM, 16QAM, QPSK</td>
<td>OOK</td>
</tr>
<tr>
<td>DC Power</td>
<td>470mW (TX + PRBS) 500mW (RX)</td>
<td>960mW (TX) 1000mW (RX)</td>
<td>120mW (TX) 160mW (RX)</td>
<td>49mW (TX) 24mW (RX) (at 0.5m, 11.5Gb/s)</td>
</tr>
<tr>
<td>Energy Efficiency  (pJ/b)</td>
<td>12.1</td>
<td>21.8</td>
<td>2.3</td>
<td>6.3 (at 0.5m, 11.5Gb/s)</td>
</tr>
<tr>
<td>Distance</td>
<td>10cm</td>
<td>100cm</td>
<td>20cm</td>
<td>0.5m, 5m</td>
</tr>
<tr>
<td>Technology</td>
<td>28nm CMOS</td>
<td>0.13μm SiGe HBT</td>
<td>65nm CMOS</td>
<td>55nm BiCMOS</td>
</tr>
<tr>
<td>Level of Integration (IC)</td>
<td>RX, TX (w/ DAC), LO</td>
<td>RX only, TX only (separate chips), LO</td>
<td>RX, TX (IF input to TX, no DAC), LO</td>
<td>RX, TX+VCO</td>
</tr>
</tbody>
</table>

- Fastest CMOS / channel link
- Close to SiGe performance
- Good energy efficiency ~ photonic link
CharmIC: 140 GHz CMOS MIMO – The Future

- Exploit high modulation BW (10% fractional BW), ~14 GHz RF, (10 + 10) GHz I/Q BB
- Four integrated Rx, Tx, and shared PLL/LO, 16 channels per package
- Support up to 64-QAM → up over 96 Gb/s per RF channel (short range applications with higher SNR)
- Expected Performance: DC Power ~ 100mW / ch, NF < 7 dB, P_{-1dB} > 4.4 dBm
CharmIC: Power of Arrays

- A modest array for Tx and Rx
- System to support ~1 Tb/s Tx and Rx at 10 m range
- Power ~ 10W on each side
  - Solar cell plus battery can keep this system running

New Spine CharmIC

- IC = 100mW * 8 ~ 1W
- ADC/DAC ~ 1W (100fJ/conv)
- SerDes ~ 5W (5pJ/bit)
- Overhead ~ 3W
- Total power < 10W!

Library of Congress ~ 15 Tbytes (a few minute)
Charming Conclusion

- Mm-Wave MIMO works! Need distributed signal processing.
- Very wideband communication > 100 GHz with Hummingbird (tested 80 Gb/s per channel so far)
- Working towards a medium and long-range array at 140 GHz to demonstrate Terabit/s wireless connectivity
  - Support more user streams / spatial diversity
  - Improve CMOS transceiver performance and integrate with III-V front-ends
  - Improved package / antenna interface
Acknowledgements

• DARPA/SRC JUMP ComSenTer
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