High-Efficiency and High-Power Amplifiers for Transmitters above 100 GHz

James F Buckwalter, Mark Rodwell, Kang Ning, Ahmed Ahmed, Andrea Arias-Purdue, Everett O’Malley, and Eythan Lam

University of California – Santa Barbara
Digital Beamformer Requirements

- Digital beamforming analysis can predict optimal PA performance.
- Architecture separates signal generation from RFFE due to space constraints at 140 GHz.
- Consider LO power (per element) and RF upconverter power consumption given an EIRP requirement.
- Optimum RF output power depends on efficiency of PA and total RFU and LO power.
- LO distribution losses are considered (not shown here)

$$N_{OPT} = \sqrt{\frac{\eta_{MOD} EIRP}{\eta_{PA} G_{ANT} (P_{IFU} + P_{LO})}}$$

$$P_{OUT,OPT} = \frac{\eta_{PA}}{\eta_{MOD}} (P_{IFU} + P_{LO})$$
Mapping Digital Beamforming Requirements

- Power, cost, and size are also requirements at these frequency bands.
- Power optimization suggests both III-V/CMOS at silicon scale to access full trade space.

Min. power occurs at 256 elements (< 2 cm x 2 cm) with $P_{dc}$ under 400 W.
Heterogeneous Beamformers above 100 GHz

- CMOS offers integration but limited output power per element above 100 GHz.
- Increased path loss demands higher power per element.
- Architecture:
  - CMOS for DSP/RF up to 30 GHz
  - CMOS SOI/SiGe for mixing to bands above 100 GHz
  - III-V for PA (or LNA)
PA Efficiency in Digital Beamformers

- Find optimum output power per element and total power.
- Current SOA: 10% and 1% for PA and MOD.
- Target SOA: 40% and 10% for PA and MOD.

→ The output power requirement is around 18 dBm to 22 dBm.
→ More efficient PAs push the output power requirement while reducing SWAP.

\[ EIRP = 65 \text{ dBm} \]
Outline

• The Case for Digital Beamforming
• Review of Power Amplifier Trade-offs
• Design Prospects to “Close the Efficiency Gap”
• High-Efficiency Upper-millimeter-wave PAs
Review of Power Amplifier Tradeoffs

- Power amplifiers (PAs) ultimately combine underlying fundamental device limitations with “real” circuit implementation challenges including loss.
- Drain efficiency ($\eta$): RF to DC efficiency is a characteristic of device loadline.
- Gain (G): Available gain of the device is characterized from $f_{\text{max}}$.
- Voltage ($V_K$ and $V_{DD}$): Knee voltage and supply voltage determine usable voltage swing.
- Q ($Q_o$ and $Q_t$): Quality factor of matching elements and impedance transformation.

$$PAE = \eta \left( 1 - \frac{1}{G} \right) \left( 1 - \frac{V_K}{V_{DD}} \right) \left( \frac{Q_o}{Q_o + Q_t} \right)$$
PAE Tradeoffs with Conduction Angle

\[
PAE = \eta \left(1 - \frac{1}{G}\right) \left(1 - \frac{V_K}{V_{DD}}\right) \left(\frac{Q_o}{Q_o + Q_t}\right)
\]

- **Gain is reduced at high frequency.**
- **As gain reduces, best PAE is achieved with conduction closer to class A.**
- **Based on device parameters \(f_{\text{max}}, V_K, V_{DD}, Q_o\), the best possible PAE is found for a given power level.**
- **Interplay between \(Q_t, \eta,\) and gain are taken into consideration.**

\[V_{CC} = 2.5V, \ V_K = 0.7V, \ f_{\text{max}} = 600 \ \text{GHz}, \ Q = 20\]
Device Technologies

• Silicon: Large scale integration and manufacturing
  – SOI CMOS
  – Silicon Germanium
• III-V: Best “junction for the function”
  – InP HBT
  – GaAs HBT
  – GaN HEMT
• Other technologies, such as InP HEMT and bulk silicon CMOS, are not considered due to limited device capability.
Comparison of Device Technologies

- Different device technologies offer different trade-offs based on device characteristics.
- Based on device voltage and current handling we can calculate the RF power (per unit width/length) and loadline resistance.
- InP HBT is within a factor of 2 of the “power density” of GaN at these bands.

<table>
<thead>
<tr>
<th>Technology</th>
<th>$f_{\text{max}}$ (GHz)</th>
<th>$V_{\text{SUP}}$ (V)</th>
<th>$V_K$ (V)</th>
<th>$I_{\text{MAX}}$ (A/mm)</th>
<th>$P_{\text{RF}}$ (W/mm)</th>
<th>$R_{\text{LL}}$ ($\Omega$-mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>InP HBT</td>
<td>600</td>
<td>2.5</td>
<td>0.7</td>
<td>3</td>
<td>1.4</td>
<td>1.2</td>
</tr>
<tr>
<td>SiGe HBT</td>
<td>450</td>
<td>1.3</td>
<td>0.5</td>
<td>2.2</td>
<td>0.44</td>
<td>0.7</td>
</tr>
<tr>
<td>CMOS FET</td>
<td>310</td>
<td>1.1</td>
<td>0.3</td>
<td>1</td>
<td>0.2</td>
<td>1.6</td>
</tr>
<tr>
<td>GaN HEMT</td>
<td>400</td>
<td>12</td>
<td>2</td>
<td>1.6</td>
<td>4.0</td>
<td>12.5</td>
</tr>
</tbody>
</table>

\[
P_{RF} = \frac{1}{4}(V_{DD} - V_K)I_{MAX}
\]

\[
R_{LL} = \frac{2(V_{DD} - V_K)}{I_{MAX}}
\]
Design for Power and Efficiency

- Given a loadline (e.g. 50 Ohm), what is the RF power available from different technologies?
- GaN delivers 15 dB higher power than InP.
- Given an output power, what is the required loadline?
- InP provides best impedance match. CMOS requires large devices which is difficult at 140 GHz.
Theoretical PAE at 140 GHz

- Based on the previous “device” results, we extrapolate the potential PAE for difference technologies incorporating losses for the output matching networks for a given output power.
- InP HBT should remain the highest PAE.
- Silicon technologies takes a significant hit in PAE due to losses in matching elements.

<table>
<thead>
<tr>
<th>Technology</th>
<th>InP HBT</th>
<th>SiGe HBT</th>
<th>CMOS FET</th>
<th>GaN HEMT</th>
</tr>
</thead>
<tbody>
<tr>
<td>PAE (Q = 1000)</td>
<td>45%</td>
<td>34%</td>
<td>32%</td>
<td>43%</td>
</tr>
<tr>
<td>PAE (Q = 10)</td>
<td>39%</td>
<td>24%</td>
<td>23%</td>
<td>34%</td>
</tr>
<tr>
<td>Optimal Conduction Angle</td>
<td>203°</td>
<td>222° 260°</td>
<td>232°</td>
<td></td>
</tr>
</tbody>
</table>

Deep class-AB/class-B designs
Comparison of BEOL Q at 140 GHz

- Low losses for t-lines in III-V (relatively thick gold).
- Highest capacitance density for CMOS SOI
- Tradeoffs for output matching size and power combiners.

<table>
<thead>
<tr>
<th>Technology</th>
<th>InP HBT</th>
<th>SiGe HBT</th>
<th>CMOS SOI</th>
<th>GaN HEMT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Loss per unit length at 140 GHz (dB/mm)</td>
<td>0.74</td>
<td>0.78</td>
<td>0.86</td>
<td>0.4</td>
</tr>
<tr>
<td>Q at 140 GHz</td>
<td>25</td>
<td>30</td>
<td>29</td>
<td>32.5</td>
</tr>
<tr>
<td>Metal Layers</td>
<td>4</td>
<td>10</td>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>Capacitance Density (nF/mm²)</td>
<td>0.3</td>
<td>1.17/2.7</td>
<td>7.6</td>
<td>0.3</td>
</tr>
</tbody>
</table>
Comparison to the Literature: Power

- Output power is between 20 and 30 dBm between 100-250 GHz for III-V
- Output power is between 10-20 dBm between 100-200 GHz for Silicon.
- Output power is between 10-20 dBm for 250-300 GHz in III-V.
Comparing PAE Bounds with State-of-the-Art

- Across 100-300 GHz, InP (□) leads on PAE.
- Below 150 GHz, CMOS/SiGe (red) are reasonable.
- GaN (X) is becoming competitive below 120 GHz.
- 10% PAE improvement through passive losses.
- Above 200 GHz, HBTs (SiGe and InP) dominate potential performance.
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• High-Efficiency Upper-millimeter-wave PAs
Common Base versus Common Emitter: Gain

• Consider MAG for 250-nm InP HBT (shown right)
• Common base offers more gain, particularly at 220 GHz.
• Note that common base is also better (substantially) than common emitter at low current density required for class-B biasing.
• Similar investigations should be undertaken with FETs which are almost exclusively common-source above 100 GHz.
Common Base versus Common Emitter: PAE

• Comparing the Pout and PAE as a function of collector current indicates that PAE is unchanged with choice of transistor configuration.

• Common emitter offers a slight advantage for output power.

• Common base – again – has higher gain. Note gain is at peak PAE.
Loadpull Comparisons of Power and PAE

- The load pull are done with single-ended CB topology.
- Large device combining brings more loss.
- Find PA cell with low loss to achieve higher output power.
Input and Output Impedance Matching

- With CB, gain is the impedance ratio of output to input.
- Same balun can be used with impedance transformation at output.
- Subquarter-wavelength baluns for input and output matching.

Schematic and Micrograph

- Base is directly connected to the ground which provides the lowest impedance on base to reduce the gain reduction from degeneration.
- Layout allows differential AC ground at base.

The chip size is 0.4mm*0.5mm including pads indicating high power density.
Measurement Results

- S-parameter measurements offer good agreement.
- Psat is 15.3 dBm with 7 dB gain.
- Peak PAE is 32%.

PAE and Power across Frequency

- The output power has a 1dB bandwidth from 122-146GHz.
- This chip achieves highest power density and peak PAE.
- First demonstration of a class-B PA above 140 GHz.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Technology</th>
<th>Frequency (GHz)</th>
<th>Gain (dB)</th>
<th>$P_{sat}$ (dBm)</th>
<th>$P_{1dB}$ (dBm)</th>
<th>PAE (%)</th>
<th>Chip Size (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>250nm InP HBT</td>
<td>110-150</td>
<td>14-16</td>
<td>24</td>
<td>20</td>
<td>8.87</td>
<td>1.88</td>
</tr>
<tr>
<td>[3]</td>
<td>130nm SiGe HBT</td>
<td>131-180</td>
<td>27</td>
<td>14</td>
<td>13.2</td>
<td>5.7</td>
<td>0.48</td>
</tr>
<tr>
<td>[6]</td>
<td>0.14µm GaN DHFET</td>
<td>98-122</td>
<td>22</td>
<td>27</td>
<td>-</td>
<td>7</td>
<td>6.98</td>
</tr>
<tr>
<td>[7]</td>
<td>0.1µm InP HEMT</td>
<td>65-140</td>
<td>6-8</td>
<td>14</td>
<td>-</td>
<td>2.4</td>
<td>1.68</td>
</tr>
<tr>
<td>[8]</td>
<td>90nm SiGe BICMOS</td>
<td>110-140</td>
<td>7.7</td>
<td>22</td>
<td>-</td>
<td>3.6</td>
<td>0.62</td>
</tr>
<tr>
<td>This work</td>
<td>250nm InP HBT</td>
<td>118-148</td>
<td>7</td>
<td>15.3</td>
<td>14.4</td>
<td>32</td>
<td>0.2</td>
</tr>
</tbody>
</table>
A >100mW, 140GHz InP PA

- 3-stage amplifier with 4 combined cells.
- Pre-driver stacking with area progression techniques.
- Common base capacitor chosen for peak efficiency at peak power.
- Design key features:
  - Area scaling + unit cell (linearized CB stages) + different stage biasing.
  - Low loss and compact 4:1 combiner
Measurement Results

- Wideband Performance: 3-dB BW=43GHz
- $P_{\text{sat}}=20.5\text{dBm}$, and PAE=20.8% at 140GHz.
- $P_{\text{sat}} = 18.9-20.5\text{dBm}$ and 14.3-20.8% PAE.
- $P_{\text{DC}}=0.53\text{W}$ (measured without heatsink!)


<table>
<thead>
<tr>
<th>$V_{\text{CC1}}$</th>
<th>$V_{\text{CC2}}$</th>
<th>$V_{\text{CC3}}$</th>
<th>$V_{\text{BB1}}$</th>
<th>$V_{\text{BB2}}$</th>
<th>$V_{\text{BB3}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5V</td>
<td>2.5V</td>
<td>1.5V</td>
<td>1.95V</td>
<td>1.4V</td>
<td>1.1V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$I_{\text{CC1}}$</th>
<th>$I_{\text{CC2}}$</th>
<th>$I_{\text{CC3}}$</th>
<th>$I_{\text{BB1}}$</th>
<th>$I_{\text{BB2}}$</th>
<th>$I_{\text{BB3}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>130mA</td>
<td>56mA</td>
<td>34mA</td>
<td>5mA</td>
<td>2mA</td>
<td>1mA</td>
</tr>
</tbody>
</table>
Opportunities for Load Modulation

Load modulation requires PAE to remain high over output backoff

Scenario I
• Maximum PAE and power overlap
• Power and efficiency drop in tandem

Scenario II
• Maximum PAE and power are offset
• Power drops and drain efficiency increases

Example: Class A Bias versus Class B Bias

We need the ability to get high efficiency near class B to leverage load modulation.
Doherty PA Principles

- Doherty PAs modulate load of main amplifier with a peaking (auxiliary) amplifier.
- However, it is very successful and used in modern cellular basestations.
- Basic Doherty uses two amplifiers that are “balanced” with transmission lines.
- Main amplifier operates in class-B.
- Auxiliary amplifier operates in class-C.
- Load modulation becomes more difficult in millimeter-wave bands because the gain is low.
Main Amplifier Load Pull

“Class-B” bias condition load pull for 2x4µm each HBT differential CB PA, this PA is used as main PA in Doherty PA design.

For main PA the power combiner should:
1. Provide capacitive impedance at both peak and compression region
2. Keep high impedance to keep high PAE and Pout
Auxiliary Amplifier Load Pull

- “Class-C” bias condition load pull for 4x4µm each HBT

For auxiliary PA the power combiner should
1. Provide inductive impedance at power back off.
2. A large range of impedance fits the high efficiency.
120GHz InP Doherty Power Amplifier

- To keep the resistive load on main PA, a series 80pH inductor is added at the output.
- At peak output power, the auxiliary PA delivers similar power to main PA.
- Additional phase shift adjustment for class-B and class-C and asymmetrical sizing PA cell should be 210°.
Doherty Simulation Results

- Peak efficiency is 27% at 17dBm. At 6dB back off, the efficiency is 23%.
- Peak gain is close to 6dB but drops to 3dB because of class-C PA gain at full power.
Conclusions

• Future applications above 100 GHz offer large scale integration for digital beamforming arrays and MIMO transceivers.
• Power requirements per channel will exceed 50 mW output power.
• Several technologies can be candidates for operation above 100 GHz. As we move to higher bands InP and SiGe HBTs become best candidates. InP efficiency can theoretically reach 40% at 140 GHz and 30% at 220 GHz.
• Design techniques for high-efficiency include embedding techniques and investigation of common-base approaches for gain.
• New results have blown the top off efficiency above 100 GHz and future improvements remain possible.
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