The Opportunities and Challenges of Using SiGe HBTs in the Deep Cryogenic Temperature Environment

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RFIC Workshop: Cryogenic Electronics for Quantum Computing and Beyond: Applications, Devices, and Circuits

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Outline

• Motivation
• Some Reminders on SiGe Technology
• Using the SiGe HBT at Deep Cryogenic Temperatures
• Compact Modeling and Circuit Implications
• Summary
Strain Engineering in Silicon

Strained Si CMOS

Close Cousins!

SiGe HBTs

Both Are Strain-Enhanced Si-based Transistors
SiGe Strained Layer Epitaxy

The Bright Idea!
Practice Bandgap Engineering
... but do it in Silicon!

![Diagram showing bandgap engineering in SiGe strained layers](image-url)
The SiGe HBT

The Idea: Put Graded Ge Layer into the Base of a Si BJT

Primary Consequences:

- smaller base bandgap increases electron injection ($\beta \uparrow$)
- field from graded base bandgap decreases base transit time ($f_T \uparrow$)

\[
\frac{\beta_{\text{SiGe}}}{\beta_{\text{Si}}} \bigg|_{V_{BE}} \equiv \Xi = \left\{ \frac{\gamma \eta \Delta E_{g,Ge(\text{grade})}/kT e^{\Delta E_{g,Ge(0)}/kT}}{1 - e^{-\Delta E_{g,Ge(\text{grade})}/kT}} \right\}
\]

\[
\frac{\tau_{b,\text{SiGe}}}{\tau_{b,\text{Si}}} = \frac{2}{\eta} \frac{kT}{\Delta E_{g,Ge(\text{grade})}} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge(\text{grade})}} \left[ 1 - e^{-\Delta E_{g,Ge(\text{grade})}/kT} \right] \right\}
\]

\[
\frac{V_{A,\text{SiGe}}}{V_{A,\text{Si}}} \bigg|_{V_{BE}} \equiv \Theta \approx e^{\Delta E_{g,Ge(\text{grade})}/kT} \left[ \frac{1 - e^{-\Delta E_{g,Ge(\text{grade})}/kT}}{\Delta E_{g,Ge(\text{grade})}/kT} \right]
\]

III-V HBT Properties + Si Processing Maturity!
Bandgap Engineering in Si!
SiGe Speed Limits

- $f_T + f_{\text{max}} > 1 \ \text{THz}$ in SiGe Is Clearly Possible \textbf{(at modest lithography)}
- My Prediction: $> 1000 \ \text{GHz} \ f_{\text{max}}$ at $4K \ @ \ BV_{\text{CEO}} > 1.5 \ \text{V} \ldots$ soon!

800 GHz $f_{\text{max}}$ at 4K and counting!

Raw Performance Translates into Favorable Cryo-T Trade-Space (power, gain, noise, etc.)
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Application Temperature Map

SiGe HBTs for all Temperatures?!

250°C  High Temperature
300 K  Room Temperature
233 K  Min PDK Temperature
218 K  Military Spec
50 K   Space Exploration
4 K    Quantum Science & Physics
10 mK

High Temperature
Room Temperature
Min PDK Temperature
Military Spec
Space Exploration
Quantum Science & Physics
Cryo-T ICs for the Quantum Realm

- Quantum Computers and SNSPD Arrays Both Need Cryo-T Electronics
- Cryogenic Integrated Circuits (ICs) Alleviate Noise and Cabling Challenges
  - decrease the number of cables and heat load
  - much lower thermal noise than at room temperature / improved signal-to-noise ratio

72-qubit
→ 1M-qubit?

Cryo-T ICs
The SiGe HBT?

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\]

SiGe HBT is Naturally Suited to Cryo-T Operation!
SiGe HBTs at Cryogenic Temperatures

- SiGe HBTs Achieve Better Performance With Cooling
  - drift field more effective at lower T \(\rightarrow\) shorter transit time
  - as T \(\downarrow\), \(f_T/f_{\text{MAX}}\) \(\uparrow\), \(g_m\) \(\uparrow\), current gain \(\uparrow\), noise \(\downarrow\)

- Demonstrated \(f_{\text{MAX}}\): **800 GHz** at 4.2 K (417 GHz at 300 K) - Operable to **70 mK**

The SiGe HBT is Naturally Suited to Cryo-T Operation
SiGe HBTs at Cryo-T

- SiGe HBTs Function Down to mK Temperatures
- $I_C$ and $I_B$ Quenched Below 40 K, Unchanging Below 15 K
Collector Transport

- **Transport Mechanisms:**
  - Drift-diffusion (scales with T)
  - Trap-assisted tunneling (no scaling with T)
  - Quasi-ballistic transport (weak scaling with T)

What do these look like in terms of band diagram and I/V curves?
Collector Transport Mechanisms

- **Transport Mechanisms:**
  - Drift-diffusion (scales with $T$)
  - Trap-assisted tunneling (no scaling with $T$)
  - Quasi-ballistic transport (weak scaling with $T$)
Impact of Technology Scaling

- Advanced Generation SiGe HBTs Expected to Have Enhanced Tunneling
- Scaling Trend: Shorter base, Higher Ge, Steeper Ge Ramp → Smaller Barrier
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Large-Signal Cryo-T Compact Models

- Simple, Converges at Cryo-T, Well-Calibrated to Data (HICUM)
Circuit-Level Model Verification

- Prototype Wideband (1-17 GHz) SiGe LNA Measured at 12 K for Verification
  - designed for 300K, but used here for modeling verification
Circuit Measurements vs. Simulations

- SiGe LNA Measured at Three Bias Points at 12 K
- Good Prediction by Model at Medium and High Bias
- Gain Offset and Input Matching Deviation Observed at Low Bias
Noise and Large-Signal Modeling

- Noise Temperature Agrees Well Considering Wirebond
- $P_{1\text{dB}}$ Modeling is Decent below 10 GHz, Deviating above 10 GHz
Parameter Variability

- Transistor Mismatch Affects Circuit Operation
- Voltage / Current Mismatch Affects DC Bias
- Capacitance Variations Affect RF Performance
- CMOS Also Has Known Issues With Variability at Low Temperatures
Gummel Characteristics

- $I_C$ and $I_B$ Show Increased Variability at 7 K
- Less Variability at High Injection Levels
DC vs. RF Variability

DC variability >> RF variability

σ/μ (%) vs. DC and RF variability measures:
- $I_C$
- $I_B$
- $\beta$
- $g_m$
- $f_T$
- $\tau_{EC}$
- $C_{BC}$

Temperature Dependence:
- 300 K
- 78 K
- 7 K
Theory of Over-T Variability Trends

- Mathematically:
  - RSD: standard deviation divided by mean $\equiv$ “Variability”
  - Arrhenius Function: $e^{-E_a/kT}$

- Arrhenius Function Appears in All Minority-Carrier Device Equations

Diode / BJT:

$$I_S = \frac{qADn_P n_i^2}{Wn_P N_A} e^{\Delta E_g / kT}$$

SiGe HBT:
(Alleviated Diffusion)

$$I_{C0, SiGe} \propto I_{C0, Si} \frac{e^{\Delta E_g (0) / kT}}{1 - e^{-\Delta E_g (grade) / kT}}$$

$$RSD(e^{-E_a/kT}) = \sqrt{\exp \left[ \left( \frac{\sigma E_a}{kT} \right)^2 \right] - 1} \propto e^{\sigma E_a / kT}$$

$T \downarrow \rightarrow$ Variability $\uparrow$
Bandgap Variations

• Two Dominant Factors That Change Bandgap:
  – bandgap narrowing (BGN) due to heavy doping
  – bandgap shift due to mechanical stress from back-end-of-line (BEOL) layout

• Doping Profile and Stress Profile Variation Increases Bandgap Variability

→ Increased Cryo-T Variability
Cryo-T Variability Trends

- Doping and Stress Profile Also Changes Other Parameters
  - diffusivity, mobility, base width, recombination lifetime, ionization, etc.
- Systematic Approach Required

Mechanical Stress

Doping Profile

Source of Variation → Physical Mechanisms → RSD(Current)

BGN
Mobility
Recombination
Incomplete Ionization
Tunneling

PN Diode
SiGe HBT
Doping Dependence of Variability

- Examine the $\text{RSD}_{50\text{K}}/\text{RSD}_{300\text{K}}$ Across Doping For Each Mechanism
  - low doping: stress dominates
  - high doping: stress and bandgap narrowing dominates
Variability in SiGe HBTs (Ge Effect)

- SiGe HBT Has Ge Across Base and BE/BC Junctions
- EB Doping Variation Changes EB Ge Value
  - worse for steeper Ge ramp

\[ I_{c0, \text{SiGe}} \propto \frac{\Delta E_g(0)/kT}{1 - e^{-\Delta E_g(\text{grade})/kT}} \]
Experimental Confirmation

- 13 SiGe HBT Measured at 300–15K (Same HBT, Same BEOL)
- TCAD Model Calibrated to I-V and Variability Measurement
- Tunneling, BGN, and Stress Variations All Needed for Variability Trends
Deep Dive into Cryo-T Current Mirrors

- Current Mirror (CM) is a **Fundamental Circuit That Copies/Scales Bias Current**
- Proper Bias Current Required for **All RF Circuits Used in Quantum Science**
- CM Errors Impacted by Variability
- CM Errors Increase Performance Uncertainty → Lower Yield, Higher Cost

What is the “Best” CM at Cryo-T?
What Limits the “Best” CM at Cryo-T?
What is Circuit Impact of CM Errors?
List of Measured Current Mirrors

- Comparisons From Different Angles
  - Device Type: CMOS vs. SiGe HBT
  - Topology: Simple vs. Cascode
  - Layout: Normal vs. Common-Centroid (CC)
  - Transistor Size: Large vs. Small

<table>
<thead>
<tr>
<th>Type</th>
<th>Topology</th>
<th>In/Out Size ((\mu)m)</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) SiGe HBT</td>
<td>Simple</td>
<td>0.1x1.25x1</td>
<td>1:1</td>
</tr>
<tr>
<td>(b) SiGe HBT</td>
<td>Simple</td>
<td>0.1x10x1</td>
<td>1:1</td>
</tr>
<tr>
<td>(c) SiGe HBT</td>
<td>CC</td>
<td>0.1x1.25x8</td>
<td>1:1</td>
</tr>
<tr>
<td>(d) nMOS</td>
<td>CC</td>
<td>0.5x2x2</td>
<td>1:1</td>
</tr>
<tr>
<td>(e) nMOS</td>
<td>Cascade, CC</td>
<td>2x10x1</td>
<td>1:1</td>
</tr>
<tr>
<td>(f) SiGe HBT</td>
<td>Wilson</td>
<td>0.1x10x1</td>
<td>1:1</td>
</tr>
<tr>
<td>(g) SiGe HBT</td>
<td>Cascade</td>
<td>0.1x10x1</td>
<td>1:1</td>
</tr>
<tr>
<td>(h) SiGe HBT</td>
<td>Simple</td>
<td>0.1x2x1 / 0.1x6x2</td>
<td>1:6</td>
</tr>
<tr>
<td>(i) pMOS</td>
<td>CC</td>
<td>1x1x12 / 1x1x6</td>
<td>2:1</td>
</tr>
<tr>
<td>(j) pMOS</td>
<td>CC</td>
<td>0.5x2x2</td>
<td>1:1</td>
</tr>
</tbody>
</table>
CM Error (300K)

- **300 K: SiGe HBT CMs Have Less Errors Than CMOS CMs**
  - Early effect, self-heating $\ll$ drain-induced barrier lowering (DIBL) and channel-length modulation
CM Error (19K) — SiGe HBT vs. CMOS

• 19 K: All CMs have **Worse Errors** (due to base leakage and DIBL)
CM (19 K) Comparisons

• **Winner:** Simple CM with Large SiGe HBT
  – simple layout, reasonable accuracy, and robust operation across large range

• **Runner-up:** Cascode CM with SiGe HBT
  – trade-off: larger power + lower headroom, but lowest errors
Impact of Variability on LNAs

- **300 K vs 19 K**: Cryo-T Has Larger Variation in all Parameters
  - bandwidth uncertainty up to 30%
  - gain uncertainty up to 7 dB
  - noise temperature uncertainty up to 5 K

Needs To Be Modeled
Summary

- SiGe HBT Performance Metrics Naturally Improve with Cooling
  - operation down into the mK environment
  - new transport physics
  - collector current quenching below 40-50K (measurement / modeling)
  - isothermal compact models very doable for circuit design
  - device parameter variability is real; circuit impact needs further study

Stay Tuned … The Best is Yet to Come!

- SiGe Possesses Many Attributes for Emerging Quantum Systems
  - extreme levels of performance at modest lithography (THz coming!)
  - all the analog / RF / mmW circuit virtues of a bipolar transistor
  - all-the-bells-and-whistles BEOL + CMOS on board, as needed
  - SiGe = silicon technology (maturity, reliability, integration level, cost)