WSL-1

5G Sub-6GHz LO Frequency Synthesis, VCO Coupling Mitigation and On/Off Disturbance Reduction

Chih-Wei Yao, Joonhee Lee, and Sangwook Han

Samsung Electronics
Motivation

• System-level req. for cellular LO/PLL
• LO/PLL designs for multi-standard (2/3/4/5G) cellular radio
Outline

• Cellular Freq. Gen. & Dist. Challenges
  – Multiple modes: 2/3/4/5G, TDD/FDD, up to 1024QAM
  – Multiple bands and carrier aggregation (CA)
    • Coupling: VCO-to-Rx, VCO-to-VCO, Tx-to-VCO
    • On/off disturbance reduction
  – Low power: turn off whenever possible
    • Fast pwr-up techniques

• Low power, High perf. PLL design
  – ADC-assisted coarse/fine TDC, TDC Chopping, TDC NL Cal
5G and Implication to RFIC Design

Circuit turns on/off more often in TDD mode to reduce power

More bands, more CA, including LTE+5G CA
2G Support

- 2G GMSK (Single-Carrier): Diff. req. from 4G/5G
  - Low phase noise VCO w/o SAW filter
  - Low BW PLL (~50kHz) to reduce PN @ 200kHz~600kHz

- Challenging for sub-sampling/sampling PLLs

<table>
<thead>
<tr>
<th>Band</th>
<th>Parameter</th>
<th>Unit</th>
<th>LB</th>
<th>HB</th>
</tr>
</thead>
<tbody>
<tr>
<td>2G Rx</td>
<td>Frequency</td>
<td>MHz</td>
<td>869~960</td>
<td>1805~1990</td>
</tr>
<tr>
<td></td>
<td>PN@200kHz</td>
<td>dBC/Hz</td>
<td>-71.01</td>
<td>-71.01</td>
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<tr>
<td></td>
<td>PN@400kHz</td>
<td>dBC/Hz</td>
<td>-103.01</td>
<td>-103.01</td>
</tr>
<tr>
<td></td>
<td>PN@600kHz (~1.6MHz)</td>
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<td>dBC/Hz</td>
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<tr>
<td></td>
<td>PN@3MHz</td>
<td>dBC/Hz</td>
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<td>-138.01</td>
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<td></td>
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<td>2G Tx</td>
<td>Frequency</td>
<td>MHz</td>
<td>824~915</td>
<td>1710~1910</td>
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<tr>
<td></td>
<td>PN@400kHz</td>
<td>dBC/Hz</td>
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<td>-117</td>
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<td></td>
<td>PN@20MHz</td>
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<td>-160</td>
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Very stringent VCO phase noise requirement
Low PLL BW
2G Support

• To re-use VCO for 2/3/4/5G, s/w btw NMOS/CMOS modes

2G: NMOS Mode

3/4/5: CMOS Mode
Sub-Sampling/Sampling PLL BW

- Sampling phase detector (SPD) gain ≈ $2\pi f_{vco} A_{vco} \approx 5-20$ GV/sec
- Need low $G_m$ and low duty-cycle to reduce loop-gain
- Difficult for BW < 100kHz
2G Support

- To eliminate Tx mixer noise, need phase modulation
  - Natural for Dig. PLLs
    - Easy DCO gain CAL / Background CAL
  - Analog PLL
    - Need VCO digital tuning & digital counters
4G/5G Support

• Need low Integ. Phase Noise (IPN)
  – 4x4 MIMO 1024QAM SSB IPN < -47 dBc (1kHz~10MHz)
  – IPN limits EVM with sufficient sig. pwr
  – MIMO: Need better IPN for deep-fading channels
  – CMOS DCXO increases phase noise from 1kHz~10kHz
UL-MIMO Phase Continuity

- UL-MIMO beam steering → const. sum. @ base-station
  - Phase btw TX1/TX2 as we turn on/off

Same for Tx MIMO

Sync Sequence

Same Relative Phase
UL-MIMO Phase Continuity

- TDC+decoder reports to modem
- Modem adjusts CORDIC (on RFIC) fix Tx phase
- Adjustment continues until goal is reached
FDD Support

- Needs low LO PN floor to prevent Rx desens
  - Tx leak to Rx band, Rx reciprocal mixing

Diagram:
- Duplexer
- LNA
- PA
- RX LO
- TX LO
- Rx LO Phase Noise
- Tx LO Phase Noise
- Rx Input
- Rx wanted signal
- Tx leak down-mixed by Rx LO PN
- Tx leak to Rx-band
- Due to Tx LO PN up-mix
- PA Output
- Rx Band
- TX LO
- TX LO
- TX LO
- TX LO
- Rx LO Phase Noise
- Rx LO Phase Noise
TDD Support

- Tx/Rx physically away → use different PLL/LO
  - To reduce power, PLL/LO turns on/off
  - PLL/LO settling time = power overhead
    - Min. T/R S/W Period: TDD LTE → 5 ms, 5G FR1 → 1.25 ms
    - 50us pwr-up time: LTE → 2%, 5G → 8%

![Diagram showing TDD LTE and 5G FR1 power-up times and settling times.](image-url)

TDD LTE: Min. 5 ms, 5G: Min. ~1.25 ms
Fast PLL/LO Settling

- VCO Reg BW < 10kHz to filter noise
- Power Up Procedure
  - Set VCO Reg 200kHz to help start-up
  - Set VCO Reg to 3kHz to reduce supply noise
  - Slow VCO Reg settling is corrected by PLL (300kHz~400kHz BW)
  - All other REG have 200kHz BW
Multiple Bands Support

• Ever-increasing number of bands
  – Incl. LAA (LTE-U) and NR-U
CA Support: Tx-VCO, VCO-Rx Coup.

Band 1

- **TX**: 1920 ~1980
- **RX**: 2110 ~2170

Band 3

- TX: 1710 ~1785
- RX: 1805 ~1880

- B3 TX
- B19 RXVCO

Band 19

- TX: 830 ~845
- RX: 875 ~890

- TX 2nd: 1660 ~1690
- RX 2LO: 1750 ~1780

- TX 4th: 3320 ~3380
- B19 RXVCO: 3500 ~3560
- TX 5th: 4150 ~4225
- RX 5LO: 4375 ~4450

- B3 2nd TX
- B19 RXVCO

Band 42(TDD)

- TX: B19 2nd RXLO
- RX: B19 2nd RXLO

- 1st TRX: 3400 ~3600

**Note**: This figure is not to scale.
CA Support: VCO-to-VCO Coup.

B3 RX
1805 ~1880 MHz

B3 TX
1710~1785 MHz

B8 RX
925 ~960 MHz

B8 TX
880 ~915 MHz

LNA
LPF
DIV-2
LPF
DIV-2

LPF
3610 ~3860 MHz
LPF
3420~3570 MHz

LPF
3700 ~3840 MHz
LPF
3520~3660 MHz

LPF
DIV-4
LPF
DIV-4

LPF
DIV-6
LPF
DIV-6

5500 ~5760 MHz
5280~5490 MHz
CA Support: Mitigate Coupling

- Choose LOIQ Gen ratio to shift VCO frequency
- Use 2\textsuperscript{nd} stg PLL (SSPLL) for UHB and NR bands
  - Rx SSPLL uses ring-osc to reduce area
  - Multiple synth ratios to help mitigate coupling
Ring Osc. Inj. Lock SSPLL

- Generate I/Q directly
- Inject at nodes at diff. time to improve PN
CA support: On/Off Disturbance

- Multiple PLL/LO On/Off
  - Supply disturbance: separate balls (star conn. PCB) + regulator
  - Shared bias disturbance: add RC filter and Active LPF
  - Ref clock disturbance: isolation buffers

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<th>CCn</th>
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<th>OFF</th>
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<td>CC2</td>
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<td>CC3</td>
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<td>CC4</td>
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</tr>
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<td>CC2</td>
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<tr>
<td>CC3</td>
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<tr>
<td>CC4</td>
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Bias Disturbance and Solution

Shared node
Strong on/off isolation

One copy for each PLL and each LOIQ Gen

Live with on/off disturbance
Use PLL BW to correct slow settling

10 kHz BW for Noise filtering

3 kHz

Bias Disturbance and Solution
Ref Clock Disturbance and Solution

CLKREF

Ref Clock Buf

LDO
RX PLL
Keep-on
To reduce on/off disturbance

LDO
TX PLL
Keep-on
To reduce on/off disturbance
Low Power by Turning Off Circuits

• Explore all opportunities to turn off circuits
  – 3G voice call (CDMA)
    • SNR increase as time
    • Turn off RFIC once incoming symbol has sufficient SNR

<table>
<thead>
<tr>
<th>Symbol i</th>
<th>Symbol i+1</th>
<th>Symbol i+2</th>
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<tr>
<td>SNR (from Modem)</td>
<td>SNR Target</td>
<td>Time</td>
</tr>
<tr>
<td>PLL/LO Pwr-Up</td>
<td></td>
<td>Settling Time</td>
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</tbody>
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Low Power by Turning Off Circuits

– Voice over LTE (VoLTE)
  • First two sym in PDCCH (DL Control Info.)
  • If no data in sub-frame, turn-off Tx/Rx/LO

Symbols

PLL/LO Pwr Up

Sub-Frame (1msec)

Power-Down Time ~810 usec

No data in Sub-Frame
Digital PLL for Cellular RFIC

• Benefits
  – One solution for all
    • BW: 10kHz~1MHz BW
    • Supports phase modulation
    • Fast settling
  – Modular Design
    • TDC & Dgt. Circuit can be reused
    • Only DCO needs customization

• Limitations
  – Stringent 2G/FDD P/N (20~300MHz): -154~-160 dBc/Hz
    • DCO fine-tune extra cap → limits VCO tuning range / pwr
  – High reference frequency (> 52MHz) operation
Digital PLL Architecture

- Based on ΔΣ fractional-\(N\) PLL
- Captures both Pos/Neg Phase Errors
- Speed-Up Locking
- Supports TDC Chopping
- TDC nonlinearity calibration
TDC Chopping

- A chopping TDC resembles a chopping amplifier
- Phase error polarity sequence from MASH111 ΔΣM
  - Noise-shaped to high frequency. Good for chopping
- TDC and regulator flicker noise is up-mixed
TDC Chopping
TDC Fine-Conversion Algorithm

Ring-Oscillator Output Nodes

Time captured by TDC coarse measurement

Instant that ends TDC measurement

Timing information reported by fine-conversion

\[ T_{res\_coarse}: \text{Coarse TDC resolution} = \frac{T_{ro\_per}}{N_{stg}} \]

Slope = \( \frac{(V_1-V_2)}{T_{res\_coarse}} \)

\[ T_{fine} = \frac{(V_1-V_{ref})}{Slope} \]

\[ = \left[ \frac{(V_1-V_{ref})/(V_1-V_2)} \right] T_{res\_coarse} \]

\[ = \left[ \frac{V_1}{(V_1-V_2)-T_{offset}} \right] T_{res\_coarse} \]

Let’s choose \( V_{ref} \) be the mid-point between supply and ground

\[ T_{offset} = \sim 0.5 (V_1-V_2) \]

\[ T_{fine} = \left[ \frac{V_1}{(V_1-V_2)-0.5} \right] T_{res\_coarse} \]
TDC Fine-Conversion Algorithm

\[ V_1 = V_1(t_{in}) \]
\[ V_2 = V_2(t_{in}) \]
\[ T_{\text{fine}} = T_{\text{fine}}(t_{in}) \]
\[ \text{Slope} = \frac{(V_1 - V_2)}{T_{\text{coarse}}} \]
\[ T_{\text{fine}} = \frac{V_1}{(V_1 - V_2)} \cdot T_{\text{coarse}} \]
TDC Design

- TDC RST initializes phase (set R.O. node voltages)
- EN H: R.O. starts to run, EN L: holds node voltages
- Voltage buffer + Res interpolator improves linearity
- Two node voltages selected for fine-conversion
TDC Fine-Conversion and Resolution

Selected Voltage Number: \( N_{ADC} = 9 \)

\( X_{DM}[12:0] = X[12:0] - XB[12:0] \)

Selected sampling voltages for SARADCs:
\( XS1 = X[9], XS1B = XB[9]. XS2 = X[10], XS2B = XB[10] \)

TDC Resolution

\[ \tau_{res} \approx \frac{T_{RO_{-}per}}{N_{stg}} \left( \frac{1}{V1} - \frac{1}{V2} \right) \]

- \( T_{RO_{-}per} \) Ring-oscillator free-running period
- \( N_{stg} \) Number of ring-oscillator delay cells
- \( (V1-V2) \) Average code difference of two SARADCs

For this design, with 7b SARADCs

\[ T_{res} = \frac{120 \text{ ps}}{13} \left( \frac{1}{46} \right) = 0.2 \text{ ps} \]
- TDC is based on a R.O., NL pattern repeats every R.O. period.
- 13-stage R.O. -> 13 zones within a R.O. period
- 4 regions per zone, 52 regions total
- Estimate the TDC error for each region remove it from incoming samples
- One-time calibration: Run PLL at a selected frequency
TDC Nonlinearity Calibration

TDC Nonlinearity after compensation

52 Regions

Timing Error (% TDC Periods)

Time (TDC periods)
TDC Error Over Temperature

- Post-layout sim w/ device mismatch
DCO fine-tuning

10-bit fine-tuning (32x32 Array) with Thermometer Decoder
Phase Noise Measurement

- 1 dB IPN degradation over +/- 60°C w/o Re-CAL
Reference Spur

\[ \text{fvco} = 5382.05 \text{ MHz} = 207*\text{fref} + 50 \text{ kHz} \]

2691.025 MHz

With TDC Calibration

500 kHz

Without TDC Calibration

500 kHz

35.9 dB Improvement

\[ \Delta \text{Mkr1 150 kHz} \quad -78.651 \text{ dB} \]

\[ \Delta \text{Mkr1 150 kHz} \quad -42.757 \text{ dB} \]

Reference spur -87.67 dBC
Fractional-N Spurs
TDC Calibration over Mult. Samples

- Nonlinearity is dominated by layout mismatch
- Temperature dependency of TDC CAL result can be reduced by improving layout
Power Consumption and Micrograph

### Chip Micrograph

<table>
<thead>
<tr>
<th>Component</th>
<th>Power Consumption (mW)</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>PFD, TDC and SARADCs</td>
<td>1.8</td>
<td>13.43%</td>
</tr>
<tr>
<td>DCO</td>
<td>6.1</td>
<td>45.52%</td>
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<tr>
<td>DCO dithering</td>
<td>0.6</td>
<td>4.48%</td>
</tr>
<tr>
<td>DCO buffers</td>
<td>3</td>
<td>22.39%</td>
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<tr>
<td>Feedback Divider</td>
<td>1</td>
<td>7.46%</td>
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<tr>
<td>Digital PLL Digital Circuit</td>
<td>0.9</td>
<td>6.72%</td>
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<tr>
<td><strong>Total</strong></td>
<td><strong>13.4</strong></td>
<td><strong>100.00%</strong></td>
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Active Area = 0.257 mm$^2$
# Performance Summary

<table>
<thead>
<tr>
<th></th>
<th>Yao JSSC 2013</th>
<th>Gao ISSCC 2016</th>
<th>Levantino JSSC 2014</th>
<th>Temporiti JSSC 2010</th>
<th>Wang ISSCC 2008</th>
<th>This Work</th>
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<tbody>
<tr>
<td>Technology</td>
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<td>28 nm</td>
<td>65 nm</td>
<td>65 nm</td>
<td>180 nm</td>
<td>14 nm</td>
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<td>0.3</td>
<td>6.8</td>
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<td>Reference (MHz)</td>
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<td>40</td>
<td>40</td>
<td>35</td>
<td>12</td>
<td>26</td>
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<tr>
<td>Output Frequency (MHz)</td>
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<td>5825.1</td>
<td>3600</td>
<td>3500</td>
<td>2400</td>
<td>2690</td>
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<tr>
<td>RMS jitter (fsec)</td>
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<td>159</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>137</td>
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<tr>
<td>In-band Phase Noise (dBC/Hz) 100 kHz</td>
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<td>-105.5</td>
<td>-103</td>
<td>-101</td>
<td>-98</td>
<td>-113.6</td>
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<tr>
<td>In-band PN Normalized to 2690 MHz (dBC/Hz)</td>
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<td>-112.2</td>
<td>-105.53</td>
<td>-103.3</td>
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<td>Near-integer Fractional spur</td>
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<td>-58</td>
<td>-64</td>
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<td>Area (mm^2)</td>
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<td>0.44</td>
<td>4</td>
<td>0.257</td>
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Conclusions

• An overview of cellular LO techniques for
  – Multi-standards supports: 2/3/4/5G, FDD/TDD, CA
  – TX/RX/VCO coupling mitigation
  – Low power consumption: turn off whenever possible

• Design of a low-power, low spur digital PLL
  – Meets all requirements 2/3/4/5G FR1
  – Coarse/fine conversion TDC
  – TDC chopping
  – TDC nonlinearity calibration
References


References
