Rad Hard By Design: A Necessity for Today’s Critical Space Missions

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BAE SYSTEMS
• Motivation
  – Space Missions: Why Rad Hard By Design (RHBD)?

• Mission Requirements Overview
  – Performance, Power, Radiation, Reliability

• Architecting RHBD Integrated Circuits (ICs) for Space
  – Requirements Specification
  – Technology Characterization
  – Design Hardening
  – Verification and Validation
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SPACE MISSIONS: WHY RAD HARD BY DESIGN?
Why RHBD for Space?

• The breadth of space-based electronics missions is expanding
  – Satellite systems are evolving in response to expanding mission requirements
  – The demand for high-performance processing & networking capabilities is rapidly increasing

• Constraints associated with the operating environment drive need for efficiency & reliability
  – The launch cost per unit weight is staggering
  – Space environment limits power availability, complicates thermal dissipation, and eliminates the ability to repair/replace components

• Availability of dedicated rad hard semiconductor foundries is limited at advanced technology nodes
Space Systems Missions

Mission Profiles
• Applications
  – Communications
  – Positioning/Navigation
  – Weather
  – Remote Sensing
• Users
  – Civil
  – Commercial
  – Military

Electronic Functions
• Command & Control
• Data Management
  – Networking
  – Processing
  – Storage
• Sensor Interfaces
  – Analog
  – Digital
  – RF
• Power
Environmental Constraints

• Costs inhibit satellite replacement
  – Cost of the satellite itself
  – Cost of launch
  – Systems cannot be repaired

• Space systems need to:
  1) Last longer than terrestrial counterparts
     • LEO: 2-5 years
     • MEO, GEO: 10-15 years
  2) In harsher conditions
     • Temperature: -55°C - 125°C
     • Space radiation environments
  3) On a fixed power budget
     • 100W-20kW (2015 Avg. US Household: 1.2kW)

LEO: Low Earth Orbit    MEO: Medium Earth Orbit    GEO: Geosynchronous Earth Orbit

Advertised/Estimated Launch Cost per kg

<table>
<thead>
<tr>
<th>Rocket</th>
<th>LEO</th>
<th>GTO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Falcon 9¹</td>
<td>Falcon Heavy¹</td>
<td>Atlas V (Min)²,³</td>
</tr>
<tr>
<td>$-</td>
<td>$-</td>
<td>$-</td>
</tr>
</tbody>
</table>

³https://www.rocketbuilder.com/
⁴https://en.wikipedia.org/wiki/Delta_IV
⁵http://breakingdefense.com/2014/05/ula-fires-back-at-spacex-at-space-symposium-details-launch-costs/

3https://www.rocketbuilder.com/
5http://breakingdefense.com/2014/05/ula-fires-back-at-spacex-at-space-symposium-details-launch-costs/
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RAD HARD BY DESIGN IN SPACE: MISSION REQUIREMENTS
Challenges of Designing for Hi-Reliability

- Environmental Stresses:
  - Temperature extremes & cycles
  - Applied voltage
  - Operational lifetime

- Device Strengths:
  - The ability of a device to withstand a stress
    - Changes over time

- Physics of Failure:
  - Time Dependent Dielectric Breakdown (TDDB)
  - Positive/Negative Bias Threshold Instability (BTI)
  - Electromigration (EM)
  - Hot Carrier Injection (HCI)
  - Radiation


Operating in a space environment increases the stress profile and creates a larger shift between beginning and end of life strength profiles.
The orbital environment is dictated by the mission at hand, and can carry a variety of environmental challenges.
# Environmental Radiation Sources

<table>
<thead>
<tr>
<th>Radiation Source</th>
<th>Types of Orbits Affected</th>
<th>Effects of Solar Cycle</th>
<th>Variations</th>
</tr>
</thead>
</table>
| Trapped Protons           | LEO, MEO, HEO, Transfer Orbits   | Solar Min – Higher Solar Max - Lower | • Geomagnetic Field  
• Solar Flares  
• Geomagnetic Storms |
| Trapped Electrons         | LEO, GEO, HEO, Transfer Orbits   | Solar Min – Lower Solar Max - Higher | • Geomagnetic Field  
• Solar Flares  
• Geomagnetic Storms |
| Galactic Cosmic Ray Ions  | LEO, GEO, HEO, Interplanetary    | Solar Min - Higher Solar Max - Lower | • Ionization Level  
• Orbit Attenuation |
| Solar Flare Protons       | LEO (I>45°), GEO, HEO, Interplanetary | During Solar Max Only               | • Distance from Sun  
• Outside 1 AU, Orbit Attenuation;  
• Location of Flare on Sun |
| Solar Flare Heavy Ions    | LEO, GEO, HEO, Interplanetary    | During Solar Max Only               | • Distance from Sun;  
• Outside 1 AU, Orbit Attenuation  
• Location of Flare on Sun |

https://radhome.gsfc.nasa.gov/radhome/papers/aspen.htm

LEO: Low Earth Orbit    
MEO: Medium Earth Orbit    
GEO: Geosynchronous Earth Orbit   
HEO: Highly Elliptical Orbit

AU: Astronomical Unit (avg. distance from Earth to Sun)
Environmental Radiation Effects

**Life-Limiting Effects**

- **Total Ionizing Dose (TID)**
  - Protons & Electrons
  - Ionizing charge buildup in semiconductors
  - Parametric degradation, functional failure

- **Displacement Damage Dose (DDD)**
  - Protons
  - Atomic dislocation buildup in semiconductors
  - Parametric degradation, functional failure

- **Single Event Latchup (SEL)**
  - Galactic Cosmic Ray Ions & Protons
  - Ionization-induced latchup
  - Functional interruption, reduction in reliability, permanent failure

**Performance-Limiting Effects**

- **Single Event Effects (SEE)**
  - Galactic Cosmic Ray Ions & Protons
  - Single Event Upsets (SEU)
    - Persistent data corruption
  - Single Event Transients (SET)
    - Spurious analog signals
    - Logical miscues
  - Single Event Functional Interrupt (SEFI)
    - Example: upset resulting in electronic device misconfiguration

The probability and severity of radiation effect occurrence is driven by the operating environment and the architecture/implementation of the system.
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RAD HARD BY DESIGN IN SPACE: ARCHITECTURE & DESIGN TRADES
Designing ICs for Space

Requirements Specification
- Environment
- Reliability
- Functional
- Performance

Design Hardening
- Architecture & Design Trades

Technology Characterization
- Semiconductor process selection & characterization

Verification & Validation
- Enhanced DRC
- Radiation/Reliability Analysis
Architecture & Design Trades

REQUIREMENTS SPECIFICATION
**Requirements Specification**

- Space system architecture drives variety of potential use-cases for ICs
- Understanding primary functional and interface requirements is key to being able to make intelligent architecture & environmental trades
- Cost of design & fabrication for small build quantities influences architecture
Understand the System Concept of Operations

- Architecture trades are driven by intended application & associated performance requirements
  - General-Purpose Processing
    - Command/Control of satellite, payloads, processors, instrumentation, data storage, etc
  - Instrumentation Interfaces
    - Analog/mixed-signal (AMS) ASICs bridge between the digital domain and sensors analog/RF kHz-GHz interfaces
  - Digital Signal Processing
    - Sophisticated processing algorithms data collected by the on-board sensors & instruments are run prior to off-loading
  - Data Networking
    - Data needs to be routed across the system at Gbaud-rates between sensors, processors, memory, and transmitters
  - Reusability/Reconfigurability?

The IC designer has tools to meet a wide range of performance, power, radiation, and reliability challenges, but not without trade-offs.
Economy of Scale: Space Electronics

- **Space ICs:**
  - Small-scale production
  - Fixed mask & foundry costs
- Design process is tailored towards risk avoidance

https://www.extremetech.com/computing/272096-3nm-process-node
Architecture & Design Trades

TECHNOLOGY CHARACTERIZATION
Semiconductor Technology Characteristics

• Radiation & reliability are technology and process dependent

• IC manufacturers are unlikely to modify process for space quantities

• Foundry & technology selection needs to be knowledgeable of process characteristics

Requirements Specification

Design Hardening

Technology Characterization

Verification & Validation
Total Ionizing Dose in Modern Processes

Planar Technologies

- Thinner oxides & pristine interfaces improve TID response

Warning: Bulk field effects, FDSOI edge effects

3-D Technologies (FinFETs)

- New geometries = new variables, but the trend continues

Process and design trades need be TID-conscious, but 100krd-level tolerance is achievable.


Total Ionizing/Non-Ionizing Dose Characterization

Characterization Process

- **Test structures**
  - Transistors, capacitors, field oxide, and SRAM structures
  - Representative of $V_T$’s, gate dimensions, oxide thicknesses and transistor spacing

- **Facilities**
  - TID: Gamma Ray, X-ray, proton sources
  - DDD: Proton, neutron sources

- **Measurements**
  - $I_D-V_G$ curves
  - Subthreshold leakage
SEE in Modern Processes

- Critical charge
  - The amount of charge needed to flip a bit is decreasing
- Sensitive volume
  - The volume of silicon where a transient ion contributes to $Q_{crit}$ is shrinking
- On-chip density
  - The number of sensitive elements is increasing
- IC complexity
  - Interaction between circuits during SEE can be difficult to predict

Relative Upset Rates vs. Technology Node

SEE characteristics of technology/process drive design-specific impact assessment.

R. Baumann, IEEE Nuclear and Space Radiation Effect Conference, Short Course 2013.
Single Event Effects Characterization

Characterization Process

- Test structures
  - SRAMs, logic chains, SET test circuits
- Facilities
  - Heavy ion and proton accelerators
- Measurements
  - Cross-section vs. LET/Energy
  - Transient pulse-widths
  - Latchup susceptibility
- Data uses
  - Influence design requirements
  - Calibrate models

SET Characterization Example

Reliability in Modern Processes

- Time Dependent Dielectric Breakdown (TDDB)
  - Applied electric fields gradually lower resistivity in gate oxides
- Hot Carrier Injection (HCI)
  - High-energy carriers in the drain inject into gate oxide & degrade I-V characteristics
- Positive/Negative Bias Threshold Instability (BTI)
  - Gate oxide interface states trap charge & shift $V_T$
- Electromigration (EM)
  - Charge carriers increase resistivity in metal interconnects
- Time, voltage, temperature, and geometry dependent

Space mission requirements exceed typical foundry characterization corners. Mission-specific qualification is usually required for technology insertion program.

Architecture & Design Trades

DESIGN HARDENING
IC Design for High-Reliability

- Perform criticality assessment on sub-blocks
- Choose sub-block IP that is most appropriate
- Implement system-level mitigation where possible and necessary
Critcality Considerations

Where might we tolerate failure?

- Functions protected by system-mitigation (ECC, etc)
  - DDR Interface
  - Data caches
- Secondary functions
  - Telemetry
- Data throughput
  - Downstream filtering/processing, error correction
  - Data caches
  - ADC/DAC
  - SerDes core

Where can’t we tolerate failure?

- Power distribution
  - Regulators and references
  - Target for RHBD
- Clock and reset networks
  - PLL, POR, distribution trees
  - Cause massive SoC interrupt
  - RHBD/Brute-force mitigation
- Mode registers
  - May require outside-intervention to rectify

Opportunities to target high-density or high-performance circuit implementation

High-criticality functions need to prioritize reliability over performance & density
## Integrated Circuit IP Trade Space

<table>
<thead>
<tr>
<th></th>
<th>Custom Design</th>
<th>Standard Cell</th>
<th>Hard IP (3rd-party)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Overview</strong></td>
<td>Circuit function designed specifically for application.</td>
<td>Circuit function built from 3rd-party library elements, for licensing fee.</td>
<td>Drop-in 3rd-party block to provide specific function.</td>
</tr>
<tr>
<td><strong>Implementation Cost</strong></td>
<td>Design process, tools, and expertise.</td>
<td>Library license fee. Synthesis, PD, and verification expertise.</td>
<td>Block license fee. PD and verification expertise.</td>
</tr>
</tbody>
</table>

Hybrid Approach: Modern RHBD ICs typically use a combination of commercial standard cell libraries, RHBD standard cell libraries and hard IP blocks.
## Integrated Circuit IP Trade Space

<table>
<thead>
<tr>
<th>Benefits</th>
<th>Custom Design</th>
<th>Standard Cell</th>
<th>Hard IP (3rd-party)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constraints</td>
<td>Risk of first use. Costly design process.</td>
<td>Some required functions may not be supported/achievable. Locked into process/foundry.</td>
<td>No flexibility in form/fit/function, or SWaP. Locked into process/foundry.</td>
</tr>
<tr>
<td>Radiation Effects</td>
<td>Bottoms-up RHBD-capability.</td>
<td>RHBD libraries available. Non-RHBD adds risk, but can be assessed.</td>
<td>Varies by design. Limited analysis possible, and may not be available in time to be useful.</td>
</tr>
<tr>
<td>Reliability</td>
<td>Maximum flexibility: FEOL and BEOL.</td>
<td>FEOL-constrained, BEOL-flexible.</td>
<td>Varies by design. Limited analysis possible, and may not be available in time to be useful.</td>
</tr>
</tbody>
</table>
Embedded Memory Considerations

- Cell Characteristics
  - Technology
  - Topology
  - Environment

- Error Correction Code
  - Strength
  - Area/Power/Performance penalties

- Memory Scrubbing

http://electroiq.com/blog/2014/02/the-most-expensive-sram-in-the-world-2-0/

- Majority of chip area dedicated to memory
  - Data buffers
  - Data/instruction cache
  - Scratchpad memory
  - Application-specific instantiations

- Major implications on IC power, performance, and radiation/reliability
# SRAM Cell SEE Characteristics

## 90nm SRAM Cell Parameters by Topology, normalized to Commercial

<table>
<thead>
<tr>
<th>SRAM Bit Cell</th>
<th>Area</th>
<th>Setup + Access Time</th>
<th>Power (1kx72 array)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>1</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>High-performance, high-density RHBD</td>
<td>2.3</td>
<td>0.9</td>
<td>1.7</td>
</tr>
<tr>
<td>Multi-Mrd RHBD</td>
<td>3.6</td>
<td>1.8</td>
<td>2.5</td>
</tr>
</tbody>
</table>


## SRAM Upset Rates by Technology Node and Orbit (upsets-bit/day)

<table>
<thead>
<tr>
<th>ORBIT</th>
<th>20nm Ultra-Scale</th>
<th>45nm Global Foundries</th>
<th>45nm BAE Systems</th>
<th>65nm Global Foundries</th>
<th>65nm Xilinx (V5QV)</th>
<th>65nm Cypress</th>
</tr>
</thead>
<tbody>
<tr>
<td>GEO, Background</td>
<td>7.1x10^-9</td>
<td>4.5x10^-8</td>
<td>9.6x10^-10</td>
<td>7.0x10^-8</td>
<td>1.4x10^-6</td>
<td>2.5x10^-7</td>
</tr>
<tr>
<td>GEO, Solar Flare</td>
<td>9.6x10^-6</td>
<td>2.0x10^-4</td>
<td>1.9x10^-6</td>
<td>2.6x10^-4</td>
<td>4.7x10^-3</td>
<td>4.8x10^-4</td>
</tr>
<tr>
<td>1400 km</td>
<td>3.6x10^-7</td>
<td>1.4x10^-6</td>
<td>6.2x10^-8</td>
<td>2.1x10^-6</td>
<td>6.6x10^-6</td>
<td>4.6x10^-6</td>
</tr>
<tr>
<td>ISS</td>
<td>7.6x10^-9</td>
<td>3.0x10^-8</td>
<td>1.3x10^-9</td>
<td>4.7x10^-8</td>
<td>3.1x10^-7</td>
<td>1.1x10^-7</td>
</tr>
</tbody>
</table>

Memory Hardening: ECC

ECC Impacts on Array Error Rates

ECC Impacts on Memory Arrays: Area & Power

<table>
<thead>
<tr>
<th>Array</th>
<th>ECC?</th>
<th>Data Bits</th>
<th>Parity Bits</th>
<th>Total Bits</th>
<th>Area/Pwr Penalty</th>
</tr>
</thead>
<tbody>
<tr>
<td>8k x8</td>
<td>No</td>
<td>65536</td>
<td>-</td>
<td>65,536</td>
<td>0%</td>
</tr>
<tr>
<td>8k x8</td>
<td>SECDED</td>
<td>65536</td>
<td>40,960</td>
<td>106,496</td>
<td>63%</td>
</tr>
<tr>
<td>2k x32</td>
<td>SECDED</td>
<td>65536</td>
<td>14,336</td>
<td>79,872</td>
<td>22%</td>
</tr>
</tbody>
</table>

SECDED: Single Error Correct, Double Error Detect

Applying ECC reduces effective error rate in exchange for area, power, complexity, latency.
ECC and Multiple Bit Upsets

- Probability of multiple bits upsetting (MBU) from single particle strike increases with scaling
  - Scaling increases density of SRAM cells
- MBUs in a single data word complicate ECC
  - Column muxing: physically separating logical neighbors limits this effect

Logic SEE Characteristics: Clock Rate

**Logical Capture of SET**

- Decreasing clock period increases probability of SET interfering with setup and hold

**Logic SEU Sensitivity vs. Frequency**

- SEU sensitivity scales linearly with clock frequency

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Implementing logic functions trade performance for SEE sensitivity (and power)

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Logic SEE Characteristics: Power

- Increased supply voltage increases the critical charge of the circuit
- Increased drive strength dissipates single event generated charge

SEE mitigation by power is effective but costly: use wisely!


Fault Tolerance: Internal Redundancy

**Spatial Redundancy**
- Triple-mode redundancy
- 3x Area/power penalty

**Temporal Redundancy**
- Temporal filtering
- Propagation delay penalty
Analog/Mixed Signal Considerations

Single Event Effects

- Single Event Transients are extremely context-dependent
  - Circuit function & design
  - Bias/loading conditions
    - Current & capacitance
  - Considerable RHBD solutions

- System mitigation:
  - Understand a block’s output transient characteristics
  - Apply block-level compensation
  - Harden configuration logic

Total Ionizing Dose

- Thick-gate oxide devices, larger overall geometries, and linear operation increase TID sensitivity
- RHBD by construction e.g. SiGe HBT

SET Characterization of RHBD Folded-Cascode Op-Amp Topologies

Architecture & Design Trades

VERIFICATION AND VALIDATION
Verification and Validation

- Design rule checks can be modified to check radiation & reliability coverage
- Bottoms-up SEE analysis rolls characterization data up to system-level requirements
- Chip qualification and radiation testing validates the design before flight
Modifying Design Rule Checks for Hi-Rel

Reliability

- Time Dependent Dielectric Breakdown (TDBB)
  - Gate oxide area
  - Supply voltage
- Hot Carrier Injection (HCI)
  - Channel length
  - Supply voltage
- Pos/Neg Bias Threshold Instability (BTI)
  - Device utilization
  - Duty factor
- Electromigration (EM)
  - Current density
  - Metal widths/lengths
  - Contact density

Radiation

- Total Ionizing Dose (TID)
  - Device spacing
  - Guardrings
  - Device utilization
    - \( V_T \), oxide thickness, device geometry
- Single Event Latchup (SEL)
  - Well contact density
  - Guardrings
  - Supply voltage

Technology characterization may drive additional design rule rigor.
Integrated Circuit SEE Model

IC SEE modeling follows a bottoms-up methodology and is updated as database evolves. The top level model should aggregate error rate predictions and compare against system requirements.
RHBD IC Flight Qualification

• Qualification testing performed on the final product validates the ability of the chip to meet design requirements
  – Electrical, Mechanical, Extended-Life, Packaging and Radiation
  – Reflective of temperature, lifetime, and functional requirements
  – Qualification plan is agreed to by all parties/stakeholders
    • Reflects the process/technology pedigree, the mission requirements & reliability goals

• Various qualification standards available
  – MIL-PRF-38535
  – MIL-STD-883
  – JEDEC JEP148A
  – ESA 2269000
RHBD IC Radiation Testing

Single Event Effects
• Heavy ion, proton accelerator
• Multiple test modes required
  – Dynamic performance validation
    • Near real-time error detection required
  – Static model validation
    • Built-in memory test, register scan chains
• Test Preparation
  – Remote operation of test equipment
  – Devices de-lidded and thinned

Total Dose
• Electrical testing of critical parameters
  – Multiple dose/characterization steps
  – Dose fixture needs to be free of sensitive components
• Gamma/neutron or proton source
  – Coordinate production test capability with total dose source
• Various sample size scenarios available per qualification standards
Summary

• Operating in space presents unique and complex challenges
• Rad Hard By Design is an effective approach for mitigating radiation effects in modern integrated circuits
• Designing integrated circuits for space requires careful balancing of performance, power, reliability and radiation hardening
Acknowledgements

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